ASICs

Digital and Mixed-Signal

Brochure

September 2016

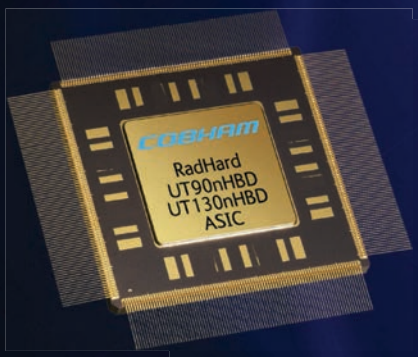
COBHAM

Digital and Mixed-Signal custom, semi-custom, off-the-shelf designs with Cobham Gaisler IP

Guaranteed radiation performance

QML-V, QML-Q, QML-Y, military, medical, industrial grades

Category 1A Trusted Accreditation



RadHard ASICs

- Multiple product assurance levels - QML Q, V and Y, military, medical and industrial
- Radiation hardened from 100 krad(Si) to 1 Megarad(Si) total dose available using Cobham RadHard techniques
- SEU-immune <1.0E-10 errors/bits-day or better using special library cells
- Robust Cobham Design Library of cells and macros
- Full complement of industry standard IP cores and Cobham Gaisler IP
- Configurable RAM compilers
- Support of cold sparing for power-down applications
- External chip capacitor attachment option available to space-quality levels for improved SSO response
- Drop-in FPGA conversion solutions

RADHARD ASIC RADIATION DATA

PARAMETER	RADIATION DATA
Total Ionizing Dose [1]	1.0E5 rad(Si) 3.0E5 rad(Si) 1.0E6 rad(Si)
Single Event Upset [2, 4]	UT90nHBD < 2.1E-11 errors/bit-day UT130nHBD < 2.4E-11 errors/bit-day UT180nHBD < 1.0E-12 errors/bit-day UT0.25µHBD < 1.6E-12 errors/bit-day UT0.35µHBD < 1.0E-12 errors/bit-day UT0.6µCRH < 5.7E-11 errors/bit-day
Single Event Latchup	Latchup-immune ≤ 110 MeV-cm^2/mg @ 125˚C
Dose Rate Upset [3]	≤ 6.6E9 rad(Si)/sec
Dose Rate Survivability	≤ 4.8E11 rad(Si)/sec
Projected Neutron Fluence	≤ 1.0E14 n/sq cm

Notes:

1. *Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019.*
2. *Is design dependent; SEU capability based on standard evaluation circuit.*
3. *Short pulse 20ns FWHM (full width, half maximum).*
4. *Calculated for Adams 90% worse case GEO environment.*

35 YEARS AND MOVING FORWARD

Cobham Semiconductor Solutions (formerly Aeroflex) has a 35-year history of cost effective RadHard Digital ASIC solutions for the most critical applications. To meet the new demands of the digital world, Cobham offers proven RadHard Mixed-Signal ASIC capabilities, expanding our products to a full range of custom solutions - from FPGA conversions to complete Mixed-Signal system-level solutions, from 5V 0.6µm CMOS to deep submicron commercial technologies.

Cobham RadHard Digital ASICs have flown on Cassini, EOS, Iridium, Milstar, P-91, the International Space Station, and many classified satellites. Cobham's commercial Mixed-Signal ASICs are currently installed in medical, security, and industrial applications. With Cobham's custom RadHard Mixed-Signal solutions, system designers do not need to settle for more costly and power-hungry hybrids or MCM-based solutions.

By leveraging our high-volume commercial RadHard product knowledge, our Cobham Gaisler portfolio, our proprietary advanced RadHard techniques, and the strength of our foundry partners, Cobham has the experience, technology, and motivation to assure your program success from cradle to grave.

FPGA-TO-RADHARD ASIC CONVERSIONS

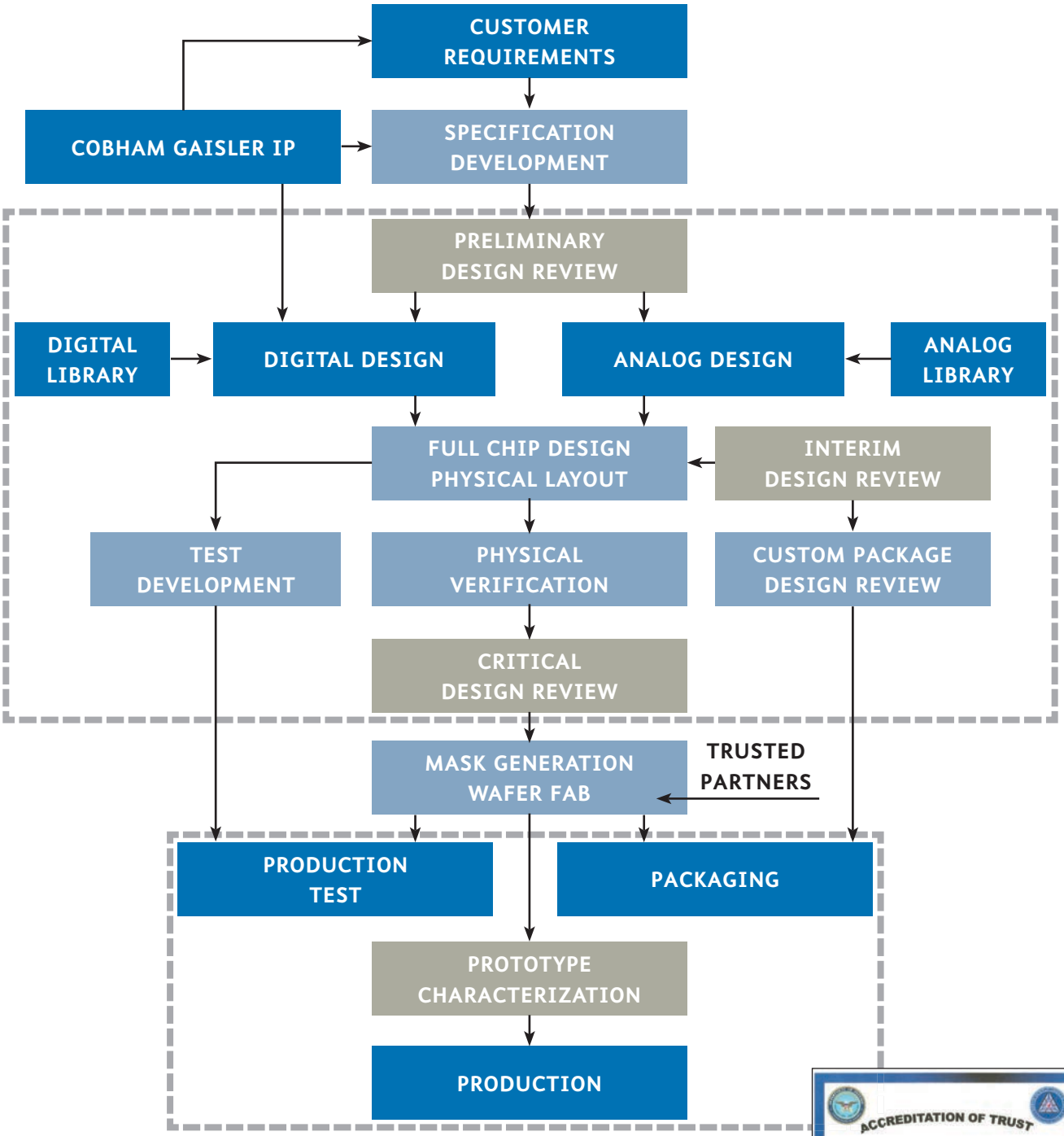
Cobham has proven experience in converting FPGAs into RadHard ASICs. For improvements in power, performance, reliability and radiation tolerance, Cobham has converted many FPGAs to RadHard ASICs. Examples include Microsemi RH1020, RH1280, RT54SX32S/72S, RTAX250S/1000S/2000S, Xilinx XC2/3/4000/4000S, and Virtex–II-II-Pro/-4/-5/-5QV/-7.

We offer these benefits.

- CML/SSTL/LVDS/PLL capability
- Chip capacitors on packages
- SEU of <2E-12 error/bit-day
- SEL of >128MeV on 0.6µm process*
- SEL of >110MeV on 0.25µm process*
- Actel compatible 84, 172, 208, 256, 352 CQFPs, 624 CCGA
- Xilinx compatible CQFP, Flip Chip, CCGA, PBGA, 1752FC/CGA
- Class Y, Cobham Class Y Facility Certification

* *maximum rate possible with test equipment @ 125˚C*

RadHard ASIC Design Flow



SUPPORTED DESIGN TOOLS

Cobham actively supports robust and easy-to-use design environments including VHDL and Verilog, using third-party design tools. Cobham supports libraries for:

- Cadence
- Synopsys
- Mentor Graphics
- Full mixed-mode simulation
- Topographical synthesis
- Floor-planned Place & Route
- Mixed-Mode Physical Design Integration
- SETsim
- Qsim
- MATLAB
- many others

Aeroflex's Trusted CAT1A capabilities for customers requiring "Trusted" services

Cobham Process Technology

TECHNOLOGY PARAMETERS	Deep Submicron	90nm CMOS	130nm CMOS
Metal layers	7-10 Cu	6-9 Cu	6-8 Al/Cu
Capacitors	MiM	MiM	MiM
High-value resistors	Yes (poly)	No	Yes
Vertical NPN bipolar	Yes	No	No
Substrate PNP bipolar	Yes	Yes	Yes
HV CMOS support	No	No	No
Thick metal inductor	Yes	No	Yes
Digital/analog supply voltages (DVdd, AVdd; Vss=0)	0.9-3.3V	2.5, 1.8, 1.2, 1.0	3.3, 2.5, 1.8, 1.5, 1.2
Alternate analog supply voltages (AVdd/AVss)			
Maximum toggle frequency	50GHz - 80GHz	33GHz	1.5GHz
Power dissipation - nW/gate - MHz; 20% duty cycle	0.6-2@0.9V	7@1.0V	18@1.2V
Gate delay 25°C (ps)	10	6	50@1.2V
Usable gates (NAND2 equivalent)	50-500M	15-50M	10-15M
Typical signal I/O	~2000	~1024	~1024
Flip-chip I/O available	Yes	Yes	Yes
Cold sparing	Yes	No	No
I/O tolerance	3.3V	2.5V	3.3V
Process Dependent Rich Portfolio (full custom analog available)	PLL, SerDes (6.25 Gbps)	PLL, SerDes (3.125 Gbps), Temp Sensor	ADCs, DACs, PLL, Voltage Regulator
SRAM compiled	Yes	Yes	Yes
Non-volatile memory	OTP Bit Cell		
Special I/O	PLL (1.2 GHz) HSSL (6.25 Gbps) SerDes (6.25 Gbps)	SSTL, MGT, CML, LVDS, PCI, PLL, SerDes	SSTL, MGT, CML, LVDS, PCI, PLL, Serdes
Total ionizing dose Rads (Si)	100-300K	100-300K	100-300K
SEL (MeV-cm^2/mg) @ Vdd max and 125°C	>60	>100	>110
Reliability (FIT rate)		<50	<20
Wafer foundry quality level	ESCC2269000	QML-Q, V, Y	QML-Q/Q+
Trusted foundry level		CAT1A	

* *Limited total-ionizing dose environments. Floating Gate Memories such as Flash and EEPROM must be periodically re-written in a total ionizing dose environment for reliability.*

TECHNOLOGY PARAMETERS	180nm CMOS	0.25µm CMOS	0.35µm CMOS	0.6µm CMOS
Metal layers	5-6 Al/Cu	4-5 Al/Cu	3-4 Al/Cu	3 Al/Cu
Capacitors	MiM	MiM	MiM/PiP	PiP
High-value resistors	Yes	Yes	Yes	Yes
Vertical NPN bipolar	Yes	Yes	Yes	Yes
Substrate PNP bipolar	Yes	Yes	Yes	Yes
HV CMOS support	5V (self-aligned)	Yes	10V (self-aligned)	20V (ext drain)
Thick metal inductor	Yes	No	Yes	No
Digital/analog supply voltages (DVdd, AVdd; Vss=0)	5.0, 3.3, 1.8	3.3, 2.5	10.0, 5.0, 3.3	5.0, 3.3
Alternate analog supply voltages (AVdd/AVss)	±2.5, ±1.65, ±0.9		±5, ±2.5, ±1.65	
Maximum toggle frequency	2.4GHz	1.2GHz	375MHz	150MHz
Power dissipation - nW/gate - MHz; 20% duty cycle	20@1.8V	40@2.5V 60@3.3V	150@2.5V	1100@5V 400@3.3V
Gate delay 25˚C (ps)	50	160@2.5V	140	225@5.5V
Usable gates (NAND2 equivalent)	8M	3M	1.5M	500K
Typical signal I/O	~1024	~530	~425	~500
Flip-chip I/O available	Yes	No	No	No
Cold sparing	Yes	Yes	Yes	Yes
I/O tolerance	5V	5V	10V	5V
Process Dependent Rich Portfolio (full custom analog available)	Band-gap, Voltage Regulator Comp/op-amps, ADCs, DACs, PLL, VCO RC oscillator	Band-gap, Voltage Regulator ADCs, DACs, PLL	Band-gap, Voltage Regulator Comp/op-amps, DACs, ADCs, PLL, VCO	Band-gap, Voltage Regulator Comp/op-amps, PLL/DLL
SRAM compiled	Yes	No	No	No
Non-volatile memory	Flash * EEPROM * RadHard OTP Metal Fuse		Flash * EEPROM * RadHard OTP Metal Fuse	
Special I/O	SSTL, MGT, CML, LVDS, PCI, USB1.1	SSTL, MGT, CML, LVDS, PCI	SSTL, MGT, CML, LVDS, PCI, RS232/RS485 (±5V), USB1.1	SSTL, MGT, CML, LVDS, PCI
Total ionizing dose Rads (Si)	100-300K	100K-1Meg	100-300K	100-300K
SEL (MeV-cm^2/mg) @ Vdd max and 125˚C	>110	>110	>110	>128
Reliability (FIT rate)	<10	<10	<10	<5
Wafer foundry quality level	QML-Q/Q+	QML-Q&V	QML-Q&V	QML-Q&V
Trusted foundry level				CAT1A

* *Limited total-ionizing dose environments. Floating Gate Memories such as Flash and EEPROM must be periodically re-written in a total ionizing dose environment for reliability.*

Application Specific Integrated Circuit (ASIC)

Deep Submicron Process

Product Brief

Cobham.com/HiRel

September 1, 2016

The most important thing we build is trust

FEATURES

- Wide ranging standard-cell libraries provide multiple options for optimizing performance or power
  - Mainstream libraries balance performance, power and area (PPA)
  - Low power libraries contain cells for clock gating, power gating and multiple power domains
  - High performance library cells enhance speed
- Standard-cell libraries offer both regular voltage threshold (RVT) and low voltage threshold (LVT) transistors
- Standard-cell libraries offer both high performance architectures and high density architectures for design optimization
- Standard-cell libraries offer poly-based cells to modulate the effective channel length of logic transistors to optimize performance or power
- Standard-cell libraries allow adaptive body biasing by applying a voltage under the ultra-thin buried oxide (BOX) to modify Vt for both LVT and RVT transistors
  - Forward Body Bias (FBB) lowers threshold voltage
  - Reverse Body Bias (RBB) raises threshold voltage
- Silicon proven IP: PLL, Process Dependent
- RadHard SRAM compiler
- Package Options: UT7152FC flip-chip LGA

OPERATIONAL ENVIRONMENT

- Temperature Range: -55°C to +125°C
- Total Dose: 300 krad(Si)
- SEL Immune: <60 MeV-cm^2/mg

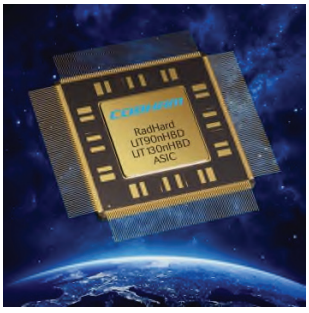
APPLICATIONS

- System on Chip (SoC) ASICs
- Wireless
- Set top boxes

INTRODUCTION

Through Cobham's state-of-the-art IC design partners, we are proud to offer deep submicron IC designs. Cobham works with our design partners to assure designs are completed to our rigorous standards of radiation designed architecture and QML quality levels. Our design partners bring their experience in deep submicron technologies to assure the highest probability of first-pass design success.

Because of this partnership solution, Cobham can select the specific deep submicron process that meets your unique needs, whether it is security, radiation hardness or product quality driving your application requirements.



Application Specific Integrated Circuit (ASIC)

UT1752FC FPGA-to-ASIC

Product Brief

Cobham.com/HiRel

September 1, 2016

The most important thing we build is trust

FEATURES

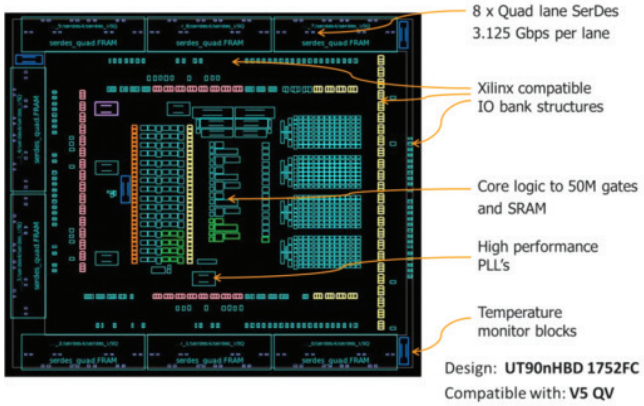
- Cobham UT90nHBD ASIC offering
- RHBD multi-Vt cell and IO library
- Compatible with Virtex-5QV 1752LGA CN/CF package
- Multiple pre-defined die frames and package substrates supporting up to 50 million equivalent 2-nand gates
- With AlSiC heat sink, Theta JC <0.15 C°/W
- Support for MIL-STD-123 screened 0402 decoupling capacitors
- Support for solder columns
- Proven development methodology using existing QML ceramic
- Daisy chain package available for board development
- SEU / Soft Error Immune 3.125Gbps SERDES IP, pin for pin, protocol compatible with Virtex-5QV, up to 32 SERDES RX/TX lanes
- Commercial and SEE hardened memory compilers

OPERATIONAL ENVIRONMENT

- Temperature Range: -55°C to +125°C
- Total Ionizing Dose: 100 krad(Si)
- SEL Immune: <110MeV-cm^2/mg
- SET Rate: 5.3x10^{-3} events/device-day

APPLICATIONS

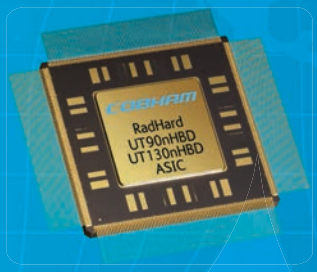
- QML-Y FPGA to ASIC conversions
- QML-Y System on Chip (SoC) ASICs
- Commercial and Military Space products



INTRODUCTION

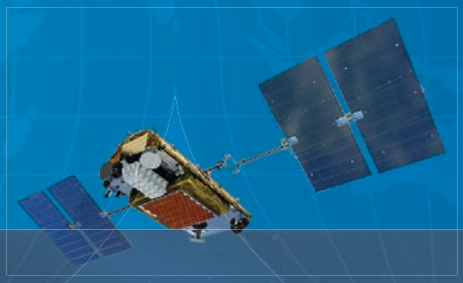
FPGA's allow for fast prototype time, but are expensive flight parts that have degraded speed performance over an ASIC solution. Cobham's ASIC solution allows you to port your FPGA design into an ASIC in record time using our pin-compatible package and FPGA conversion framework. Our ASIC's offer cost savings over your current FPGA, contain up to 5x the functionality of a single Virtex-5QV, with enhanced speed performance.

The UT1752FC FPGA-to-ASIC product provides a path to create a Virtex-5QV FPGA pin-for-pin and functionally equivalent QML Class-Y 90nm ASIC. The UT1752FC FPGA-to-ASIC product consists of five elements:
- Pre-defined set of Cobham UT90nHBD ASIC die frames with existing ceramic 1752 LGA substrates
- QML certified UT90nHBD ASIC development methodology
- QML Class Y certified flip-chip assembly flow with support for AlSiC heat sink, MIL-PRF-123 0402 capacitors, and solder column attach
- Pre-defined production test and burn-in hardware
- 1752 LGA daisy chain package with solder column option



RadHard ASICs

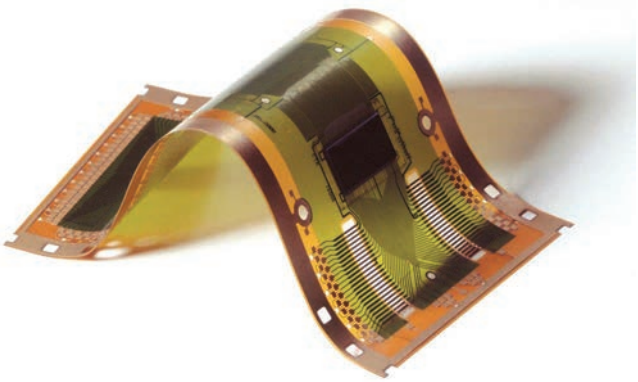
Digital and Mixed-Signal



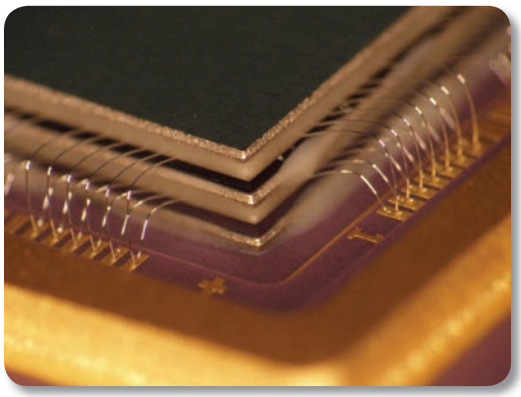
PACKAGING

TYPE	LEADS/DESCRIPTION
CQFP	68, 84, 132, 172, 196, 208, 256, 304, 340, 352
CPGA	281, 299
CLGA / CCGA	472, 624, 729, 1028, 1752
Chip-on-Flex	100µ lead pitch
Plug & Sense™	Sensor and read-out ASIC in same package
Flip Chip	729, 1752 LGA / CGA
Class Y*	1752 LGA / CGA

**Cobham Class Y Certified Facility*



Cobham also offers custom packages including multi-chip modules, end modules, and all JEDEC packages.



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