Standard Products

UT69151 SμMMIT™ RTE

Product Handbook
January 2013
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FEATURES

- Comprehensive MIL-STD-1553 dual redundant Remote Terminal (RT) with integrated bus transceivers, Memory, and Memory Management Unit (MMU)
- MIL-STD-1553B, Notice II RT
  - Internal command illegalization
  - 16-bit read/write time-tag with user-defined resolution
  - Subaddress data buffering
- Programmable interrupt architecture with automatic interrupt logging available
- Autonomous operation
  - External initialization bus
  - Ideal for low cost remote terminals
- Internal Memory Management Unit (MMU) interfaces host subsystem to 64Kbit SRAM
  - Wait state and zero-wait state configurations
- Built-In Test capability
- Supports IEEE Standard 1149.1 (JTAG)
- Flexible power supply configurations
  - +5-volt only operation
- Flexible packaging offering:
  - 139-pin pingrid array (PGA)
  - 140-lead flatpack
  - 132-lead flatpack
- Standard Microcircuit Drawing 5962-98587

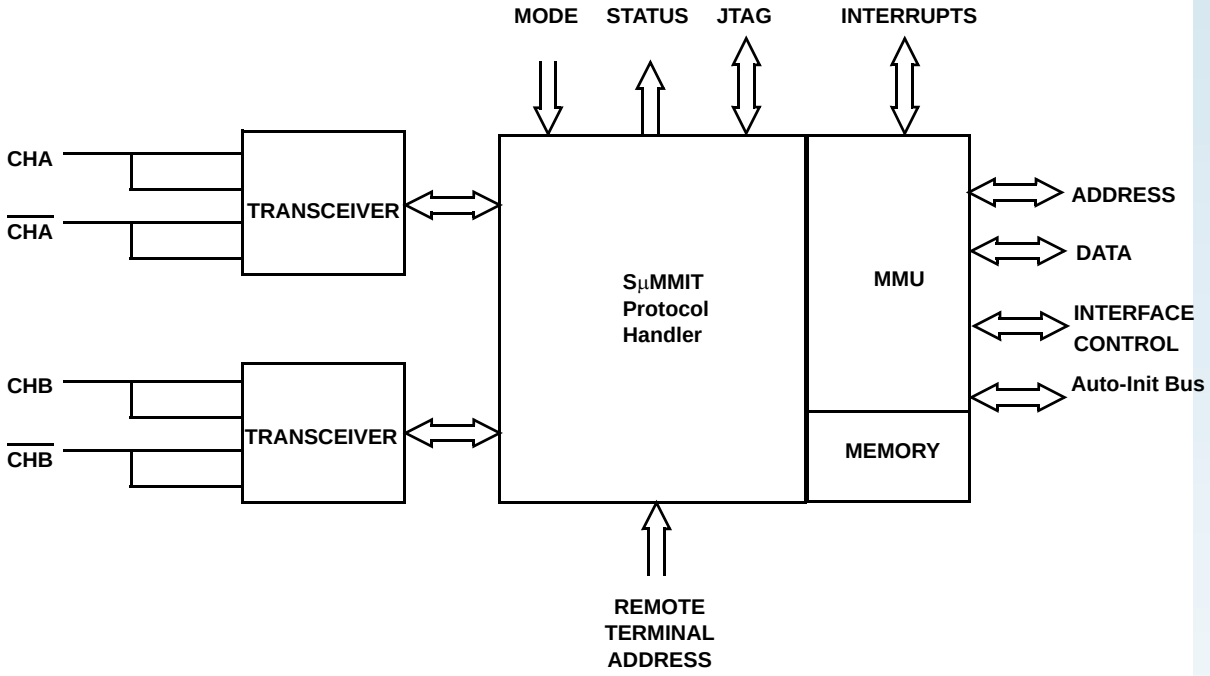

Figure 1. UT69151 SμMMIT RTE Block Diagram

2.0 REMOTE TERMINAL ARCHITECTURE

The SμMMIT Remote Terminal (RTE) is an interface device linking a MIL-STD-1553 serial data bus to a host microprocessor and/or subsystem. The SμMMIT RTE's MIL-STD-1553 interface includes encoding/decoding logic, error detection, command recognition, DMA interface, control/ configuration registers, clock, and reset logic. The following sections review the architecture and use. Each section supplies information on the SμMMIT RTE's configuration and operation.

2.1 Register Descriptions

The following list provides the bit descriptions of the 32 internal registers that control SμMMIT RTE operation. All register bits are active high and reflect a logic zero condition (0000 hex) after Master Reset (except those reflecting input pins).

Register Number	Name	Register Address
0	Control Register	0000 (hex)
1	Operational Status Register	0001 (hex)
2	Current Command Register	0002 (hex)
3	Interrupt Mask Register	0003 (hex)
4	Pending Interrupt Register	0004 (hex)
5	Interrupt Log List Pointer Register	0005 (hex)
6	BIT Word Register	0006 (hex)
7	Time-Tag Register	0007 (hex)
8	RT Descriptor Pointer Register	0008 (hex)
9	1553 Status Word Bits Register	0009 (hex)
10-15	Not Applicable	000A to 000F (hex)
16-31	Illegalization Registers	0010 to 001F (hex)

Note: Reference section 7.1, Table 12 for SμMMIT RTE 8-bit register address numbers.

2.1.1 Control Register (Read/Write) - Register 0

This 16-bit register controls SμMMIT RTE configuration. To make changes to the SμMMIT RTE and this register, the STEX bit (Bit 15 of the Control Register) must be logic zero. Note: The user has 5μs after $\overline{\text{TERACT}}$ active to stop execution.

Bit Number	Mnemonic	Description
15	STEX	Start Execution. Assertion of this bit initiates SμMMIT RTE operation. A Control Register write negating this bit inhibits SμMMIT RTE operation. A remote terminal address parity error prevents SμMMIT RTE operation regardless of the logical state of this bit. If a RT address parity error exists, bit 3 of Register 1 will be set low and bit 2 of Register 1 will be set high.
14	SBIT	Start BIT. Assertion of this bit places the SμMMIT RTE into the Built-In Test routine. The BIT test has a fault coverage of 93.4%. If the SμMMIT RTE has been started, the host must halt the device in order to place the SμMMIT RTE into the Built-In Test routine (STEX = 0) (see section 6.0 for additional information). Note: If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.

Bit Number	Mnemonic	Description
13	SRST	Software Reset. Assertion of this bit immediately places the SμMMIT RTE into a software reset. The software reset (which takes 5μs to execute), like $\overline{\text{MRST}}$, clears all internal logic. Note: During auto-initialization this bit should not be loaded with a logic one. SRST will only function after $\overline{\text{READY}}$ is asserted.
12	CHAEN	Channel A Enable. Setting this bit enables Channel A operation. If negated, the SμMMIT RTE does not recognize commands received over Channel A.
11	CHBEN	Channel B Enable. Setting this bit enables Channel B operation. If negated, the SμMMIT RTE does not recognize commands received over Channel B.
10	ETCE	External Timer Clock Enable. Assertion of this bit to a logic one allows the external timer clock input to supply stimulus to the internal time-tag counter. Refer to section 2.1.8 for additional information. Note: The user can only change the clock frequency before starting the device (i.e., setting bit 15 of Register 0 to a logic one).
9	PPACK	Ping-pong acknowledge made. See section 3, Circular Buffer and Ping-Pong Operation for additional information.
8	CBSEL1	Circular buffer mode select. See section 3, Circular Buffer and Ping-Pong Operation for additional information.
7	CBSEL2	Circular buffer mode select. See section 3, Circular Buffer and Ping-Pong Operation for additional information.
6	N/A	Always set this bit to logical zero.
5	N/A	Always set this bit to logical zero.
4	BCEN	Broadcast Enable. Assertion of this bit enables the SμMMIT RTE broadcast option. Negation of this bit enables remote terminal address 31 as a unique remote terminal address.
3	DYNBC	Dynamic Bus Control Acceptance. This bit controls the SμMMIT RTE's ability to accept the dynamic bus control mode code. Assertion of this bit allows the SμMMIT RTE to respond to a dynamic bus control mode code with status word bit 18 set to a logic one. Negation of this bit prevents the assertion of status word bit 18 upon reception of the dynamic mode code.
2	PPEN	Ping-Pong Enable. Assertion of this bit enables the ping-pong buffer feature of the SμMMIT RTE and disables the message indexing feature. Negation of this bit disables the ping-pong feature and enables the message indexing feature. See section 3, Circular Buffer and Ping-Pong Operation for additional information.
1	INTEN	Interrupt Log Enable. Assertion of this bit enables the SμMMIT interrupt logging feature. Negation of this bit prevents the logging of interrupts.
0	XMTSW	Transmit Status Word. Assertion of this bit allows the SμMMIT RTE to automatically execute the TRANSMIT STATUS WORD mode code when configured for MIL-STD-1553A mode operation. Refer to section 2.9 for additional information.

2.1.2 Operational Status Register (Read/Write) - Register 1

This register reflects pertinent status information for the SμMMIT RTE and is not reset to 0000 (hex) on $\overline{\text{MRST}}$. Instead, the register reflects the actual stimulus applied to input pins RTA(4:0), RTPTY, A/$\overline{\text{B}}$ STD, and $\overline{\text{LOCK}}$. Assertion of the $\overline{\text{LOCK}}$ input prevents the modification of the remote terminal address, mode selects, and A or B Standard. In this case, a write to this register's most significant nine bits is meaningless. If $\overline{\text{LOCK}}$ is negated, a read of this register reflects the information written into this register's most significant nine bits.

Note: To make changes to the SμMMIT RTE and this register, the STEX bit (Bit 15 in Register 0) must be logic zero**.**

Bit Number	**Mnemonic**	**Description**
15	RTA4	Terminal Address Bit 4. This bit is the most significant bit of the remote terminal address. This bit is latched on the rising edge of $\overline{\text{MRST}}$ and is a read only bit if the $\overline{\text{LOCK}}$ pin is active.
14	RTA3	Terminal Address Bit 3. This bit is Bit 3 of the remote terminal address. This bit is latched on the rising edge of $\overline{\text{MRST}}$ and is a read only bit if the $\overline{\text{LOCK}}$ pin is active.
13	RTA2	Terminal Address Bit 2. This bit is Bit 2 of the remote terminal address. This bit is latched on the rising edge of $\overline{\text{MRST}}$ and is a read only bit if the $\overline{\text{LOCK}}$ pin is active.
12	RTA1	Terminal Address Bit 1. This bit is Bit 1 of the remote terminal address. This bit is latched on the rising edge of $\overline{\text{MRST}}$ and is a read only bit if the $\overline{\text{LOCK}}$ pin is active.
11	RTA0	Terminal Address Bit 0. This bit is the least significant bit of the remote terminal address. This bit is latched on the rising edge of $\overline{\text{MRST}}$ and is a read only bit if the $\overline{\text{LOCK}}$ pin is active.
10	RTPTY	Terminal Address Parity Bit. This bit is appended to the remote terminal address bus (RTA(4:0)) to supply odd parity. The SμMMIT RTE requires odd parity for proper operation. This bit is latched on the rising edge of $\overline{\text{MRST}}$ and is a read only bit if the $\overline{\text{LOCK}}$ pin is active.
9	N/A	Always set this bit to logical zero.
8	Logical one	Always set this bit to logical one.
7	A/$\overline{\text{B}}$ STD	Military Standard 1553A or 1553B Standard. This bit determines whether the SμMMIT RTE will be set to operate under MIL-STD-1553A or B. Assertion of this bit enables the XMTSW bit (Bit 0 of the Control Register). Negation of this bit automatically allows the SμMMIT RTE to operate under the MIL-STD-1553B protocol. This bit is latched on the rising edge of $\overline{\text{MRST}}$ and is a read only bit if the $\overline{\text{LOCK}}$ pin is active. See section 2.9 for further definition.
6	LOCK	$\overline{\text{LOCK}}$ Pin. This read-only bit reflects the inverted state of input pin $\overline{\text{LOCK}}$ and is latched on the rising edge of $\overline{\text{MRST}}$.
5	AUTOEN	$\overline{\text{AUTOEN}}$ Pin. This read-only bit reflects the inverted state of input pin $\overline{\text{AUTOEN}}$. Assertion of this input enables SμMMIT RTE auto-initialization.
4	SSYSF	$\overline{\text{SSYSF}}$ Pin. This read-only bit reflects the inverted state of the input pin $\overline{\text{SSYSF}}$.
3	EX	SμMMIT RTE Executing. This read-only bit indicates whether the SμMMIT RTE is presently executing or whether it is idle. A logic one indicates that the SμMMIT RTE is executing; logic zero indicates that the SμMMIT RTE is idle.
2	TAPF	Terminal Address Parity Fail. This bit indicates the observance of a terminal address parity error. The SμMMIT RTE checks for odd parity. This read only bit reflects the parity of Operational Status Register bits 15-10, and is latched on the rising edge of $\overline{\text{MRST}}$.

Bit Number	Mnemonic	Description
1	READY	$\overline{\text{READY}}$ Pin. This read-only bit reflects the inverted state of the output pin $\overline{\text{READY}}$ and is cleared on reset.
0	TERACT	$\overline{\text{TERACT}}$ Pin. Assertion of this bit indicates that the SμMMIT RTE is presently processing a message. This read only bit reflects the inverted state of output pin $\overline{\text{TERACT}}$ and is cleared on reset.

Note: Remote Terminal Address and Parity checked on start of execution.

2.1.3 Current Command Register (Read-only) - Register 2

This 16-bit register contains the last valid command processed by the SμMMIT RTE.

Bit Number	Mnemonic	Description
15 to 0	CC15-CC0	Current Command Bits. This register contains the last valid command received by the SμMMIT RTE. This register is valid 13μs after $\overline{\text{TERACT}}$ is negated. (Bit 15 MSB - Bit 0 LSB).

2.1.4 Interrupt Mask Register (Read/Write) - Register 3

The SμMMIT RTE interrupt architecture allows for the masking of all interrupts. An interrupt is masked if the corresponding bit of this register is set to logic zero. This feature allows the host or subsystem to temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event.

Bit Number	**Mnemonic**	**Description**
15	MAB	Memory Access Blocked Interrupt
14	WRAPF	Wrap Fail Interrupt
13	TAPF	Terminal Address Parity Fail Interrupt
12	BITF	BIT Fail Interrupt
11	MERR	Message Error Interrupt
10	SUBAD	Subaddress Accessed Interrupt
9	BDRCV	Broadcast Command Received Interrupt
8	IXEQ0	Index Equal Zero Interrupt
7	ILLCMD	Illegal Command Interrupt
6-0	N/A	Not Applicable

2.1.5 Pending Interrupt Register (Read-only) - Register 4

The Pending Interrupt Register contains information that identifies events that generate interrupts. The assertion of any bit in this register asserts an output pin, $\overline{\text{MSG\_INT}}$ or $\overline{\text{YF\_INT}}$ (three clock cycles). Writing to the most significant 4 bits of this register generates a $\overline{\text{YF\_INT}}$.

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Bit Number	Mnemonic	Description
15	MAB	Memory Access Blocked. Once the SμMMIT RTE begins internal DMA activity, an internal timer starts. If all internal DMA activity is not completed by the time the counter decrements to zero, the interrupt is generated. In the SμMMIT RTE mode, the $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked), current command processing ends, and the SμMMIT RTE will remain on-line. Current cycle terminated, bus released.
14	WRAPF	Wrap Fail Interrupt. The RTE automatically compares the transmitted word (encoder word) to the reflected decoder word via the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is asserted in the BIT Word Register and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked). The loop-back path is via the MIL-STD-1553 bus transceiver.
13	TAPF	Terminal Address Parity Fail Interrupt. This bit reflects the outcome of the remote terminal address parity check. A logic one indicates a parity failure. When a parity error occurs, the SμMMIT RTE does not begin operation (STEX bit forced to logic zero), channel A and B do not enable, the TAPF bit is asserted here and in the BIT Word Register, and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked).
12	BITF	BIT Fail Interrupt. Assertion of this bit indicates a BIT failure. Status word bit 19 is automatically set to a logic one when a BIT failure occurs. If a BIT fails, the BITF bit is asserted here and in the BIT Word Register, and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked). Operation continues.
11	MERR	Message Error Interrupt. Assertion of this bit indicates that a message error condition exists. The SμMMIT RTE can detect Manchester errors, sync-field, word count errors (too many or too few), MIL-STD-1553 word parity errors, bit count errors (too many or too few), and protocol errors. If not masked, this bit is always set when the SμMMIT RTE asserts bit 9 of the status word (e.g., illegal commands, invalid data word, etc.). $\overline{\text{MSG\_INT}}$ interrupt generated (if not masked).
10	SUBAD	Subaddress Accessed Interrupt. Assertion of this bit indicates a pre-selected subaddress has transacted a message. To determine the exact subaddress, the host interrogates the interrupt log IAW. $\overline{\text{MSG\_INT}}$ interrupt generated (if not masked).
9	BDRCV	Broadcast Command Received Interrupt. This bit is set to a logic one to indicate the SμMMIT RTE's receipt of a valid broadcast command. The SμMMIT RTE suppresses status word transmission. $\overline{\text{MSG\_INT}}$ interrupt generated (if not masked).
8	IXEQ0	Index Equal Zero Interrupt. The SμMMIT RTE asserts this bit to indicate the completion of a pre-defined number of commands by the SμMMIT RTE. Upon assertion of this interrupt, the host or subsystem updates the subaddress descriptor to prevent the potential loss of data. $\overline{\text{MSG\_INT}}$ interrupt generated (if not masked).
7	ILLCMD	Illegal Command Interrupt. This bit is set to a logic one to indicate the reception of an illegal command by the SμMMIT RTE. Upon receipt of this command, the SμMMIT RTE responds with a status word only; Bit 9 of the status word is set to a logic one. $\overline{\text{MSG\_INT}}$ interrupt generated (if not masked).
6-0	N/A	Always set these bits to logical zero.

2.1.6 Interrupt Log List Pointer Register (Read/Write) - Register 5

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32 word ring-buffer that contains information pertinent to the service of interrupts. The SμMMIT RTE architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 4 bits of this register should be initialized to logical zero. The 7 bits ranging from bit 11 to bit 5 designate the location of the Interrupt Log List within a 4K memory space. The lower 5 bits of this register should be initialized to a logic zero. The SμMMIT RTE controls the lower 5 bits to implement the ring-buffer architecture. The host or subsystem reads this register to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Note: Bits 15-12 are not used. Bits 11-5 indicate the starting base address of the Interrupt Log List, and bits 4-0 indicate the ring location of the Interrupt Log List. See section 4.0 for a description of the Interrupt Architecture.

Bit Number	Mnemonic	Description
15-12	N/A	Always set these bits to logical zero.
11-5	INTA(11:5)	Interrupt Log List Pointer Base Address Bits. (Bit 11 MSB - Bit 5 LSB).
4-0	INTA(4:0)	Always set these bits to logical zero.

2.1.7 BIT Word Register (Read/Write) - Register 6

This register contains information on the SμMMIT RTE's current health. The SμMMIT RTE transmits the contents of this register upon reception of a Transmit Bit Word Mode Code. The lower 8 bits of this register are user-defined.

Bit Number	Mnemonic	Description
15	MAB	Memory Access Blocked. This bit is set if all internal DMA activity is not completed between the time internal DMA activity begins and when the timer decrements to zero. In the event of a DMA failure, current message processing terminates; remote terminal waits for next 1553 message.
14	WRAPF	Wrap Fail. The SμMMIT RTE automatically compares the transmitted word (encoder word) to the reflected decoder word via the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit asserts and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked). The loop-back path is via the MIL-STD-1553 bus transceiver. A wrap failure does not result in the terminal flag bit being set to a logical one. Message processing continues.
13	TAPF	Terminal Address Parity Fail. This bit reflects the outcome of the remote terminal address parity check. A logic one indicates a parity failure. When a parity error occurs theSμMMIT RTE does not begin operation (STEX bit forced to a logic zero), channel A and B do not enable, and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked).
12	BITF	BIT Fail. Assertion of this bit indicates a BIT failure. Bits 11 through 8 should be interrogated to determine the specific failure. Status word bit 19 is automatically set to a logic one when a BIT failure occurs. If a BIT fails, the BITF bit is asserted, and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked). Operation continues.
11	CHAF	Channel A Fail. Assertion of this bit indicates a BIT test failure in Channel A.
10	CHBF	Channel B Fail. Assertion of this bit indicates a BIT test failure in Channel B.
9	N/A	Always set this bit to logical zero.
8	MTF	Memory Test Fail.
7-0	UDB(7:0)	User-Defined Bits.

2.1.8 Time-Tag Register (Read/Write) - Register 7

The Time-Tag Register reflects the state of a 16-bit free running counter. The resolution of this counter is user-defined via input TCLK (0 to 4MHz) or fixed at 64µs/bit. The Time-Tag counter is automatically reset when the SµMMIT RTE receives a valid synchronize without data mode code. The SµMMIT RTE automatically loads the Time-Tag counter with the data associated with reception of a valid synchronize with data mode code. The Time-Tag counter begins operation on the rising edge of $\overline{\text{MRST}}$ or within 64µs; after the receipt of a valid mode code, reset remote terminal, or sync with/without data. When the SµMMIT RTE is halted (STEX = 0), the Time-Tag continues to run.Time-Tag value is captured upon command word-validation.

Bit Number	Mnemonic	Description
15-0	TT(15:0)	Time-Tag Counter Bits. (Bit 15 MSB - Bit 0 LSB)

2.1.9 Remote Terminal Descriptor Pointer Register (Read/Write) - Register 8

The SµMMIT RTE accesses a block of external memory to gain information on how to process a valid command. Each subaddress and mode code has a block of memory reserved for this task. Located contiguously in memory, these reserved memory locations are called a descriptor space. The Remote Terminal Descriptor Pointer Register contains an address that points to the top of this memory space. The SµMMIT RTE uses the T/$\overline{\text{R}}$ bit, subaddress/mode code field, and mode code to select one block within the descriptor table for message processing. The Remote Terminal Descriptor Pointer Register is static during message processing.

Bit Number	Mnemonic	Description
15-12	N/A	Always set these bits to logical zero.
11-0	RTDA(11:0)	Remote Terminal Descriptor Address Bits. (Bit 11 MSB - Bit 0 LSB)

2.1.10 1553 Status Word Bits Register (Read/Write) - Register 9

The host or subsystem accesses this register to control the outgoing MIL-STD-1553 status word. The host or subsystem controls the Instrumentation, Busy, Terminal Flag, Service Request, and Subsystem Flag by writing to bits 9 through 0 of this register. The SμMMIT RTE's status word response reflects assertion of these bit(s) until negated by the host or subsystem unless the Immediate Clear Function is enabled. The Immediate Clear Function automatically clears these bits after being transmitted in a status word.

The Immediate Clear Function does not affect the operation of the Transmit Status word and Transmit Last Command word Mode Codes. Transaction of a legal valid command with the INS bit set to a logic one and the Immediate Clear Function enabled, results in the transmission of a status word with Bit 10 asserted. If the ensuing command is a Transmit Status word or Last Command mode code, Bit 10 of the outgoing status word remains a logic one. For MIL-STD-1553B applications, the register is as follows:

Bit Number	Mnemonic	Description
15	IMCLR	Immediate Clear Function. Assertion of this bit enables the Immediate Clear Function (IMF) of the SμMMIT RTE. Enabling the IMF results in the clearing of the INS, BUSY, TF, SRQ, and/or SUBF bit immediately after a message is completed. This function is enabled by asserting this bit when asserting bit(s) INS, BUSY, TF, SRQ, and/or SSYSF. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
14-10	N/A	Always set these bits to logical zero.
9	INS	Instrumentation Bit. This bit asserts the Instrumentation bit of the MIL-STD-1553B status word. (Bit time 10 of the Status Word).
8	SRQ	Service Request Bit. This bit asserts the Service Request bit of the MIL-STD-1553B status word. (Bit time 11of the Status Word).
7-4	N/A	Always set these bits to logical zero.
3	BUSY	Busy Bit. Assertion of this bit is reflected in the outgoing MIL-STD-1553B status word. Assertion of this bit prevents memory accesses. (Bit time 16 of the Status Word).
2	SSYSF	Subsystem Flag Bit. This bit asserts the Subsystem Flag bit of the MIL-STD-1553B status word and may also be set with the SSYSF input pin. (Bit time 17 of the Status Word).
1	N/A	Always set this bit to logical zero.
0	TF	Terminal Flag. Assertion of this bit is reflected in the outgoing MIL-STD-1553B status word. The SμMMIT RTE automatically asserts this bit if a BIT failure occurs. Inhibit Terminal Flag mode code prevents the assertion by the host or subsystem. Override Inhibit Terminal Flag Mode Code re-establishes the Terminal Flag option (Bit time 19 of the Status Word).

For MIL-STD-1553A applications, the register is as follows:

Bit Number	Mnemonic	Description
15	IMCLR	Immediate Clear Function. Assertion of this bit enables the Immediate Clear Function (IMF) of the SμMMIT RTE. Enabling the IMF results in the clearing of the bit times 10-19 immediately after a status word is transmitted. This function is enabled by asserting this bit when asserting bit times 10-19. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
14-10	N/A	Always set these bits to logical zero.
9	SB10	Status bit time 10.
8	SB11	Status bit time 11.
7	SB12	Status bit time 12.
6	SB13	Status bit time 13.
5	SB14	Status bit time 14.
4	SB15	Status bit time 15.
3	SB16	Status bit time 16.
2	SB17	Status bit time 17.
1	SB18	Status bit time 18.
0	SB19	Status bit time 19.

2.1.11 Illegalization Registers

The 16 registers are divided into 8 blocks, 2 registers per block (see table 1).

Table 1. Illegalization Register Blocks

Block Name	Address (hex)
Receive	0010 and 0011
Transmit	0012 and 0013
Broadcast Receive	0014 and 0015
Broadcast Transmit (Automatically Illegalized)	0016 and 0017
Mode Code Receive	0018 and 0019
Mode Code Transmit	001A and 001B
Broadcast Mode Code Receive	001C and 001D
Broadcast Mode Code Transmit	001E and 001F

The blocks correspond to the following types of commands. Register address 0010 (hex) and 0011 (hex) illegalize receive commands to 32 subaddresses. The most significant bit of register 0010 (hex) controls the illegalization of subaddress 01111. The least significant bit controls subaddress 00000. Register 0011 (hex) controls illegalization of subaddresses 10000 through 11111. The least significant bit relates to subaddress 10000; the most significant bit relates to subaddress 11111. Transmit commands and broadcast commands (both receive and transmit) use the same encoding scheme as receive subaddress illegalization.

Registers 18 (hex) through 1F (hex) control the illegalization of mode codes. Register 18 governs the illegalization of receive mode codes (T/$\overline{R}$ bit = 0) 00000 through 01111 and register 19 mode codes 10000 through 11111. Register blocks Transmit Mode Code (T/$\overline{R}$ bit = 1), Broadcast Receive Mode Codes, and Broadcast Transmit Mode Codes use the same decode scheme as receive mode codes.

Table 2 shows the illegalization register map. For each block, the numbers shown in the column under each bit number identifies the specific subaddress or mode code (in hex) that the register bit illegalizes (Logical 0 = legal, Logical 1 = illegal).

Table 2. Illegalization Register Map

Name	Register Number																
Bit Number		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Receive	16	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	17	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Transmit	18	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	19	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Brd Receive	20	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	21	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Brd Transmit	22	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
	23	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
Mode Receive	24	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	25	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Transmit	26	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	27	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Brd Receive	28	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	UU	01	WW
	29	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Brd Transmit	30	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	ZZ	01	XX
	31	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY

Notes:
1. Brd = Broadcast.
2. Mode = Mode code.
3. XX= Automatically illegalized by SμMMIT RTE.
4. YY= Automatically illegalized by SμMMIT RTE in 1553B only.
5. ZZ= Automatically illegalized by SμMMIT RTE in 1553B and 1553A if XMTSW is enabled.
6. WW = Automatically illegalized in 1553A.
7. UU = Automatically illegalized in 1553A if XMTSW enabled.

2.2 Descriptor Block

To process messages, the SμMMIT RTE uses data supplied in the internal registers with data stored in internal memory. The SμMMIT RTE accesses a four word descriptor block stored in internal memory. The descriptor block is accessed at the beginning and end of command processing. Multiple descriptor blocks are sequentially entered into memory to form a descriptor table. The following paragraphs discuss the descriptor block in detail.

The host or subsystem controlling the SμMMIT RTE allocates 512 consecutive memory spaces for the subaddress and mode code descriptor table. The top of the descriptor table can reside at any address location except locations 0-31. Defined and entered into memory by the host, the SμMMIT RTE is linked to the descriptor table via the Descriptor Address Register contents (see figures 2a and 2b). Each descriptor block contains a Control Word, Data Pointer A, Data Pointer B, and Broadcast Data Pointer. Each subaddress and mode code is assigned a descriptor for receive and transmit commands (T/$\overline{R}$ bit equal zero or one).

Control word information allows the SμMMIT RTE to generate interrupts, buffer messages, and control message processing. For a receive command, the Data Pointer is read to determine the top of the data buffer. The SμMMIT RTE stores data sequentially from the top of data buffer plus two locations (e.g., 0100, 0101, 0102, 0103, etc.). When processing a transmit command, the Data Pointer is read to determine where data words are retrieved. The SμMMIT RTE retrieves data words sequentially from the address the Data Pointer designates plus a two address location offset.

The Broadcast Data Pointer allows for separate storage of non-broadcast data from broadcast data per MIL-STD-1553B Notice II. The host or subsystem enables or disables this feature via the Control Word's least significant bit.

When disabled, the non-broadcast and broadcast data is stored via Data List Pointer A or B. For transmit commands, the Broadcast Data Pointer is not used. The SμMMIT RTE does not transmit any information on the receipt of a broadcast transmit command.

The SμMMIT RTE reads the descriptor block during command processing (i.e., after assertion of $\overline{\text{TERACT}}$). The SμMMIT RTE reads the control word and three Data Pointers. The SμMMIT RTE then begins the acquisition of data words for either transmission or storage.

After transmission or reception, the SμMMIT RTE begins post-processing. The SμMMIT RTE performs a DMA burst during post-processing. An optional interrupt log entry is performed after a descriptor update. During the descriptor update, the SμMMIT RTE modifies the Control Word index field and bits 4, 2, and 1, if required. The SμMMIT RTE updates Data Pointer A if no message errors occurred during the message transaction. Reception of a broadcast command, with no message errors, results in the update of the Broadcast Data Pointer. Neither Data Pointer A, B or Broadcast is updated if the SμMMIT RTE has the ping-pong mode of operation enabled.

See section 3, Circular Buffer and Ping-Pong Operation for additional information.

T/R	Subaddress/Mode Code Descriptors	Address Equation
0	Subaddress	Descriptor Address Register Contents + [(SA# x 4) + 0]
1	Subaddress	Descriptor Address Register Contents + [(SA# x 4) + 128]
0	Mode Codes	Descriptor Address Register Contents + [(MC# x 4) + 256]
1	Mode Codes	Descriptor Address Register Contents + [(MC# x 4) + 384]

Figure 2a. Descriptor Table

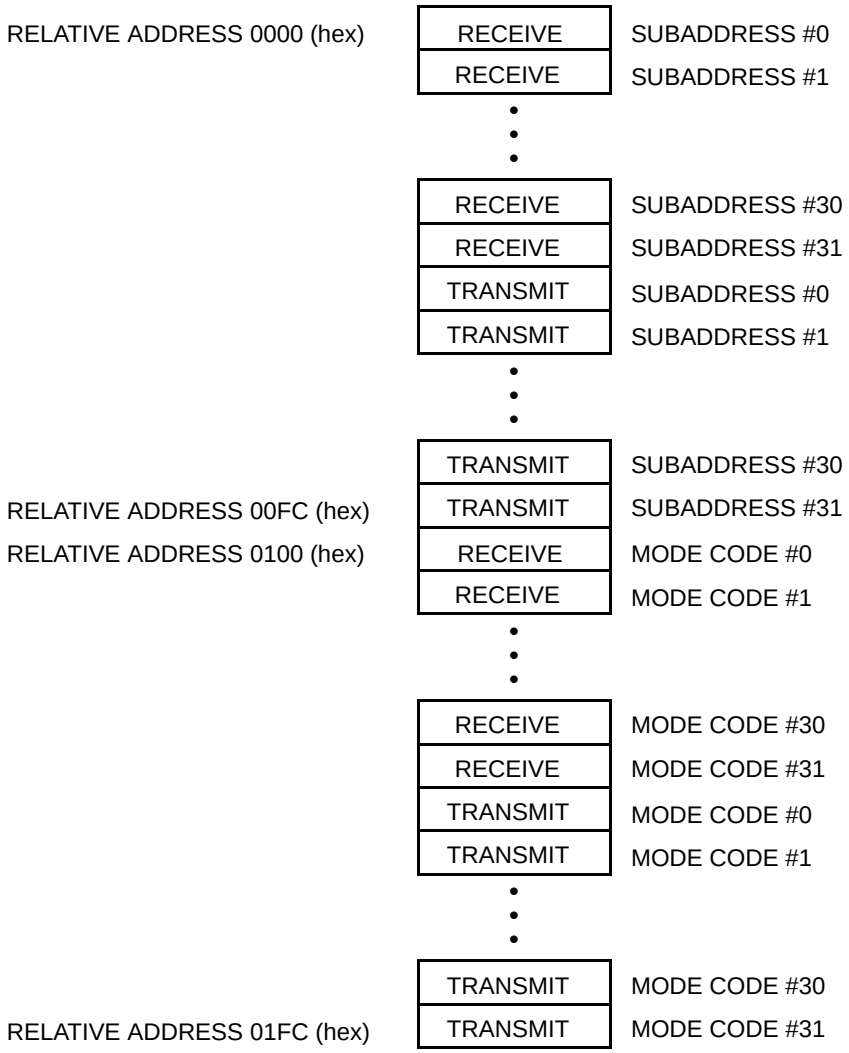


Figure 2b. Descriptor Table

2.2.1 Receive Control Word

The following bits describe the receive subaddress Descriptor Control Word. Information contained in this word assists the SμMMIT RTE in message processing. The Descriptor Control Word is initialized by the host or subsystem and updated by the SμMMIT RTE during command post-processing.

Bit Number	Mnemonic	Description
15-8	INDX	Index Field. These bits define multiple message buffer length. The host or subsystem uses this field to instruct the SμMMIT RTE to buffer "N" messages. "N" can range from 0 (00 hex) to 104 (68 hex). If buffer ping-ponging is enabled, the INDX field is "don't care" (i.e., does not contain applicable information). During ping-pong mode operation, initialize the index field to 00 (hex). TheSμMMIT RTE does not perform multiple message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the subaddress is illegalized. The SμMMIT RTE can generate an interrupt when the index field transitions from one to zero (see bit 7).
7	INTX	Interrupt Index Equals Zero. Assertion of this bit enables the generation of an interrupt when the index field transitions from one to zero. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{\text{MSG\_INT}}$ asserts after message processing.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when the subaddress receives a valid command; his includes illegal and broadcast commands. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{\text{MSG\_INT}}$ asserts after message processing.
5	IBRD	Interrupt Broadcast Received. Assertion of this bit enables the generation of an interrupt when the subaddress receives a valid broadcast command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{\text{MSG\_INT}}$ asserts after message processing.
4	BAC	Block Accessed. The subsystem or host initializes this bit to zero; the SμMMIT RTE overwrites the zero with a logic one upon completion of message processing. After interrogating this bit, the host resets this bit to zero to observe further accesses.
3	N/A	Always set this bit to logical zero.
2	A/$\overline{\text{B}}$	Buffer A/$\overline{\text{B}}$. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; a logic zero indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a valid broadcast command.
0	NII	Notice II. Assertion of this bit enables the use of the Broadcast Data Pointer as a buffer for broadcast command information. When negated, broadcast information is stored in the same buffer as non-broadcast information.

2.2.2 Transmit Control Word

The following bits describe the transmit subaddress Descriptor Control Word. Information contained in this word assists the SμMMIT RTE in message processing. The Descriptor Control Word is initialized by the host or subsystem and updated by the SμMMIT RTE during command post-processing.

Bit Number	**Mnemonic**	**Description**
15-7	N/A	Always set these bits to logical zero.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when the subaddress receives a valid command; his includes illegal and broadcast commands. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{\text{MSG\_INT}}$ asserts after message processing.
5	N/A	Always set this bit to logical zero.
4	BAC	Block Accessed. The subsystem or host initializes this bit to zero, the SμMMIT RTE overwrites the zero with a logic one upon completion of message processing. After interrogation, the host should reset this bit to zero to observe further accesses.
3	N/A	Always set this bit to logical zero.
2	A/$\overline{\text{B}}$	Buffer A/$\overline{\text{B}}$. Indicates the data pointer to access when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; a logic zero indicates buffer B. This bit is a “don’t care” if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a broadcast command.
0	N/A	Always set this bit to logical zero.

2.2.3 Mode Code Receive Control Word

The following bits describe the receive mode code Descriptor Control Word. Information contained in this word assists the SμMMIT RTE in message processing. The Descriptor Control Word is initialized by the host or subsystem and updated by the SμMMIT RTE during command post-processing.

Note: In MIL-STD-1553A, all mode codes are without data, and the T/$\overline{R}$ bit is ignored. See section 2.9 for the MIL-STD-1553A operation.

Bit Number	Mnemonic	Description
15-8	INDX	Index Field. These bits define message buffer length. The host or subsystem uses this field to instruct the SμMMIT RTE to buffer "N" messages. "N" can range from 0 (00 hex) to 104 (68 hex). If buffer ping-ponging is enabled, the INDX field is "don't care" (i.e., does not contain applicable information). The SμMMIT RTE does not perform message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the mode code is illegalized. The SμMMIT RTE can generate an interrupt when the index field transitions from one to zero (see bit 7).
7	INTX	Interrupt Index Equals Zero. Assertion of this bit enables the generation of an interrupt when the index field transitions from one to zero. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when mode code command is received; his includes illegal and broadcast commands. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
5	IBRD	Interrupt Broadcast Received. Assertion of this bit enables the generation of an interrupt when a valid broadcast mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
4	BAC	Block Accessed. The subsystem or host initializes this bit to zero; the SμMMIT RTE overwrites the zero with a logic one upon completion of message processing. After interrogating this bit, the host resets this bit to zero to observe further accesses.
3	N/A	Always set this bit to logical zero.
2	A/$\overline{B}$	Buffer A/$\overline{B}$. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; logic zero indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a valid broadcast command.
0	NII	Notice II. Asserting this bit enables the use of the Broadcast Data Pointer as a buffer for broadcast command information. When negated, broadcast information is stored in the same buffer as non-broadcast information.

2.2.4 Mode Code Transmit Control Word

The following bits describe the transmit mode code Descriptor Control Word. Information contained in this word assists the SμMMIT RTE in message processing. The Descriptor Control Word is initialized by the host or subsystem and updated by the SμMMIT RTE during command post-processing.

Note: In MIL-STD-1553A, all mode codes are without data, and the T/$\overline{R}$ bit is ignored. See section 2.9 for the MIL-STD-1553A operation.

Bit Number	Mnemonic	Description
15-7	N/A	Always set these bits to logical zero.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when mode code command is received; his includes illegal and broadcast commands. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
5	IBRD	Interrupt Broadcast Received. Assertion of this bit enables the generation of an interrupt when a valid broadcast mode code is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
4	BAC	Block Accessed. The subsystem or host initializes this bit to zero; the SμMMIT RTE overwrites the zero with a logic one upon completion of message processing. After interrogating this bit, the host resets this bit to zero to observe further accesses.
3	N/A	Always set this bit to logical zero.
2	A/$\overline{B}$	Buffer A/$\overline{B}$. This bit indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; a logic zero indicates buffer B. This bit is a “don’t care” if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a broadcast command.
0	N/A	Always set this bit to logical zero.

2.2.5 Data Pointer A and B

Data Pointer A and B contain address information for the retrieval and storage of message data words. In the index mode of operation, the SμMMIT RTE reads Data Pointer A to determine the location of data for retrieval or storage. The SμMMIT RTE uses the Data Pointer to initialize an internal counter; the counter increments after each data word. For a receive command, the SμMMIT RTE stores the incoming data word sequentially into memory. As part of command post-processing, the SμMMIT RTE writes a new data pointer into the descriptor block. The SμMMIT RTE continues to update the data pointer until the Control Word index field decrements to zero. An example is shown in figure 3.

Note: The index feature is not applicable for transmit commands (i.e., T/$\overline{R}$ bit = 1).

For ping-pong buffer operation, the host uses either Data Pointer A or Data Pointer B. The SμMMIT RTE determines which pointer to access via the state of Control Word bit 2. The SμMMIT RTE retrieves or stores data words from the address contained in the data pointer, automatically incrementing the data pointer as data words are received. The data pointer is never updated as part of command post-processing in the ping-pong mode of operation. See figures 3 and 4.

Bit Number	Mnemonic	Description
15-0	DP(15:0)	Data Pointer Bits. The second and third words of the descriptor block contain the data buffer location. The SμMMIT RTE accesses either Data Pointer A or Data Pointer B depending on the state of Control Word Bit 2 during ping-pong operation. For index operation, the SμMMIT RTE accesses only Data Pointer A. The SμMMIT RTE updates Data Pointer A after message processing is complete and the index field is not equal to zero and ping-pong operation disabled. Bit 15 is the most significant bit; bit 0 is the least significant bit.

2.2.6 Broadcast Data Pointer

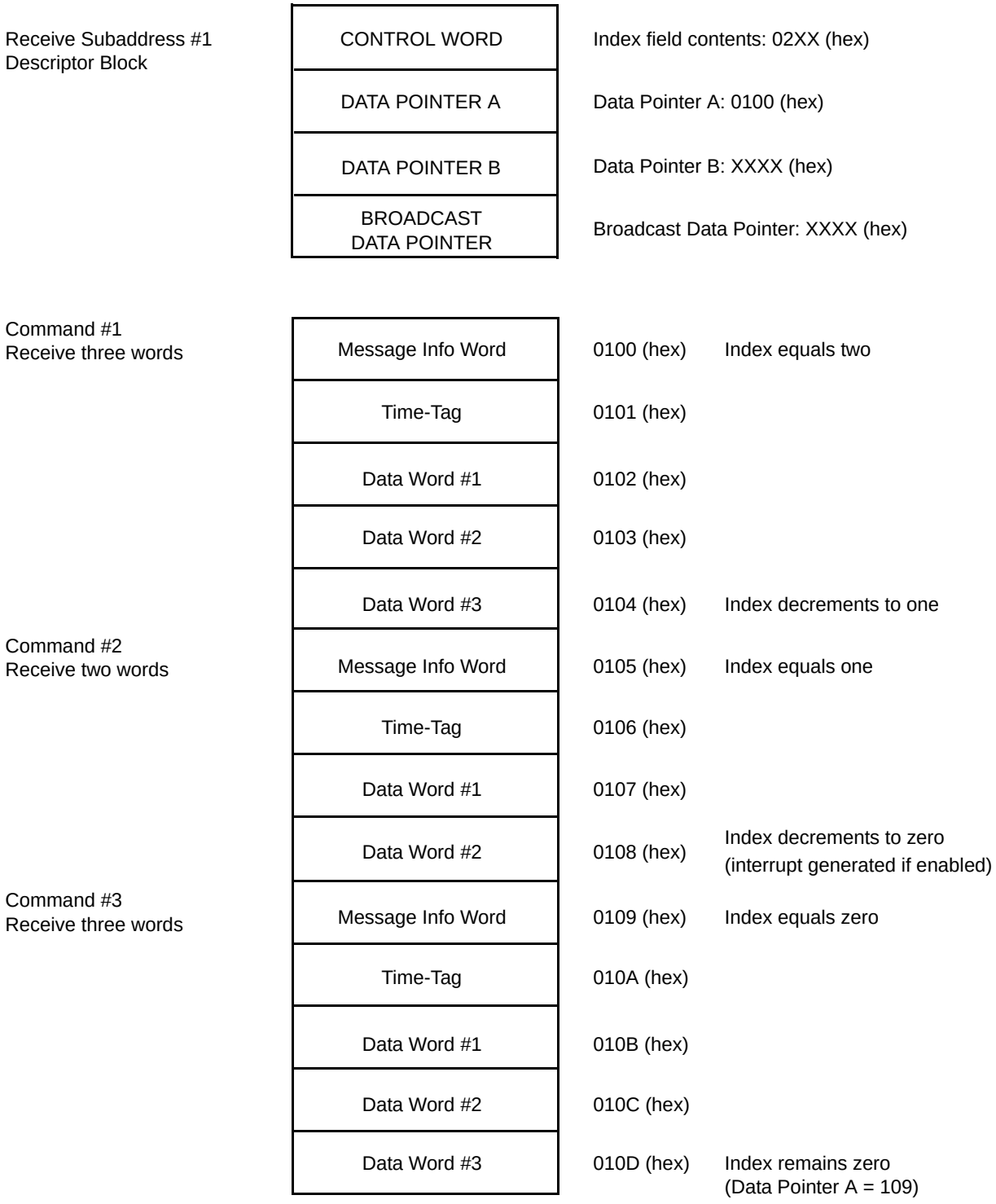
The following bits describe the receive subaddress/mode code descriptor Broadcast Data Pointer. This word contains the address for the Message Information word, Time-Tag word, and data words associated with a broadcast command. The SμMMIT RTE automatically increments this data pointer during command post-processing, if ping-pong operation disabled.

Bit Number	Mnemonic	Description
15-0	BP(15:0)	Broadcast Data Pointer. The fourth word of the descriptor block contains the broadcast data buffer location. This pointer can reside anywhere inside of a 64K data space. The SμMMIT RTE accesses this pointer when Control Word bit 0 is a logic one and broadcast is enabled. Bit 15 is the most significant bit; bit 0 is the least significant bit. Note: If ping-pong is enabled, this pointer does not update. Note: When the broadcast command is followed by a Transmit Last Command or Transmit Status Word mode code, the SμMMIT RTE transmits a status word with bit time 15 of the status word set to a logic one. The broadcast bit is cleared by reception of the next valid non-broadcast command.

2.3 Data Structures

The following sections discuss the data structures that result from command processing. For each complete message processed, the SμMMIT RTE generates a Message Information word and Time-Tag word. These words aid the host or subsystem in further message processing. The Message Information word contains word count, message type, and message error information. The Time-Tag word is a 16-bit word containing the command validity time. The Time-Tag word data comes from the SμMMIT RTE's internal Time-Tag counter.

See section 3, Circular Buffer and Ping-Pong Operation for additional data structure information



Note:
x = “don’t care”

Figure 3. Non-Broadcast Receive Message Indexing

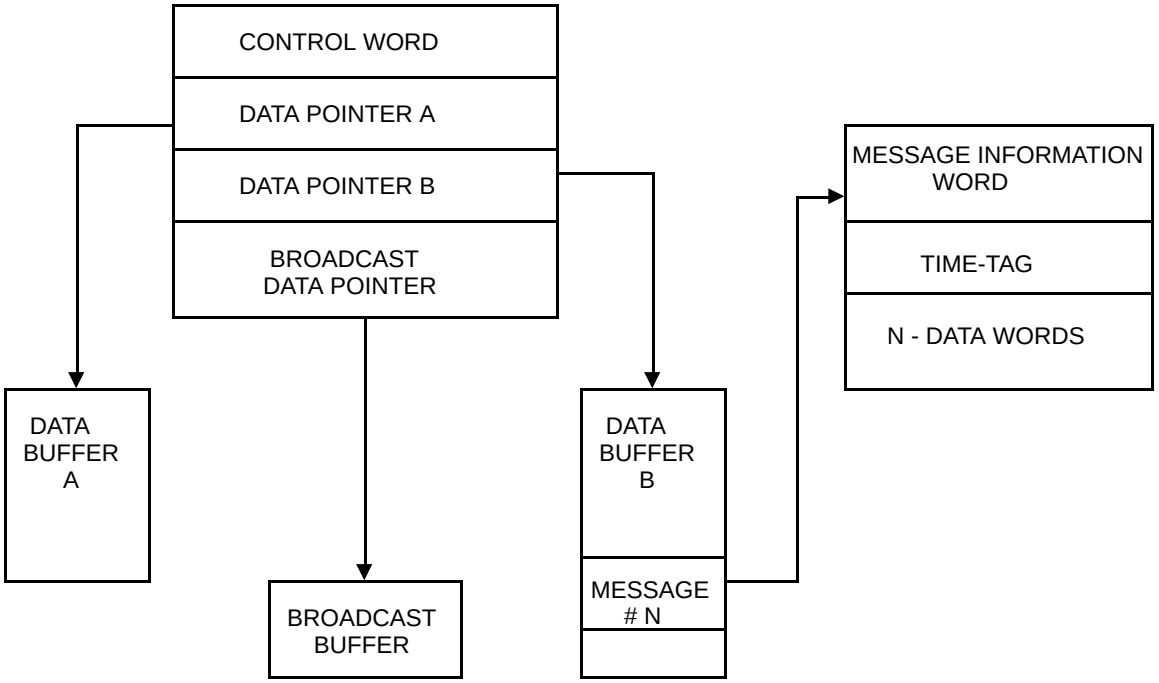


Figure 4. SμMMIT RTE Descriptor Block (Receive)

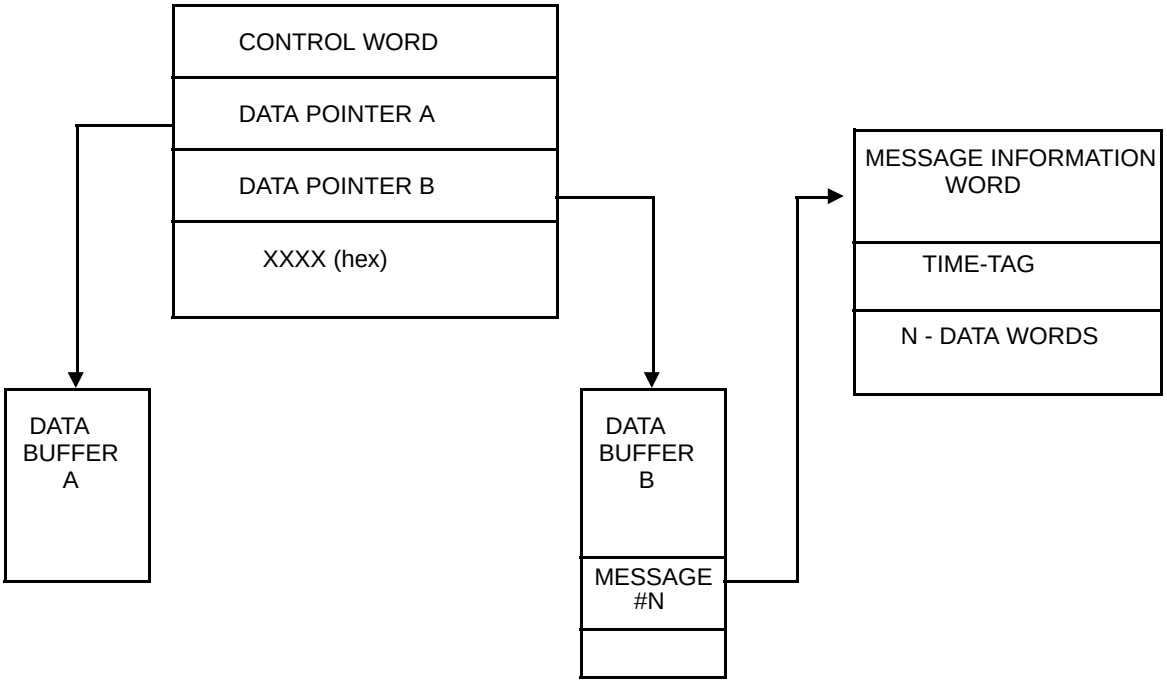


Figure 5. SμMMIT RTE Descriptor Block (Transmit)

2.3.1 Subaddress Receive Data

For receive commands, the SμMMIT RTE stores data words plus two additional words. The SμMMIT RTE adds a Receive Information word and Time-Tag word to each receive command data packet. The SμMMIT RTE places the Receive Information word and Time-Tag word ahead of the data words associated with a receive command (see figures 3, 4 and 5). When message errors occur, the SμMMIT RTE enters the Receive Information word, and Time-Tag word. Once a message error condition is observed, all data words are considered invalid.

Data storage occurs at the memory location pointed to by the data pointer plus two locations.

2.3.1.1 Receive Information (Info) Word

The following bits describe the Receive Information Word contents.

Bit Number	**Mnemonic**	**Description**
15-11	WC(4:0)	Word Count Bits. These five bits contain word count information extracted from the receive command word bit times 15 to 19.
10	N/A	Not applicable.
9	CHA/$\overline{B}$	Channel A/$\overline{B}$. Assertion of this bit indicates that the message was received on channel A. Conversely, if this bit is set to logic zero, the message was received on channel B.
8	RTRT	Remote Terminal to Remote Terminal transfer. The command processed was a RT-to-RT transfer.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for details.
6-5	N/A	Not applicable.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	TO	Time-Out Error. Assertion of this bit indicates the SμMMIT RTE did not receive the proper number of data words, i.e., the number of data words received was less than the word count specified in the command word.
2	OVR	Overrun Error. Assertion of this bit indicates the SμMMIT RTE received a word when none was expected or the number of data words received was greater than expected.
1	PRTY	Parity Error. Assertion of this bit indicates the SμMMIT RTE observed a parity error in the incoming data words.
0	MAN	Manchester Error. Assertion of this bit indicates the SμMMIT RTE observed a Manchester error in the incoming data words.

2.3.2 Subaddress Transmit Data

The host or subsystem is responsible for organization of the data packet (i.e., N data words) into memory and establishing the applicable data pointer. The host or subsystem allocates two memory locations at the top of the data packet for the storage of the Transmit Information word and Time-Tag word. An example transmit data structure for three words is shown below.

```
Data Pointer A -----> 0100 (hex)  XXXX  ;reserved for Transmit Info word
equals 0100 (hex)     0101 (hex)  XXXX  ;reserved for Time-Tag word
                      0102 (hex)  FFFF  ;data word
                      0103 (hex)  FFFF  ;data word
                      0104 (hex)  FFFF  ;data word
```

Note: Data Pointer A points to the top of the data structure not to the top of the data words.

2.3.2.1 Transmit Information (Info) Word

The following bits describe the Transmit Information word contents.

Bit Number	**Mnemonic**	**Description**
15-11	WC(4:0)	Word Count Bits. These five bits contain word count information extracted from the transmit command word bit times 15 to 19.
10	N/A	Not applicable.
9	CHA/$\overline{B}$	Channel A/$\overline{B}$. Assertion of this bit indicates that the message was received on the A bus. Conversely, if this bit is set to logic zero, the message was received on the B bus.
8	N/A	Not applicable.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for more detail.
6-5	N/A	Not applicable.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	N/A	Not applicable.
2	OVR	Overrun Error. Assertion of this bit indicates the SμMMIT RTE received a data word with a Transmit Command.
1-0	N/A	Not applicable.

2.3.3 Mode Code Data

The transmit and receive data structures for mode codes are similar to those for subaddress. The receive data structure contains an Information word, Time-Tag word, and message data word. All receive mode codes with data have one associated data word. Data storage occurs at the memory location pointed to by the data pointer plus two locations. Reception of the synchronize with data mode code automatically loads the Time-Tag counter and stores the data word at the address defined by the data pointer plus two locations.

The transmit mode code data structure contains an Information word, Time-Tag word, and associated data word. The subsystem or host is responsible for linking the SμMMIT RTE Data Pointer to the data (e.g., Transmit Vector word). For mode codes with internally generated data words (e.g., Transmit BIT word, Transmit Last Command), the transmitted data word is added to the data structure.

For MIL-STD-1553A mode of operation, all mode codes are defined without data words. For mode codes without data, the data structure contains the Message Information word and Time-Tag word only.

Note: In MIL-STD-1553A, all mode codes are without data and the T/$\overline{R}$ bit is ignored. See section 2.9 for the MIL-STD-1553A operation.

2.3.3.1 Mode Code Receive Information (Info) Word

The following bits describe the Mode Code Receive Information word contents.

Bit Number	**Mnemonic**	**Description**
15-11	MC (4:0)	Mode Code. These five bits contain the mode code information extracted from the receive command word bits times15 to 19.
10	N/A	Not applicable.
9	CHA/$\overline{B}$	Channel A/$\overline{B}$. Assertion of this bit indicates that the message was received on the A bus. Conversely, if this bit is set to logic zero, the message was received on the B bus.
8	RTRT	Remote Terminal to Remote Terminal transfer. Assertion of this bit indicates the command processed was a RT-to-RT transfer.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for details.
6-5	N/A	Not applicable.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	TO	Time-out Error. Assertion of this bit indicates the SμMMIT RTE did not receive the proper number of data words, i.e., the number of data words received was less than the word count specified in the command word.
2	OVR	Overrun Error. Assertion of this bit indicates the SμMMIT RTE received a word when none was expected, or the number of data words received was greater than expected.
1	PRTY	Parity Error. Assertion of this bit indicates the SμMMIT RTE observed a parity error in the incoming data words.
0	MAN	Manchester Error. Assertion of this bit indicates the SμMMIT RTE observed a Manchester error in the incoming data words.

2.3.3.2 Mode Code Transmit Information (Info) Word

The following bits describe the Mode Code Transmit Information word contents.

Bit Number	Mnemonic	Description
15-11	MC (4:0)	Mode Code. These five bits contain the mode code information extracted from the command word bit times 15 to 19.
10	N/A	Not applicable.
9	CHA/$\overline{B}$	Channel A/$\overline{B}$. Assertion of this bit indicates that the message was received on the A bus. Conversely, if this bit is set to logic zero, the message was received on the B bus.
8	N/A	Not applicable.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for details.
6-5	N/A	Not applicable.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	N/A	Not applicable.
2	OVR	Overrun Error. Assertion of this bit indicates the SµMMIT RTE received a data word with a Transmit Command.
1-0	N/A	Not applicable.

2.4 Mode Code and Subaddress

The SμMMIT RTE provides subaddress and mode code decoding that meets MIL-STD-1553B requirements. In addition, the device has automatic internal illegal command decoding for reserved MIL-STD-1553B mode codes. Table 3 shows the SμMMIT RTE's response to all possible mode code combinations.

Table 3. Mode Code Descriptions

T/R	Mode Code	Function	Operation
0	00000-01111	Undefined (w/o data)	1. Command word stored 2. Status word transmitted
0	10000	Undefined (with data)	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10001	Synchronize (with data)	1. Command word stored 2. Data word stored 3. Time-Tag counter loaded with data word value 4. Status word transmitted
0	10010	Undefined	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10011	Undefined	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10100	Selected Transmitter Shutdown	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10101	Override Selected Transmitter Shutdown	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10110-11111	Reserved	1. Command word stored 2. Data word stored 3. Status word transmitted
1	00000	Dynamic Bus Control	1. Command word stored 2. Dynamic Bus Acceptance bit set in outgoing status word if enabled in the Control Register 3. Status word transmitted
1	00001	Synchronize	1. Command word stored 2. Time-Tag counter reset to 0000 (hex) 3. Status word transmitted
1	00010	Transmit Status Word	1. Command word stored 2. Last status word transmitted 3. Status word cleared after master reset Note: SμMMIT RTE updates status word if illegalized.
1	00011	Initiate Self-Test	1. Command word stored 2. Status word transmitted 3. BIT initiated 4. TF bit set if BITF bit asserted
1	00100	Transmitter Shutdown	1. Command word stored 2. Status word transmitted 3. Alternate bus disabled

Table 3. Mode Code Descriptions (Cont.)

T/R	Mode Code	Function	Operation
1	00101	Override Transmitter Shutdown	1. Command word stored 2. Status word transmitted 3. Alternate bus enabled Note: Reception of the override transmitter shutdown mode code does not enable a channel not previously enabled in the Control Register. Reset remote terminal mode code clears the transmitter shutdown function.
1	00110	Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal flag bit set to zero and assertion disabled 3. Status word transmitted
1	00111	Override Inhibit Terminal Flag	1. Command word stored 2. Terminal Flag bit enabled for assertion 3. Status word transmitted
1	01000	Reset Remote Terminal	1. Command word stored 2. Status word transmitted 3. SμMMIT RTE reset, see section 2.8 for more information on software reset
1	01001-01111	Reserved	1. Command word stored 2. Status word transmitted
1	10000	Transmit Vector Word	1. Command word stored 2. Service request bit set to a logic zero in out going status 3. Status word transmitted 4. Data word transmitted 5. Clears the SRQ bit in the 1553 status word bits register (Register 9)
1	10001	Reserved	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10010	Transmit Last Command	1. Command word not stored 2. Last status word transmitted 3. Last command word transmitted 4. Data word stored (Transmit Last Command) 5. Transmitted data word is all zero after reset Note: The SμMMIT RTE stores the Transmit Last Command mode code if illegalized and updates status word.
1	10011	Transmit BIT Word	1. Command word stored 2. Status word transmitted 3. BIT word transmitted from BIT Word Register 4. Data word stored (Transmit BIT Word)
1	10100-10101	Undefined (with data)	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10110-11111	Reserved	1. Command word stored 2. Status word transmitted 3. Data word transmitted

2.5 Encoder and Decoder

The SμMMIT RTE interfaces directly to a transmitter/receiver via theSμMMIT RTE Manchester II encoder/decoder. The SμMMIT RTE receives the command word from the MIL-STD-1553 bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the SμMMIT RTE processes each incoming data word for correct format, word count, and contiguous data. If a message error is detected, the SμMMIT RTE stops processing the remainder of the message (i.e., DMAs), suppresses status word transmission, and asserts bit 9 (ME bit) of the status word. The SμMMIT RTE will track the message until proper word count is finished.

The SμMMIT RTE automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is asserted in the BIT Word Register and the $\overline{\text{YF\_INT}}$ will be generated, if enabled. In addition to the loop-back compare test, a timer precludes a transmission greater than 800μs by the assertion of Fail-Safe Timer. This timer is reset upon receipt of another command. Remote Terminal Response Time:

MIL-STD-1553A = 7μs
MIL-STD-1553B = 10μs
Data Contiguity Time-Out = 1.0μs

2.6 RT-RT Transfer Compare

The RT-to-RT Terminal Address compare logic ensures that the incoming status word's Terminal Address matches the Terminal Address of the transmitting RT specified in the command word. An incorrect match results in setting the message-error bit and suppressing transmission of the status word. (RT-to-RT transfer time-out = 55 to 59μs). The receiving SμMMIT RTE does not check ME or SSYSF of the transmitting remote terminal.

2.7 Terminal Address

The SμMMIT RTE Terminal Address is programmed via six input pins: RTA(4:0) and RTPTY. Negating $\overline{\text{MRST}}$ latches the SμMMIT RTE's Terminal Address from pins RTA(4:0) and parity bit RTPTY. The address and parity cannot change until the next assertion and negation of the $\overline{\text{MRST}}$ input (for $\overline{\text{LOCK}}$ = 0). The Terminal Address parity is odd; input pin RTPTY is set to a logic state to satisfy this requirement. Assertion of Operational Status Register bit 2 (TAPF) indicates incorrect Terminal Address parity. The Operational Status Register bit 2 is valid after the rising edge of $\overline{\text{MRST}}$.

For example:

RTA(4:0) = 05 (hex) = 00101 (binary)
RTPTY = 1, Sum of 1s = 3 (odd), Operational Status Register Bit 2 = 0

RTA(4:0) = 04 (hex) = 00100 (binary)
RTPTY = 0, Sum of 1s = 1 (odd), Operational Status Register Bit 2 = 0

RTA(4:0) = 04 (hex) = 00100 (binary)
RTPTY = 1, Sum of 1s = 2 (even), Operational Status Register Bit 2 = 1

Note:

- The SμMMIT RTE checks the Terminal Address and parity after the SμMMIT RTE has been started. With Broadcast disabled, RTA(4:0)=11111 operates as a normal RT address.
- The BIT Word Register parity fail bit is valid after the SμMMIT RTE has been started.
- The Terminal Address is also programmed via a write to the Operational Status Register ($\overline{\text{LOCK}}$ = 1).The SμMMIT RTE loads the Terminal Address on the completion of the Control Register write which starts the SμMMIT RTE.
- YF_INT occurs if enabled.

2.8 Reset

The SμMMIT provides for several different reset mechanisms. The SμMMIT software reset (Control Register Bit 13) is equal to a master reset and takes 5μs to complete. Assertion of this bit results in the immediate reset of the SμMMIT RTE and termination of command processing. The host or subsystem is responsible for the re-initialization of the SμMMIT RTE for operation. Configuration of the device for auto-initialization frees the host or subsystem from this task.

A Reset Remote Terminal mode code (Mode Code 01000, T/$\overline{\text{R}}$ =1) is equal to a master reset only if $\overline{\text{AUTOEN}}$ is enabled. If $\overline{\text{AUTOEN}}$ is not enabled, the reset remote terminal mode code clears the encoder/decoders, resets the time-tag, enables the channels to the programmed host state, and re-enables the Terminal Flag for assertion. This reset is performed after the transmission of the 1553 Status word. All outputs have asynchronous reset except $\overline{\text{MSG\_INT}}$. To reset this signal, apply two clock cycles before the rising edge of $\overline{\text{MRST}}$.

Caution: Per the MIL-STD-1553 specification (sections 4.3.3.5.1.7.9 and 30.4.3), a remote terminal must "complete the reset function within 5µs following transmission of the status word." If the $\overline{\text{AUTOEN}}$ function is enabled in the SµMMIT, reset may require additional time depending on the application.

2.9 MIL-STD-1553A Operation

To maximize flexibility, the SµMMIT has been designed to operate in many different systems which use various protocols. Specifically, two of the protocols that the SµMMIT may be interfaced to are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, the SµMMIT may be configured through an external pin or through control register bits (depending on the state of the $\overline{\text{LOCK}}$ pin). Table 4 defines the three ways to program the SµMMIT.

Table 4. MIL-STD-1553A Operation

A/$\overline{\text{B}}$ STD (pin or bit)	**XMTSW (bit only)**	**RESULT (protocol selected)**
0	X	1553B response, 1553B Standard
1	0	1553A response, 1553A Standard
1	1	1553A response, Auto execute the TRANSMIT STATUS WORD mode code

When configured to meet MIL-STD-1553A, the SµMMIT will operate as follows:

- Responds with a status word within 7µs;
- Ignores the T/$\overline{\text{R}}$ bit for all mode codes;
- All mode codes are defined without data;
- All mode codes use mode code transmit control and information words;
- Mode code 00000 is defined as Dynamic Bus Control (DBC);
- Subaddress 00000 defines a mode code;
- ME and TF bits are defined in the 1553 status word; all other status word bits are programmable (i.e., NO BUSY mode, etc.);
- Broadcast of all mode codes, except Mode Code 00000 (DBC) and Mode Code 00010 (Transmit Status word if enabled), is allowed;
- To illegalize a Mode Code, the user needs to illegalize both the receive and transmit versions;
- Illegalization of row 1F (hex) is not automatic.

3.0 CIRCULAR BUFFERS and PING-PONG OPERATIONS

3.1 Data Management

The SμMMIT RTE circular buffer simplifies the software service of remote terminals implementing bulk or periodic data transfers. The Enhanced SμMMIT architecture allows the user to select one of two circular buffer modes. The user selects the preferred mode, at start-up, by writing to Control Register bits 7 and 8. The Control Register bits allow for the decode of three unique modes. Table 5 reviews mode selections.

Table 5. Enhanced Mode of Operation

Mode Number	Bit 7	Bit 8
0	0	0
1	0	1
X	1	0
2	1	1

3.1.1 Mode Number 0

Remote Terminal Index or Ping-Pong Operation, non-Enhanced SμMMIT, the user programs bits 7 and 8 to logical zero. Operation is per sections 2.2 and 2.3 (default state).

3.1.2 Mode Number 1

Remote Terminal Buffer 1, the user programs bit 7 to a logical 0 and bit 8 to a logical 1. The SμMMIT RTE merges transmit and receive data into a circular buffer along with message information. For each valid receive message, the SμMMIT RTE enters a message information word, time-tag word, and data word(s) into a unique receive circular buffer. For each valid transmit message, the SμMMIT RTE enters a message information word and time-tag word into reserved memory locations within the transmit circular buffer. The SμMMIT RTE automatically controls the wrap around of circular buffers.

Two pointers define circular buffer length: top of buffer and bottom of buffer. The lower case user specifies the top of buffer (i.e., top address (TA_{16})) by writing a value into the second word of a unique mode code or subaddress descriptor block. The user defines the bottom of the buffer (i.e., bottom address (BA_{16})) by writing to the fourth word of that unique descriptor block. Both the TA_{16} and BA_{16} remain static during message processing. The third word in the descriptor block identifies the current address (i.e., last accessed address plus one). The circular buffer wraps to the top address after completing a message that results in CA_{16} being greater than or equal to BA_{16}. If CA_{16} increments past BA_{16} during intra-message processing, the SμMMIT RTE will access memory (read or write) address locations past BA_{16}. Delimit all circular buffer boundaries with at least 34 address locations.

Each subaddress and mode code, both transmit and receive, has a unique circular buffer assignment. The SμMMIT RTE decodes the command word T/R bit, subaddress/mode field, and word count/mode code field to select a unique descriptor block which contains TA_{16}, CA_{16}, and BA_{16}.

For receive messages, the SμMMIT RTE stores the message information word into address location CA_{16}, the time-tag word into $CA_{16}+ 1_{16}$, and the data into the next "N_{16}" locations starting at address $CA_{16}+2_{16}$. For each transmit command, the SμMMIT RTE stores the message information word into address location CA_{16} and time-tag word into location $CA_{16}+ 1_{16}$. Retrieval of data for transmission starts at address location $CA_{16} + 2_{16}$. When entering multiple transmit command data packets into the circular buffer, delimit each data packet with two reserved memory locations. The SμMMIT RTE enters the message information word and time-tag word into the delimiting memory locations.

3.1.3 Mode Number 2

Circular Buffer 2, the user programs Control Register bit 7 to a logical 1 and bit 8 to a logical 1. The SμMMIT RTE separates message data and message information into unique circular buffers. The separation of data from message information simplifies the software that loads and unloads data from the buffers. Each subaddress and mode code, both transmit and receive, has a unique pair of circular buffers. The SμMMIT RTE decodes the command word T/R bit, subaddress/mode field, and word count/mode code field to select a unique descriptor block which contains TA_{16}, CA_{16}, and Message Information Buffer (MIB).

Control the wrap-around of both the data and message buffers by specifying the number of messages before wrap-around occurs in bits 15 to 8 of the Control Word. The second word entered into the descriptor block determines the top of the data buffer (TA_{16}). The third word in the descriptor block identifies the current position (CA_{16}) in the buffer (i.e., last accessed address plus one). The fourth word in the descriptor block identifies the MIB's starting location and current position. The MIB contains Time-Tag and Message Information words for each message transacted on the bus. The data buffer and Message Information Buffer wrap around after processing a predetermined number of messages. Each subaddress and mode code, both transmit and receive, have a unique data buffer and MIB assignment.

3.2 Ping-Pong Handshake

The SμMMIT RTE provides a software handshake which indicates the enable and disable of buffer ping-pong operation. During remote terminal operation, the SμMMIT RTE asynchronously ping-pongs between two subaddress or mode code data buffers. To perform buffer service, the application software must freeze the remote terminal's access to a single buffer. The SμMMIT RTE's ping-pong enable/disable handshake allows the application software to asynchronously freeze (i.e., disable ping-pong operation) the remote terminal to a single buffer.

3.2.1 Ping-Pong Enable/Disable Handshake

Prior to starting remote terminal operation, enable the buffer ping-pong feature by writing a logical 1 to bit 2 of the Control Register. During ping-pong operation, the remote terminal ping-pongs between the two data buffers, for each subaddress or mode code, on a message by message basis. Each unique MIL-STD-1553 subaddress and mode code is assigned two data buffer locations (A and B). The remote terminal retrieves data from a buffer or stores data into a buffer depending on the message type (i.e., transmit or receive command). During ping-pong operation, the remote terminal determines the active subaddress or mode code buffer at the beginning of message processing, the remote terminal complements bit 2 of the Descriptor Control Word to access the alternate buffer on the following message (i.e., ping-pong). See Figure 6 for ping-pong buffer flow chart.

To off-load or load the subaddress and mode code buffers without collisions (e.g., remote terminal writing and application software reading the same buffer), the application software must disable ping-pong operation (i.e., freeze the remote terminal access to a single buffer, either A or B). Disabling ping-pong operation allows the application software to off-load or load the alternate buffer while the remote terminal continues to use the active buffer. To implement this architecture, ping-pong operation must enable and disable asynchronously via software with feedback to indicate that buffer ping-ponging is truly disabled. Second, unique subaddress and mode code flags indicate which buffer is active. Each unique subaddress and mode code is assigned a flag which indicates the active buffer.

To begin the process of off-loading or loading the remote terminal's subaddress and/or mode code buffers, when using the ping-pong feature, the application software performs the following sequence: disables ping-pong operation, determines the active buffer, services the alternate buffer, enables ping-pong operation.

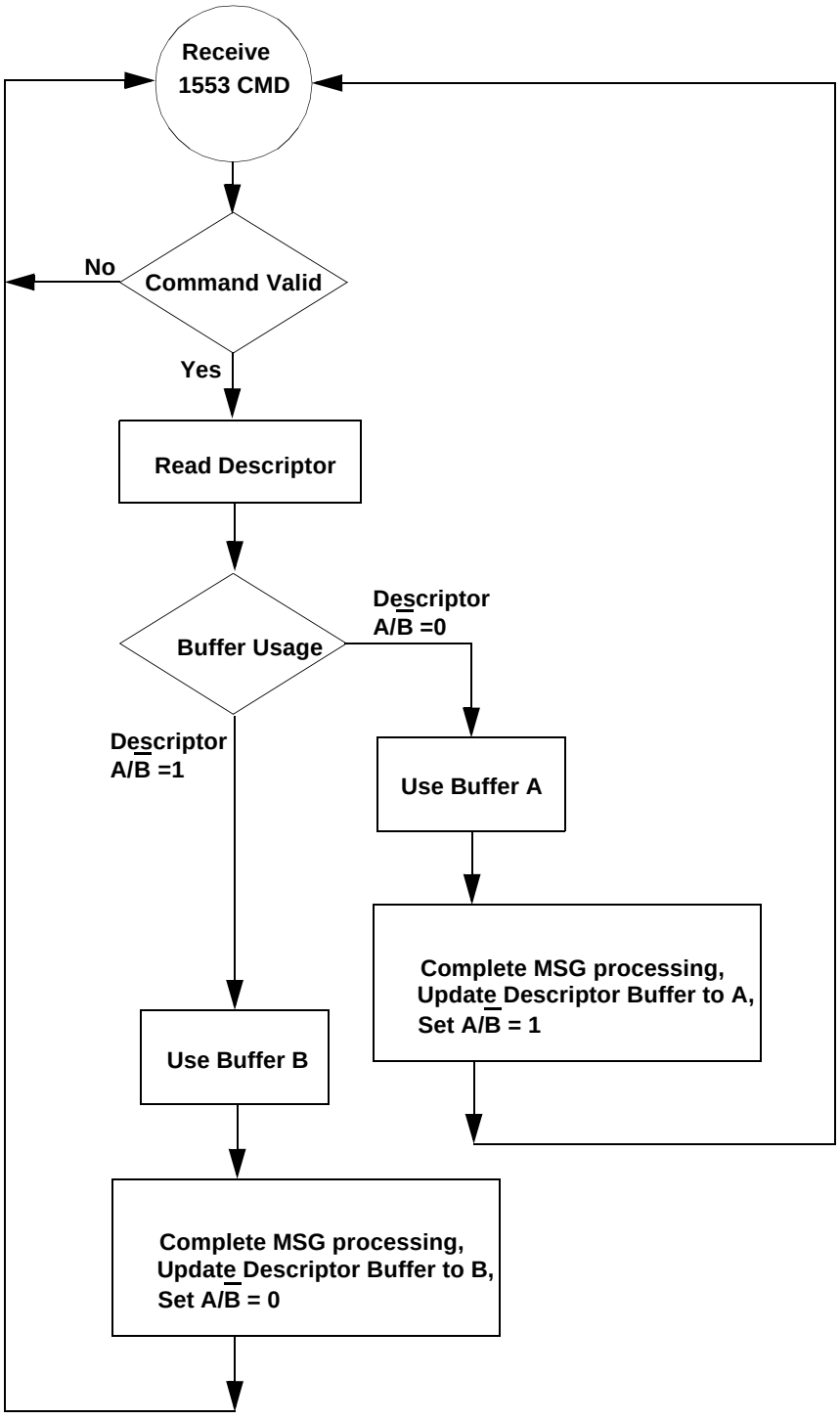


Figure 6. Ping-Pong Buffer Flow Chart

The application software disables ping-pong operation by writing a logical zero to Control Register bit 2. The disable of ping-pong operation is acknowledged by bit 9 of the Control Register. Bit 9 of the Control Register acknowledges the ping-pong disable by transitioning from a logical one to a logical zero. The application software interrogates bit 2 of each Descriptor Control Word to determine the active buffer on a subaddress or mode code basis. If bit 2 is a logical zero, the remote terminal uses Buffer A and the application software off-loads or loads Buffer B. If bit 2 is a logical one, the remote terminal uses Buffer B and the application software off-load or loads Buffer A. Figure 7 displays Control Register bits for ping-pong enable/disable and acknowledge.

The application software enables ping-pong operation by writing a logical one to Control Register bit 2. The enable of ping-pong operation is acknowledged by bit 9 of the Control Register. Bit 9 of the Control Register acknowledges the ping-pong enable by transitioning from a logical zero to a logical one.

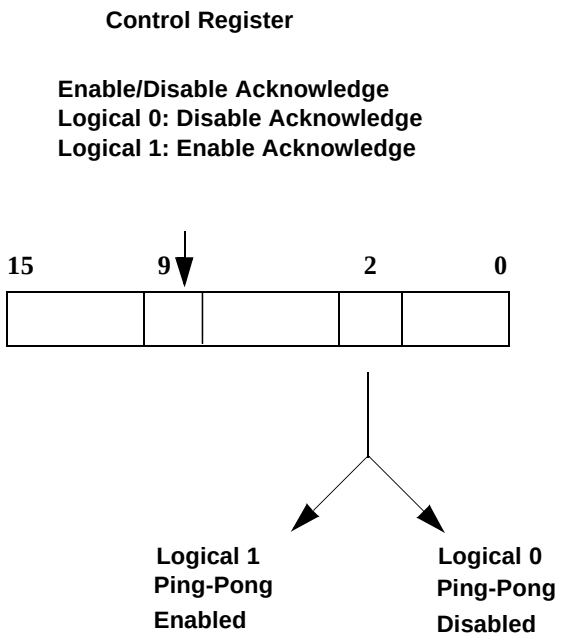


Figure 7. Ping-Pong Handshake

3.2.1.1 Ping-Pong Enable/Disable Examples

The following examples will walk through some enabling and disabling behaviors of the SμMMIT RTE Ping-Pong mode of operation. Note that when enabling and disabling ping-ponging, the act of enabling or disabling must be observed via the acknowledge bit. If no acknowledge is seen, the user must make another attempt at enabling or disabling.

Example 1: Typical Ping-Pong Enable and Disable

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Start execution	1	x	x	x	x	x	0	x	x	x	x	x	x	1	x	x
2	Read result of Start w/PP	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x	x
3	Disable of PP	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x	x
4	Read result of disable	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x
5	Enable of PP	1	x	x	x	x	x	0	x	x	x	x	x	x	1	x	x
6	Read result of enable	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x	x

Example 2: Failed Disable of Ping-Pong

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
1	Disable of PP (just after internal μC has copied control register)	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x
2	Read result of disable (no acknowledge, must retry)	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x

Example 3: Failed Enable of Ping-Pong Control

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Enable of PP (just after internal μC has copied control register)	1	x	x	x	x	x	0	x	x	x	x	x	x	1	x	x
2	Read result of enable (no enable, must retry)	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x

The maximum time between an enable/disable attempt and an observed result is about 32µS. When writing to enable/disable, the user reads the acknowledge bit reflecting the last machine state, e.g., if enabled, bit 9 = 1, if disabled, 9 = 0.

Note: Bit 9 of the control register is meant to be read only, but can be written to. Do not write to Bit 9.

Example 4: Misuse of Ping-Pong Control

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Start execution	1	x	x	x	x	x	0	x	x	x	x	x	x	1	x	x
2	Read result of Start w/PP	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x	x
3	Disable of PP (Writing Bit 9)	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x
4	Read back	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x
5	Read back 32µS later	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x
6	When did the SuMMIT acknowledge? Can't tell																

Do you have to wait 32µS? No, not always. The user should poll for acknowledge.

Example 5: Longest Acknowledge Delay

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Disable PP	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x	x
2	Read back (enabled)	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x	x
3	Read back 32uS later (worst case)	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x

What if we don’t see acknowledge? You’ll be able to tell right away if an acknowledge is coming or not.

Example 6: Missed Acknowledge

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Disable PP	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x	x
2	Read back	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x	x
3	In this case, the users write was overwritten; the user must re-write and look for acknowledge.																

3.3 Circular Buffer Mode #1

To implement Circular Buffer 1's architecture, the four word descriptor block and Control Register are different than in the mode #0. Bits 15 through 8 of the Control Word are don't care. The second word of the descriptor block defines the buffer's starting or top address (TA_{16}). The TA pointer remains static during message processing. The fourth entry into the descriptor block identifies the buffer's bottom address (i.e., BA_{16}) and also remains static during message processing. The third descriptor block word represents the current address (i.e., CA_{16}) in the buffer and is dynamic. If the SμMMIT RTE observes no message error conditions, the CA_{16} pointer updates at the end of message processing. The application software reads the dynamic CA_{16} pointer to determine the current bottom of the buffer.

First, a review of receive message processing. The SμMMIT RTE begins all message processing by reading a unique descriptor block after reception and validation of a subaddress or mode code command word. The SμMMIT RTE internally increments the CA_{16} pointer to store the receive data word(s). After message processing completes, the SμMMIT RTE stores the message information word and time-tag word into the circular buffer preceding the message data. At the end of message processing, the SμMMIT RTE updates CA_{16} (if no errors are detected). For CA_{16} larger than BA_{16} storage of the next message begins at the address location pointed to by the TA_{16} pointer, and CA_{16} is made equal to TA_{16}. If CA_{16} is less than BA_{16} , CA_{16} points to the next available memory location in the buffer (i.e., $CA_{16} + 1$).

For transmit commands, the SμMMIT RTE begins transmission of data from memory location $CA_{16} + 2_{16}$. Reserve the first two locations for the message information word and time-tag word. After message processing completes, the SμMMIT RTE enters the message information word and time-tag word into the circular buffer. At the end of message processing, the SμMMIT RTE updates CA_{16} (if no errors are detected). For CA_{16} larger than BA_{16}, storage of the next message begins at the address location pointed to by the TA_{16} pointer, and CA_{16} is made to equal TA_{16}. If CA_{16} is less than BA_{16}, CA_{16} points to the next available memory location in the buffer (i.e. $CA_{16} + 1$).

In this mode of operation, bits INDX, NII and A/B of the Descriptor Control Word and the PPEN bit of the Control Register are don't care. Message information word bit 5 reflects the reception of broadcast message via the BRD bit.
The SμMMIT RTE generates a circular buffer empty/full interrupt when the buffer reaches the end (i.e., CA_{16} greater than BA_{16}) and begins a new message at the top of the buffer. Bit 8 of the Mask Register and bit 7 of the Descriptor Control Word mask and enable the generation of the Full/Empty interrupt. Bit 8 of the Interrupt Mask Register is specified in section 2.1.4, and bit 7 of the Descriptor control word is described for receive control words in Section 2.2.1 and 2.2.3. When either interrupt occurs, the output will be asserted, and bit 8 in both the Pending Interrupt Register and the Interrupt Information Word will be asserted. Section 2.1.5 describes each bit in the Pending Interrupt Register, and Table 8 specifies each bit in the Interrupt Information Word. Figure 8 describes the relationship between TA_{16}, BA_{16}, and CA_{16}.

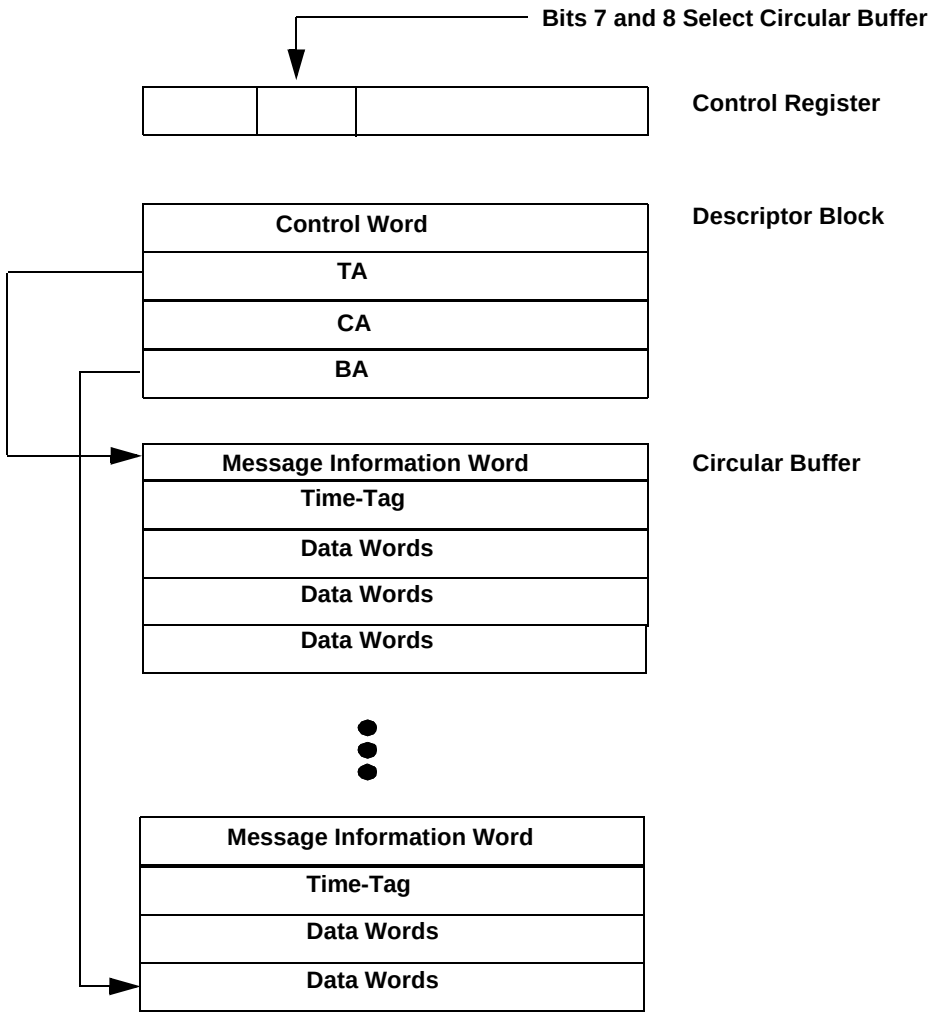


Figure 8. Circular Buffer Mode #1

3.4 Circular Buffer Mode #2

To implement Circular Buffer 2's architecture, the descriptor block and Control Register are different than in mode #0. Bits 15 through 8 of the Control Word specify the Message Information Buffer (MIB) length; the maximum MIB length is 256. Table 6 shows how the Control Word's most significant bits select the depth of the MIB. The Control Words eight most significant bits remain static during message processing.

The second word of the descriptor block defines the top address (TA_{16}) of the data circular buffer. The TA_{16} pointer remains static during message processing. The third descriptor word identifies the current address (i.e., CA_{16}) of the data circular buffer. The application software reads the dynamic CA_{16} pointer to determine the current address of the data buffer. The SμMMIT RTE increments the CA_{16} pointer, at the end of message processing, until the MIB buffer is full. When the MIB wraps around, the SμMMIT RTE loads the CA_{16} pointer with the TA_{16} pointer.

The fourth word in the descriptor block defines the top or base address of the Message Information Buffer (i.e., MIB) and the current MIB address (i.e., offset from base address). The SμMMIT RTE enters the message information word and time-tag word into the MIB, for each message, until the end of the MIB is reached. When the MIB reaches the end, the next message's message information word and time-tag word is entered at the top of the MIB. The MIB pointer is a semi-static pointer. The SμMMIT RTE updates the current address field at the end of message processing. The base address field remains static.

Application software reads the current MIB address to determine the number of messages processed since last service. The variable length MIB requires the base address and current address field to also vary in length. Table 6 displays the relationship between Control Word bits 15 through 8, MIB length, MIB base and current address fields. The current address field of the MIB must begin on an even boundary.

First is a review of receive message processing. The SμMMIT RTE begins all message processing by reading the descriptor block of the subaddress or mode code command received (i.e., Control Word, TA_{16}, CA_{16}, and MIB). The SμMMIT RTE begins storage of data word(s) starting at the location contained in the CA_{16} pointer. The SμMMIT RTE automatically updates the CA_{16} pointer internally as message processing progresses. After receiving the correct number of data words, the SμMMIT RTE stores the message information word and time-tag word into the MIB. At the end of message processing, the SμMMIT RTE updates CA_{16} and MIB Current Address Field (CAF). If CAF equals the specified MIB length, CA_{16} is updated to TA_{16} and the MIB CAF is reset to zero. If CAF is less than the specified MIB length, CA_{16} and MIB CAF point to the next available memory location in each buffer. Control Word bits 15 to 8 specify the MIB length.

For transmit commands, the SμMMIT RTE begins transmission of data from memory location CA_{16}. After message processing completes, the SμMMIT RTE enters the message information word and time-tag word into the MIB. At the end of message processing, the SμMMIT RTE updates CA_{16} and the MIB CAF. If CAF equals the specified MIB length, CA_{16} is updated to TA_{16} and the MIB CAF is reset to zero. If CAF is less than the specified MIB length, CA_{16} and MIB CAF point to the next available memory location in each buffer.

In this mode of operation, bits INDX, NII and A/B of the descriptor control word and the PPEN bit of the Command Register are don't care. The BRD bit is added to the Message Information Word bit 5.

The SμMMIT RTE generates a circular buffer empty/full interrupt when the MIB reaches the end and begins a new message at the top of the buffer. Bit 8 of the Mask Register and bit 7 of the descriptor Control Word mask and enable the generation of the Full/Empty interrupt. Bit 8 of the Interrupt Mask Register is specified in section 2.1.4, and bit 7 of the Descriptor control word is described for receive control words in Section 2.2.1 and 2.2.3. When either interrupt occurs, the output will be asserted, and bit 8 in both the Pending Interrupt Register and the Interrupt Information Word will be asserted. Section 2.1.5 describes each bit in the Pending Interrupt Register, and Table 8 specifies each bit in the Interrupt Information Word. Figure 9 describes the relationship between TA_{16}, CA_{16}, and MIB.

Table 6. Control Word and MIB Length

Control Word Bits (15:8)	Length of MIB	# of Messages	MIB Pointer Base and CAF [Base Address][CAF] = Memory Location Bit Positions 15 - 14 - 13 - 12 - 11 - 10 - 9 - 8 - 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
FF	256	128	[----------Base Address ----------][----------CAF---------]
7F	128	64	[----------Base Address----------][----------CAF---------]
3F	64	32	[----------Base Address----------][----------CAF---------]
1F	32	16	[----------Base Address----------][----------CAF---------]
0F	16	8	[----------Base Address----------][----------CAF------]
07	8	4	[----------Base Address----------][----------CAF---]
03	4	2	[----------Base Address----------][-------CAF-]
01	2	1	[----------Base Address----------][CAF]

Note:
User must use one of these eight choices.

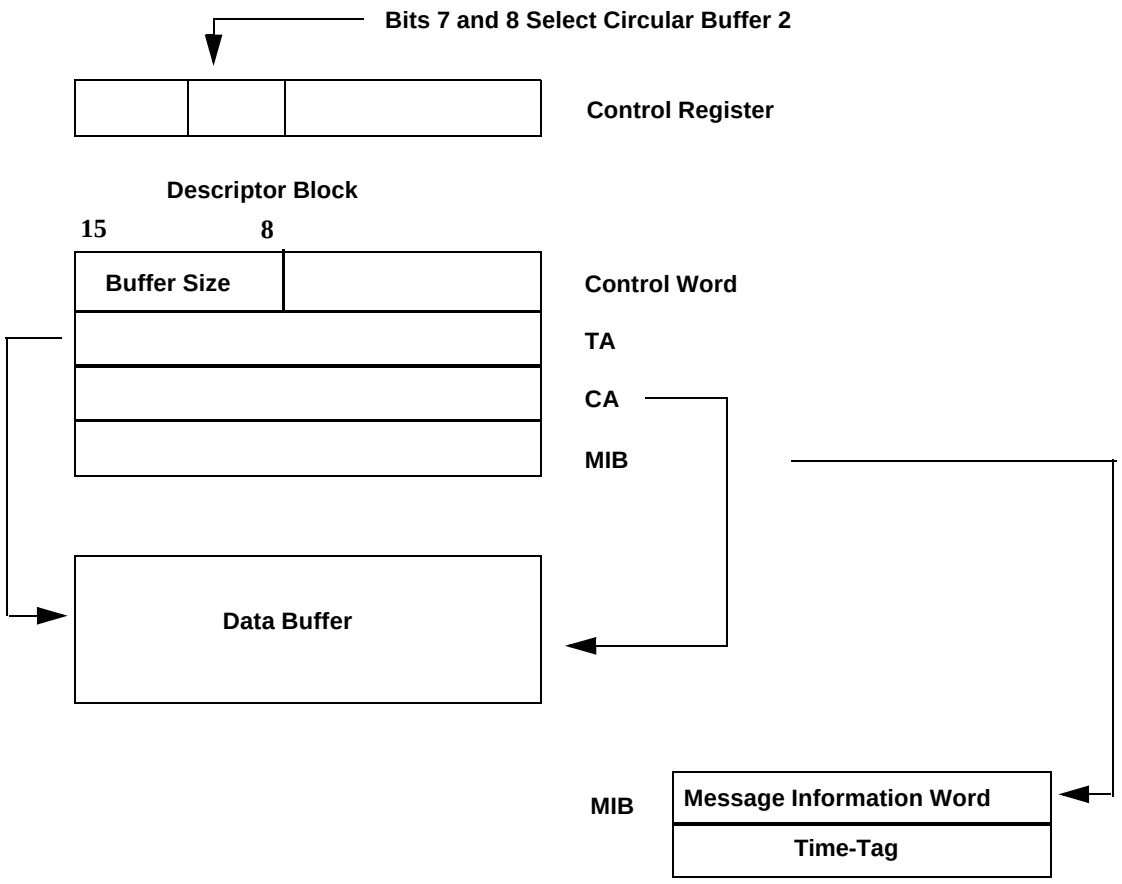


Figure 9. Circular Buffer Mode #2

4.0 INTERRUPT ARCHITECTURE

The SµMMIT RTE's interrupt architecture involves three internal registers, an Interrupt Log List, two interrupt outputs, and two interrupt acknowledges. The three internal registers include a Pending Interrupt Register, Interrupt Mask Register, and Interrupt Log List Register. See figure 10 and register descriptions for additional information. The Pending Interrupt Register contains information that identifies the events generating the interrupts. The Interrupt Mask Register allows the user to mask or disable the generation of interrupts. The Interrupt Log List Register contains the base address of a 32-word interrupt ring buffer. Two interrupt outputs signal the occurrence of an interrupt event. The interrupt architecture differentiates interrupts as either a hardware interrupt ($\overline{\text{YF\_INT}}$) or message interrupt ($\overline{\text{MSG\_INT}}$). The user programs the interrupt outputs as either pulsed outputs or level outputs depending on system requirements.

Assertion of the $\overline{\text{YF\_INT}}$ interrupt signals a hardware failure condition. Failures include DMA time-out, wrap-around self-test, terminal address parity, or built-in test (BIT). $\overline{\text{YF\_INT}}$ failures are reflected in the four most significant bits of the Pending Interrupt Register. The $\overline{\text{YF\_INT}}$ output asserts on the occurrence of a failure.

Assertion of the $\overline{\text{MSG\_INT}}$ interrupt signals a message related event has occurred. $\overline{\text{MSG\_INT}}$ events are reflected in the 12 least significant bits of the Pending Interrupt Register. The $\overline{\text{MSG\_INT}}$ asserts after message processing is complete.

The interrupt architecture allows for the entry of 16 interrupts into a 32-word ring buffer (see figure 10). The SµMMIT RTE automatically handles the interrupt logging overhead. Each interrupt generates two words of information to help the host or subsystem perform interrupt processing. The Interrupt Identification Word (IIW) identifies the type(s) of interrupt that occurred. The Interrupt Address Word (IAW) identifies the interrupt source (e.g., subaddress or command block) via a 16-bit address.

The SµMMIT RTE's interrupt outputs are user programmable. The user can select either pulsed interrupt outputs or level sensitive outputs. In the level mode of operation, assertion of either input (i.e., $\overline{\text{YF\_ACK}}$ or $\overline{\text{MSG\_ACK}}$) negates the respective interrupt output (i.e., $\overline{\text{YF\_INT}}$ or $\overline{\text{MSG\_INT}}$). The state of MSEL(4) selects the mode of operation, Table 7 reviews operation.

Table 7. MSEL(4) Operation

MSEL(4)	$\overline{\text{YF\_INT}}$ / $\overline{\text{MSG\_INT}}$	$\overline{\text{YF\_ACK}}$ / $\overline{\text{MSG\_ACK}}$
0	Pulse Output	Tied High
1	Level Output	Active Low

4.1 Interrupt Identification Word (IIW)

The Interrupt Identification Word (IIW) is a 16-bit word identifying the interrupt type(s). The format is similar to the Pending Interrupt Register. The host or subsystem reads the IIW to determine which interrupt event occurred. The bit descriptor for the IIW is provided in Table 8.

4.2 Interrupt Address Word (IAW)

The Interrupt Address Word (IAW) is a 16-bit word that identifies the interrupt source.

4.3 Interrupt Log List Address

The interrupt log list resides in a 32-word ring buffer. The host or subsystem defines the location buffer, within a 4K x 16 memory space, via the Interrupt Log List Register (Register 5). Restrict the ring buffer address to a 32-word boundary.

During initialization the host or subsystem writes a value to the Interrupt Log List Pointer Register, initializing the least significant five bits to a logic zero. The next 7 bits (bit 5 through 11) determines the base address of the buffer. The SµMMIT RTE increments the ring buffer pointer on the occurrence of the first interrupt, storing the IIW and IAW at locations 00000 and 00001 respectively. The SµMMIT RTE logs ensuing interrupts sequentially into the ring buffer until interrupt number 16 occurs. The SµMMIT RTE enters interrupt 16's IIW in buffer location 11110 and the IAW at location 11111. The ring wraps-around at a value of 11111.

The SµMMIT RTE increments the ring buffer pointer as interrupts occur. The least significant five bits of the Interrupt Log List Pointer Register reflect the ring buffer pointer value. Figure 10 and Table 3 shows the ring buffer interrupt architecture.

The host or subsystem reads the ring buffer pointer value to determine the number of interrupts that have occurred. By extracting the least significant five bits from the Interrupt Log List Register and logically shifting the data once to the right, the host or subsystem determines the number of interrupt events.

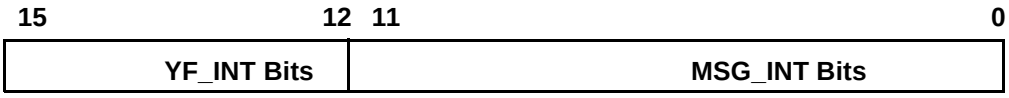


Figure 10. Pending Interrupt and Mask Register

Table 8. Interrupt Identification Word

Bit Number	Mnemonic	Description
15-12	N/A	Not Applicable.
11	MERR	Message Error Interrupt (All modes).
10	SUBAD	Subaddress Accessed Interrupt.
9	BDRCV	Broadcast Command Received Interrupt.
8	IXEQ0	Index Equal Zero Interrupt.
7	ILCMD	Illegal Command Interrupt.
6	N/A	Not Applicable.
5	N/A	Not Applicable.
4	N/A	Not Applicable.
3	N/A	Not Applicable.
2	N/A	Not Applicable.
1	N/A	Not Applicable.
0	N/A	Not Applicable.

5.0 Auto-Initialization

The SμMMIT RTE auto-initialization feature allows autonomous operation. The SμMMIT RTE will automatically configure itself for operation from nonvolatile byte-wide memory (PROM, ROM, E^2PROM, EPROM, etc.). The configuration sequence begins after the negation of input pin $\overline{\text{MRST}}$, if $\overline{\text{AUTOEN}}$ is enabled.

During auto-initialization, the SμMMIT RTE loads all internal registers and transfers the descriptor space into RAM. Initialize registers not used during SμMMIT RTE operation to 0000 (hex). The SμMMIT RTE must have 64 memory locations allocated for register data.

Following register initialization, the SμMMIT RTE reads the descriptor from ROM and enters the descriptor into RAM. The starting address for the descriptor is read from the Descriptor Pointer Register. The SμMMIT RTE internally generates all address information required for auto-initialization.

The SμMMIT RTE requires 1088 consecutive ROM locations for initialization. The 1088 memory locations include: 64 for internal register information, 512 for subaddress descriptor information, and 512 for mode code descriptor information. Unused descriptor blocks should be initialized to four words of 0000 (hex).

The SRT accesses 1088 consecutive memory locations in 64-word blocks. Once access is granted, the SRT reads words from ROM, then transfers the information into RAM. The SμMMIT RTE does not respond to MIL-STD-1553 commands until initialization is complete, the start execution bit has been set, and the RT parity has been verified. After initialization, the SμMMIT RTE can respond to MIL-STD-1553 commands.

5.1 Auto-Initialization Hardware

An external auto-initialization bus allows configuration of SμMMIT RTE without host intervention. Auto-initialization is ideal for low cost remote sensing applications where a host microprocessor or microcontroller is not required.

To enable the auto-initialization function, assert the $\overline{\text{AUTOEN}}$ pin prior to the rising edge of $\overline{\text{MRST}}$. The de-assertion of $\overline{\text{MRST}}$ signals the beginning of the auto-initialization sequence. The SμMMIT RTE enables the boot memory by asserting the $\overline{\text{ECS}}$ output. The SμMMIT RTE accesses up to 8K x 8 words via the auto-initialization bus.

To interface to slower non-volatile memory the auto-initialization read cycle period is programmable. The user selects between zero and seven wait states per read. A wait state is equal to 82ns. The user programs the read cycle duration via inputs EC(2:0). The SμMMIT RTE latches inputs EC(2:0) on the rising edge of $\overline{\text{MRST}}$. Table 9 reviews the possible combinations of wait-states. Figures 11a and 11b show a system configuration along with typical auto-initialization read cycles. Following completion of an auto-initialization sequence the SμMMIT RTE asserts the $\overline{\text{READY}}$ output.

Table 9. Programmable Wait-State

$EC(2:0)_2$	Number of Wait-States
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

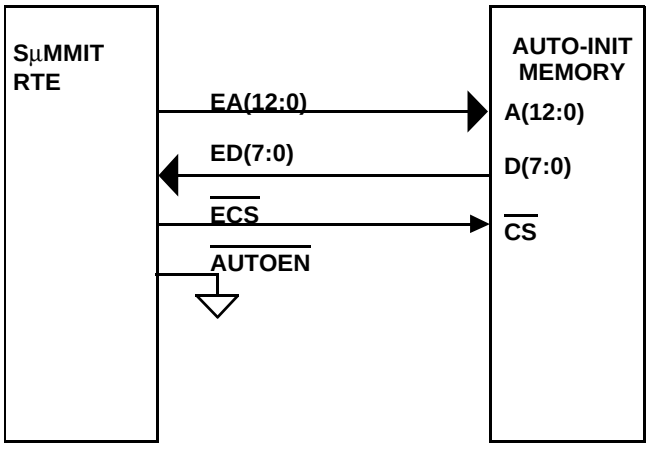
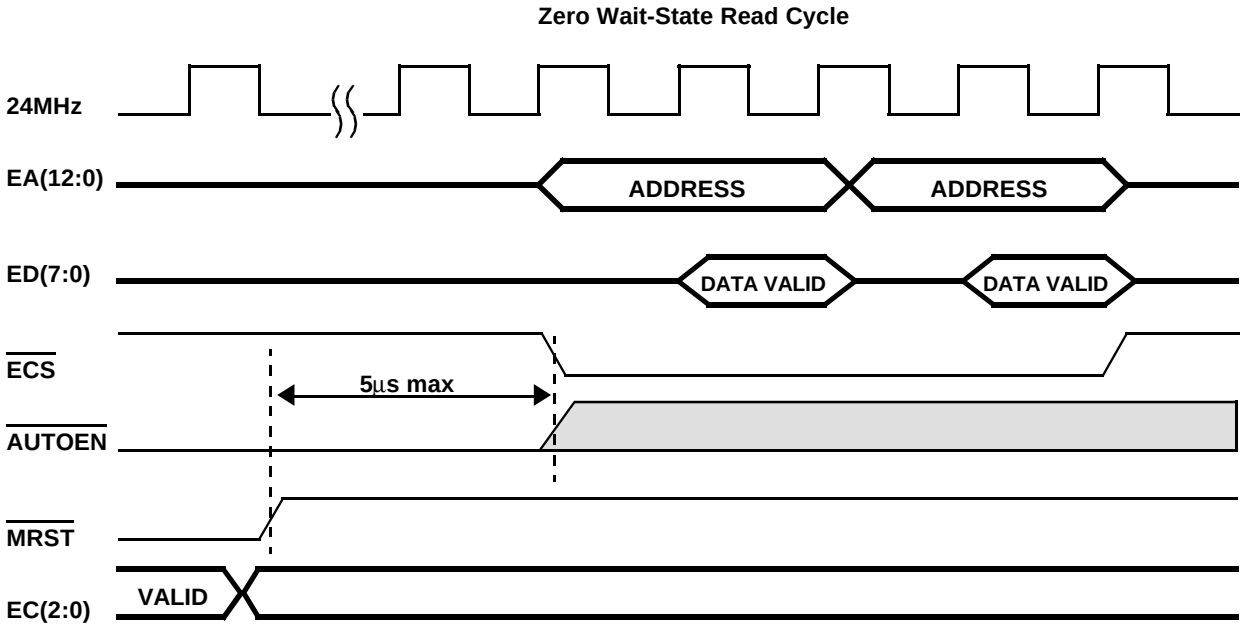


Figure 11a. Auto-Initialization System Configuration



Note:
Two bytes are read on each ECS cycle using only an address transition (AT).

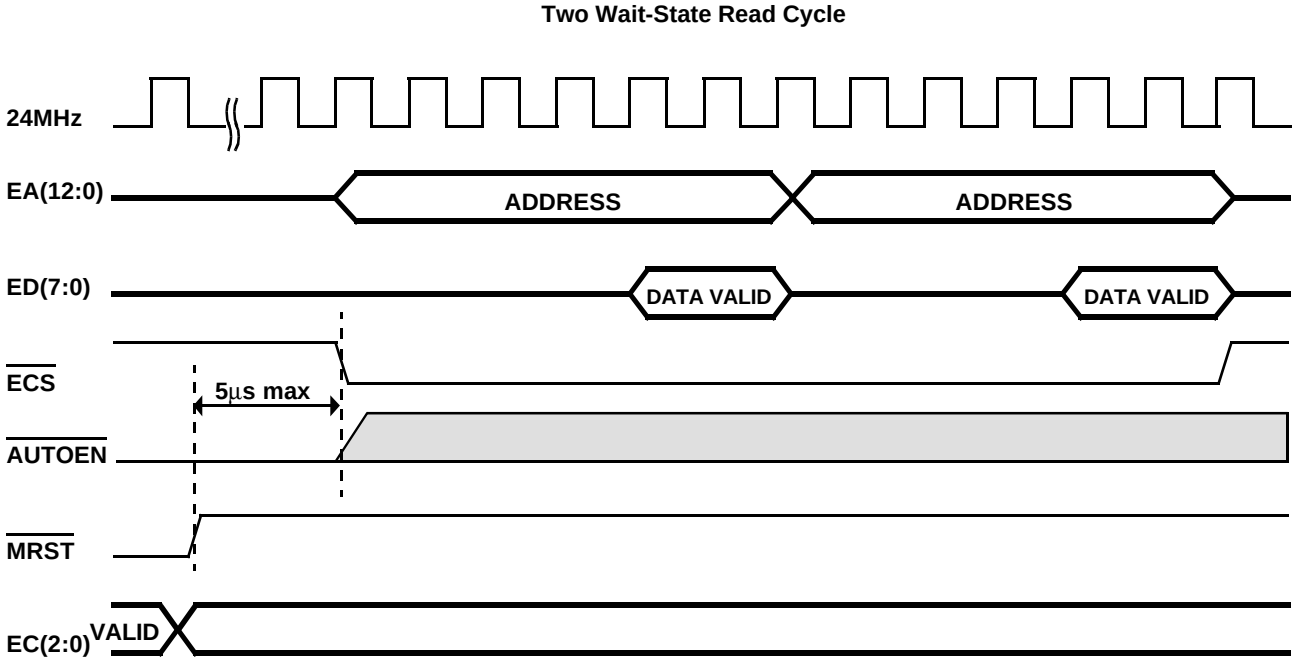


Figure 11b. Auto-Initialization Read Cycle

6.0 Testability

The following section reviews the built-in test capabilities of the SμMMIT RTE. Table 10 is a list of the various components that comprehend the SμMMIT RTE.

Table 10. SμMMIT RTE Internal Component List

Product	Protocol Die	Transceivers
SμMMIT RTE	Yes	Yes

Table 11 reviews the various BIT initiation sequences and the components that the sequence tests along with BIT execution times.

Table 11. BIT Initiation

Initiation Type	Protocol Die	Transceivers[1]	Execution Time[2]
CPU Initiated	Yes	No	70mS
Mode Code Initiated	Yes	No	70mS
Op-Code Initiated	Yes	No	70mS

Notes:

1. The transceiver is tested with the data wrap-around feature of the SμMMIT RTE. See sections 2.1.5.
2. Control Register write of 4000_{16}. Before initiating memory test, reset the SμMMIT RTE by asserting $\overline{\text{MRST}}$.

7.0 System Configuration

7.1 Register Transfers

The host's or subsystem's access to the SµMMIT RTE internal registers is similar to its access to RAM. After gaining control of the memory bus, the host supplies address information to bidirectional address bus pins A(4:0). After supplying the address information, the host asserts SµMMIT RTE inputs $\overline{CS}$ and RD/$\overline{WR}$ to designate a register access and the type of access. The memory access terminates on the negation of $\overline{CS}$. For more information on register cycles refer to the timing diagrams and AC electrical specifications in section 20. For register utilization versus mode of operation see Table 12.

Table 12. Internal Register Utilization

Register Number	Register Number 8-Bit Mode	Register Name
0	0,1	Control
1	2,3	Operational Status
2	4,5	Current Command
3	6,7	Interrupt Mask
4	8,9	Pending Interrupt
5	A,B	Interrupt Log List
6	C,D	BIT Word
7	E,F	Time Tag
8	10,11	SRT Descriptor Pointer
9	12,13	1553 Status Word Bits
A	14,15	N/A
B	16,17	N/A
C	18,19	N/A
D	1A,1B	N/A
E	1C,1D	N/A
F	1E,1F	N/A
10 to 1F	20 to 3F	Illegalization (16)
		Total 26

7.2 SμMMIT RTE

The SμMMIT RTE supplies hardware designers with a flexible interface to meet the needs of state-of-the-art MIL-STD-1553 interfaces. The SμMMIT RTE contains internal SRAM and a memory management unit, interfaces to either 8-bit or 16-bit subsystems, supports multiplexed and non-multiplexed interfaces, and has user selectable control signals.

7.2.1 Internal Registers

The SμMMIT RTE contains 32 internal registers that control and report on message activity and operation. The 32 registers are memory mapped into the subsystem memory. Table 13 reviews the registers and identifies the mode of operation applicable. The host reads or writes these registers using the timing diagrams shown in figures 12 a-d.

7.2.2 Memory Map

The SμMMIT RTE contains 64Kbits of memory for message storage and system data storage. MSEL(5) determines the organization of the memory as either by 16 or by 8. When organized by 16 (i.e., MSEL(5) = 0) the SμMMIT RTE' s internal memory looks like 4K x 16 of SRAM. For by 8 applications (MSEL(5) = 1) the SμMMIT RTE's internal memory looks like 8K x 8 of SRAM. The host reads or writes SRAM using the timing diagrams shown in figures 12 a-d. Table 13 shows the memory organization for either 8-bit or 16-bit operation.

7.2.3 Buffer Mode Operation

For the SμMMIT RTE operation, disable buffer mode, i.e, control register bit 6 = Logic 0.

7.2.4 Hardware Interface

The SμMMIT RTE offers hardware designers a flexible interface to commonly found embedded computers. The hardware designer selects control signals, bus widths, and bus functionality (i.e., non-multiplexed versus multiplexed) to meet their interface requirements. Table 14 reviews how the user selects the SμMMIT RTE's operation that best meets their interface requirements.

Figures 13 a-d show typical system interfaces and use of the mode select inputs to configure the SμMMIT RTE to interface to various embedded computers.

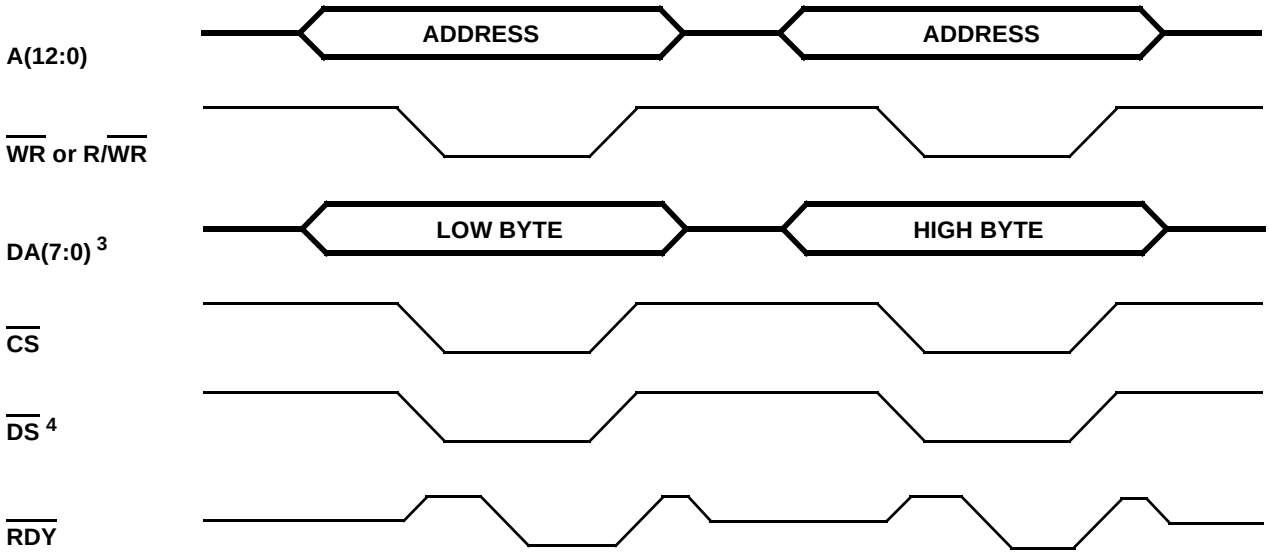
Table 13. Memory Organization

Mode	Memory Organization	Register Location	Memory Range
8-bit	8K x 8	0000 (hex) to 003F (hex)	0040 (hex) to 1FFF (hex)
16-bit	4K x 16	0000 (hex) to 001F (hex)	0020 (hex) to 0FFF (hex)

Table 14. User-Selectable Control Signals

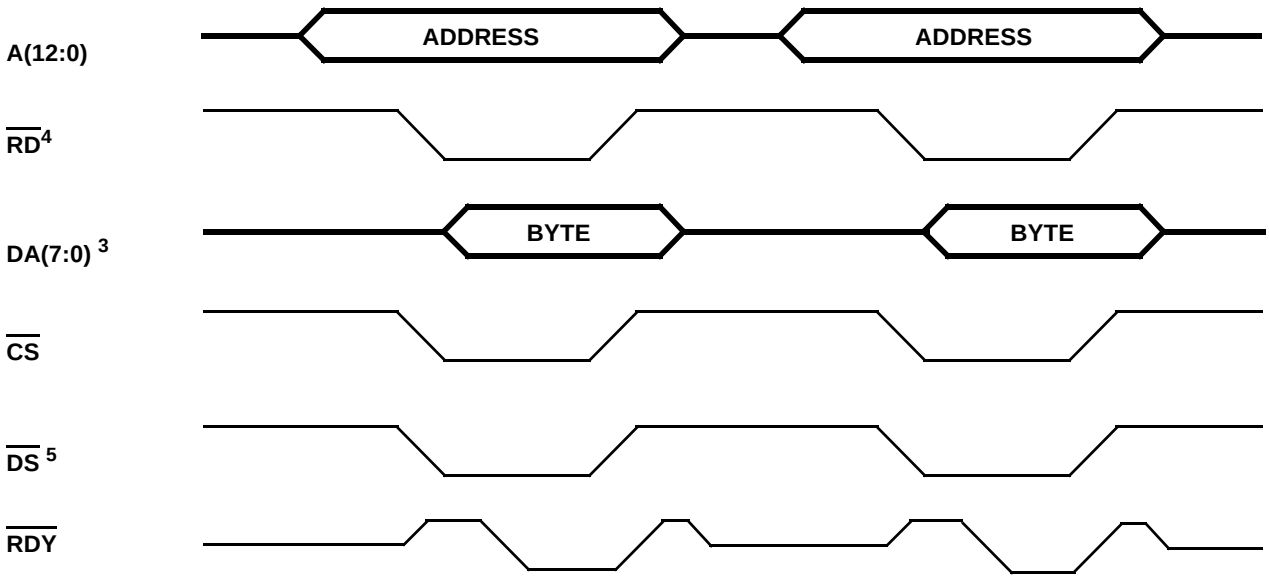
Function	Input Pin	Logic 1	Logic 0
Control Signal Select	MSEL(2)	R/$\overline{WR}$, $\overline{CS}$, $\overline{DS}$, $\overline{RDY}$	$\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RDY}$, $\overline{DS}$
Bus Functionality Select	MSEL(3)	Non-Multiplexed Address and Data	Multiplexed Address and Data, ALE
Interrupt Select	MSEL(4)	Level ($\overline{YF\_INT}$, $\overline{MSG\_INT}$, $\overline{YF\_ACK}$, and $\overline{MSG\_ACK}$)	Pulse ($\overline{YF\_INT}$ and $\overline{MSG\_INT}$)
Bus Width Select	MSEL(5)	8-bit	16-bit

Non-Multiplexed Memory/Register Write Access (8-bit Mode)[1, 2]



Notes:
1. ALE must be tied high.
2. Latter assertions of $\overline{CS}$, $\overline{DS}$, $\overline{WR}$ or R/$\overline{WR}$ starts cycle.
3. Tie DA(15:8) to V_{SS} via a 10K Ω resistor.
4. $\overline{DS}$ asserts to signal that data is valid on the bus.

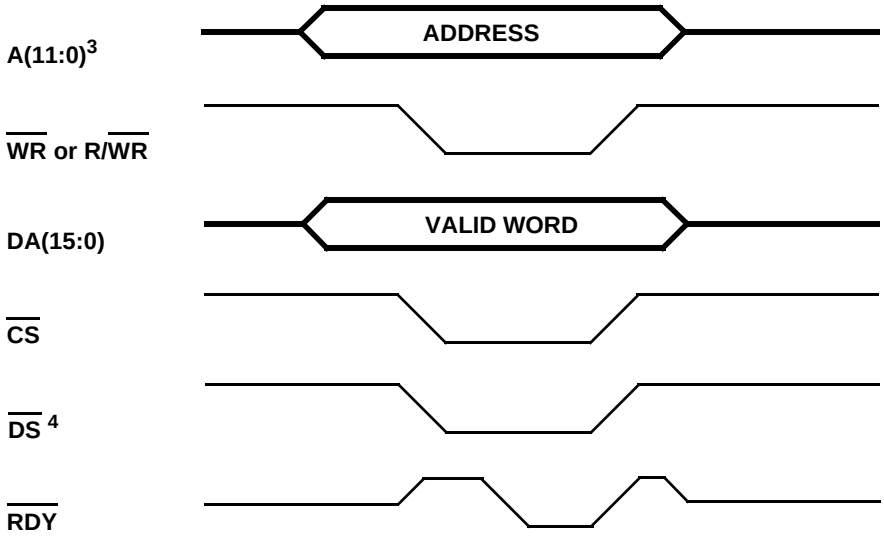
Non-Multiplexed Memory/Register Read Access (8-bit Mode)[1,2]



Notes:
1. ALE must be tied high.
2. Latter assertions of $\overline{CS}$, $\overline{DS}$, $\overline{WR}$ starts cycle.
3. Tie DA(15:8) to V_{SS} via a 10K Ω resistor.
4. When using R/$\overline{WR}$ as an input signal, tie RD to a logical one. During the read cycle R/$\overline{WR}$ remains logical one.
5. $\overline{DS}$ asserts to signal the SµMMIT RTE to place data on the bus.

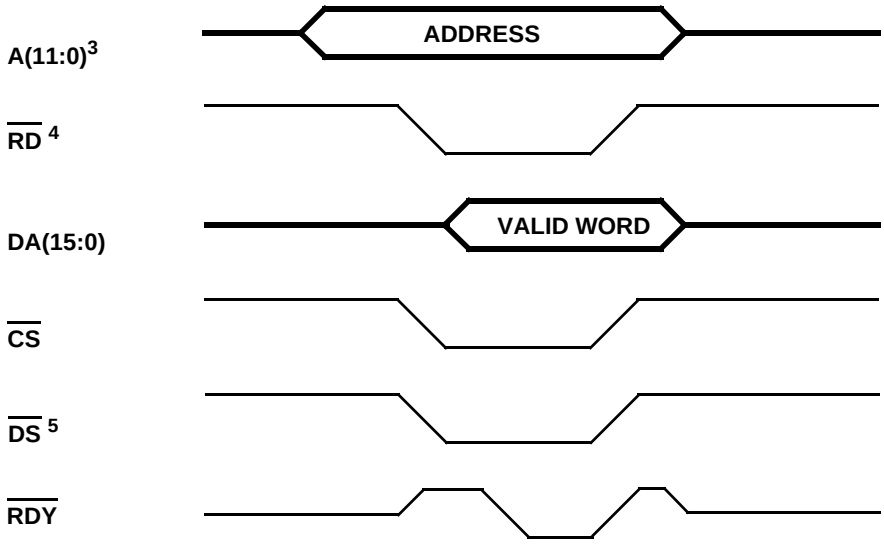
Figure 12a. 8-bit Memory and Register Access

Non-Multiplexed Memory/Register Write Access (16-bit Mode)[1, 2]



Notes:
1. ALE must be tied high.
2. Latter assertions of $\overline{CS}$, $\overline{DS}$, $\overline{WR}$ or R/$\overline{WR}$ starts cycle.
3. A15-A12 must be tied low.
4. $\overline{DS}$ asserts to signal that data is valid on the bus.

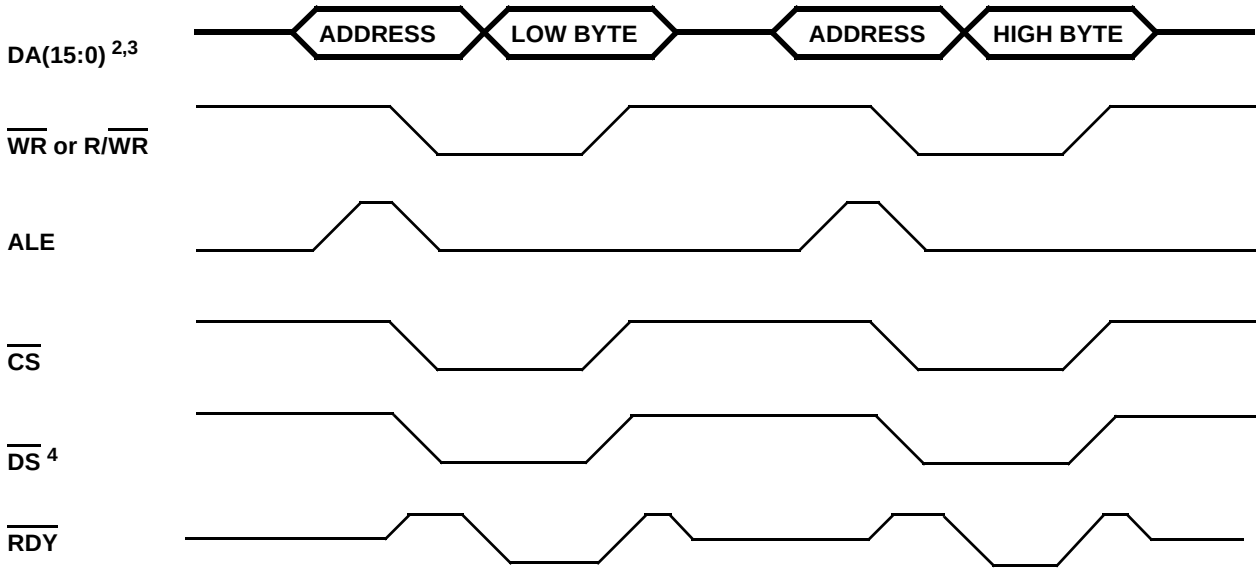
Non-Multiplexed Memory/Register Read Access (16-bit Mode)[1,2]



Notes:
1. ALE must be tied high.
2. Latter assertion of $\overline{CS}$, $\overline{DS}$, $\overline{RD}$ starts cycle.
3. A15-A12 must be tied low.
4. $\overline{DS}$ asserts to signal the SµMMIT RTE to place data on the bus.
5. When using R/$\overline{WR}$ as an input signal, tie RD to a logical one. During the read cycle R/$\overline{WR}$ remains logical one.

Figure 12b. 16-bit Memory and Register Access

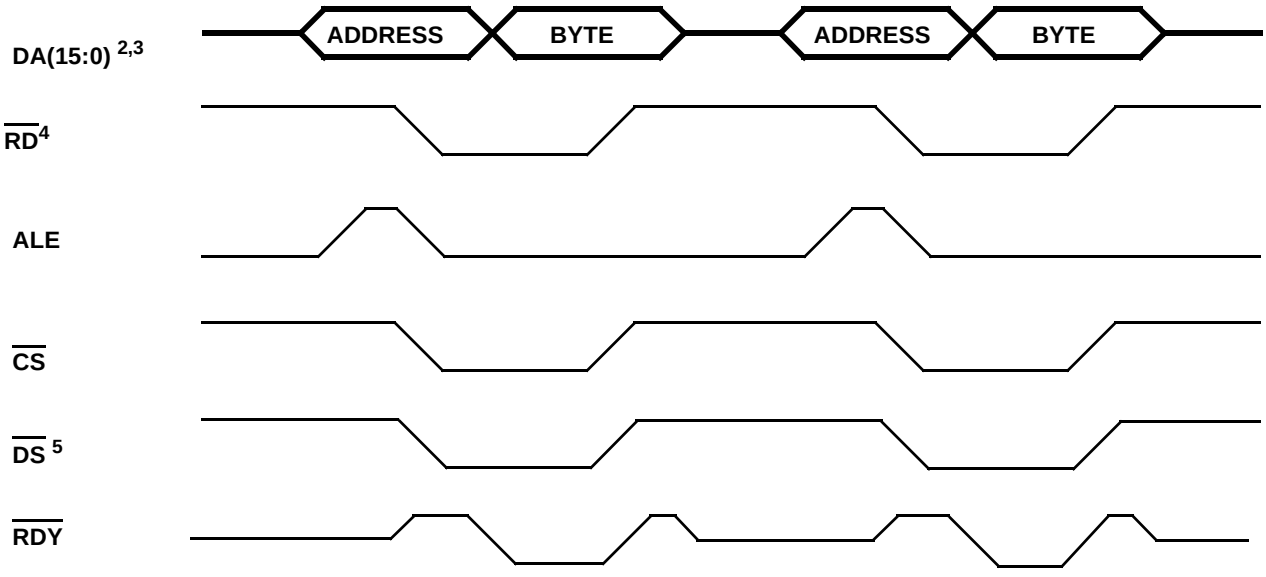
Multiplexed Memory/Register Write Access (8-bit Mode)[1]



Notes:

1. Latter assertion of $\overline{CS}$, $\overline{DS}$, $\overline{WR}$ or R/$\overline{WR}$ starts cycle.
2. For multiplexed address and data interfaces ALE latches the address into the SµMMIT RTE. Data is applied to inputs DA(7:0), tie A(15:0) to either a logical one or zero.
3. Tie DA(15:8) to V_{SS} via a 10K Ω resistor.
4. $\overline{DS}$ asserts to signal that data is valid on the bus.

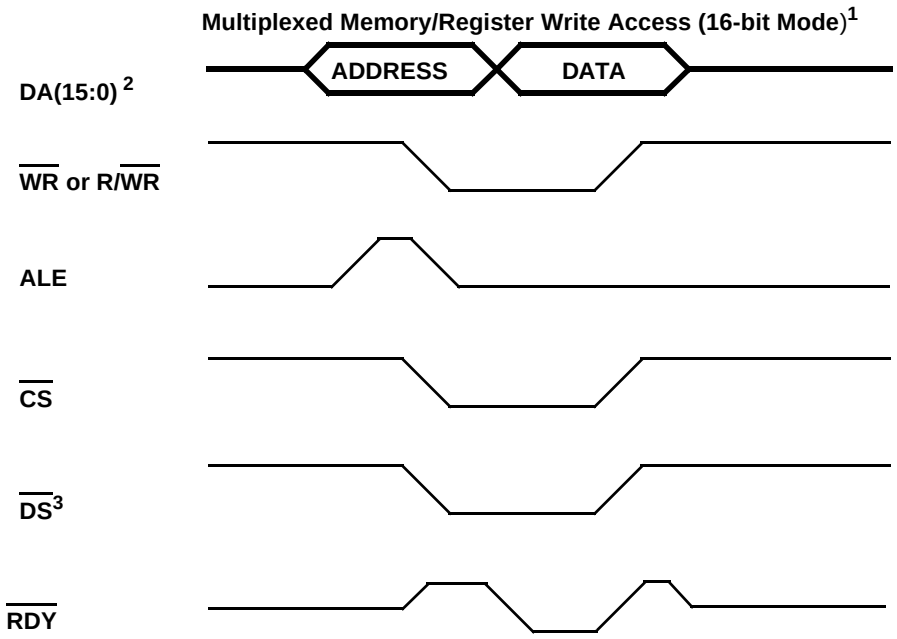
Multiplexed Memory/Register Read Access (8-bit Mode)[1]



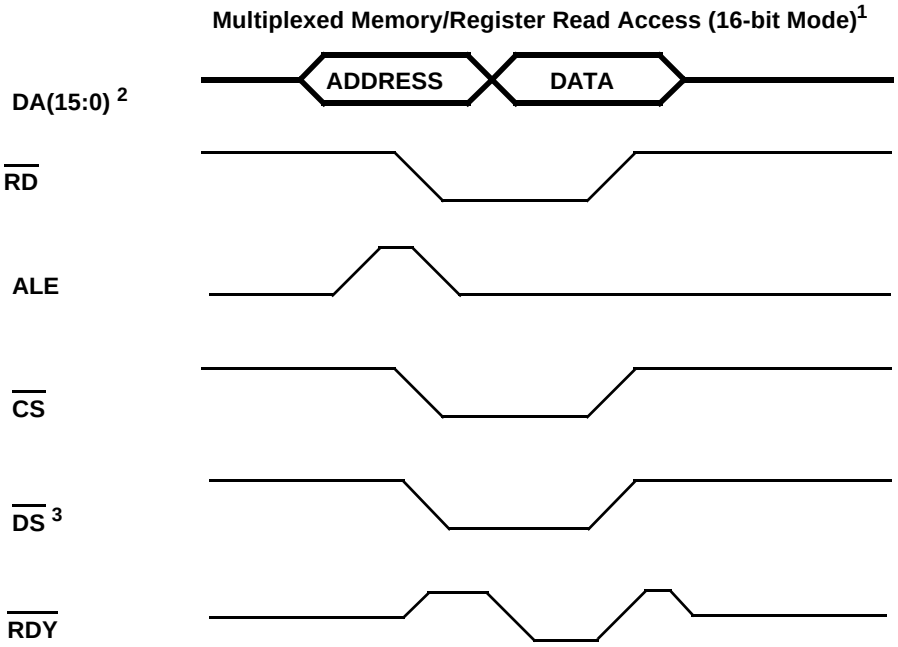
Notes:

1. Latter assertion of $\overline{CS}$, $\overline{DS}$, $\overline{RD}$ starts cycle.
2. For multiplexed address and data interfaces ALE latches the address into the SµMMIT RTE. Data is read from outputs DA(7:0), tie A(15:0) to either a logical one or zero.
3. Tie DA(15:8) to V_{SS} via a 10K Ω resistor.
4. When using R/$\overline{WR}$ as an input signal, tie RD to a logical one. During the read cycle R/$\overline{WR}$ remains logical one.
5. $\overline{DS}$ asserts to signal the SµMMIT RTE to place data on the bus.

Figure 12c. Multiplexed 8-bit Memory and Register Access



Notes:
1. Latter assertion of $\overline{CS}$, $\overline{DS}$, $\overline{WR}$ or R/$\overline{WR}$ starts memory cycle.
2. For multiplexed address and data interfaces ALE latches the address into the SμMMIT RTE. Data is applied to inputs DA(15:0), tie A(15:0) to either a logical one or zero.
3. $\overline{DS}$ asserts to signal that data is valid on the bus.



Notes:

1. Latter assertion of $\overline{CS}$, $\overline{DS}$, $\overline{RD}$ starts memory cycle.
2. For multiplexed address and data interfaces ALE latches the address into the SμMMIT RTE. Data is read from outputs DA(15:0), tie A(15:0) to either a logical one or zero.
3. $\overline{DS}$ asserts to signal the SμMMIT RTE to place data on the bus.

Figure 12d. Multiplexed 16-bit Memory and Register Access

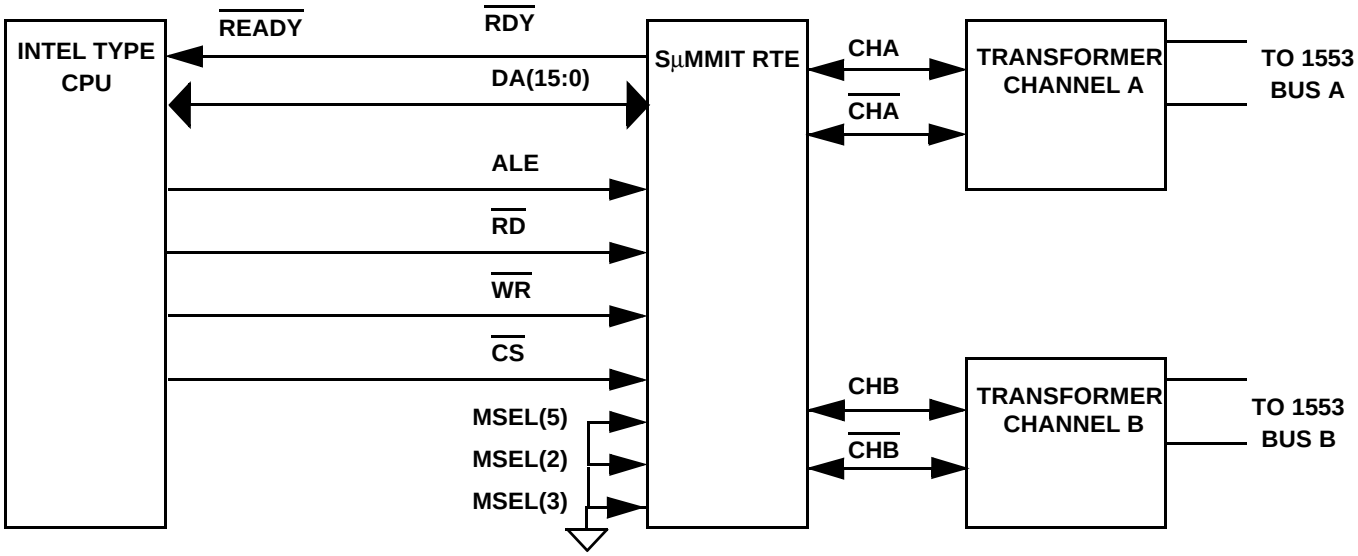


Figure 13a. 16-bit Interface (Intel Type)

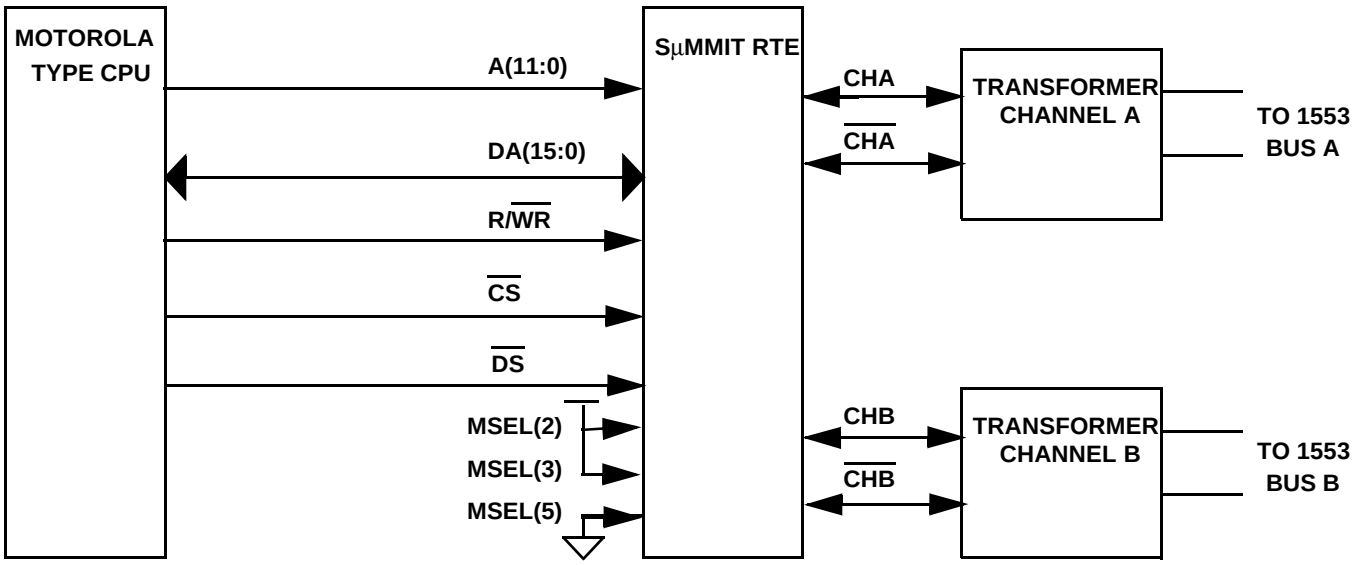


Figure 13b. 16-bit Interface (Motorola Type)

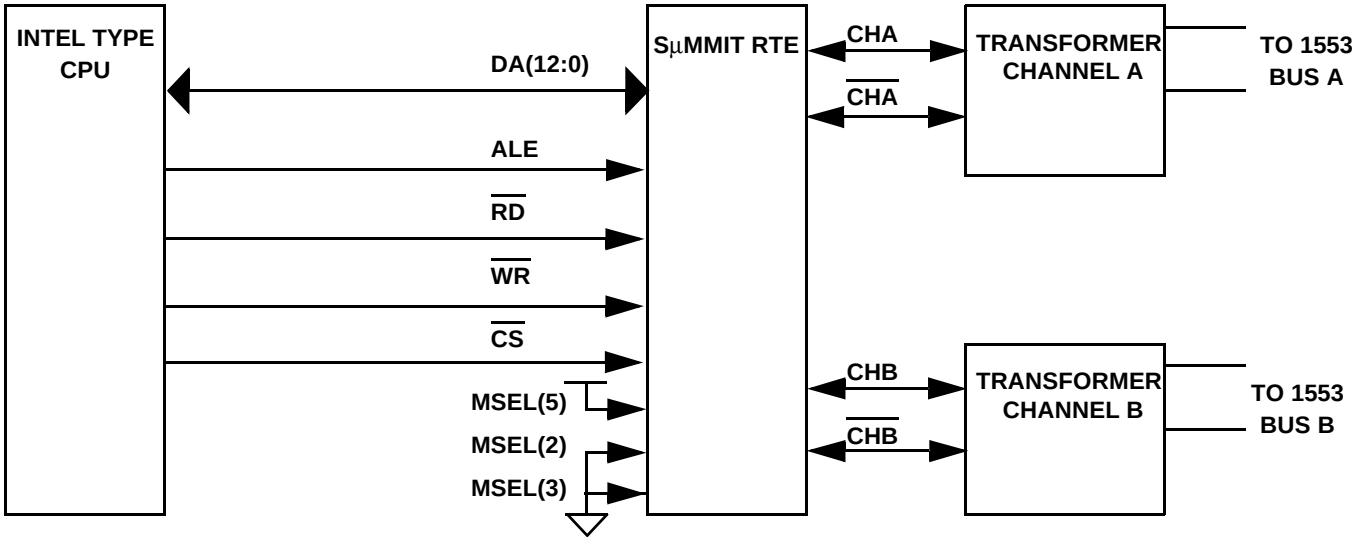


Figure 13c. 8-bit Interface (Intel Type)

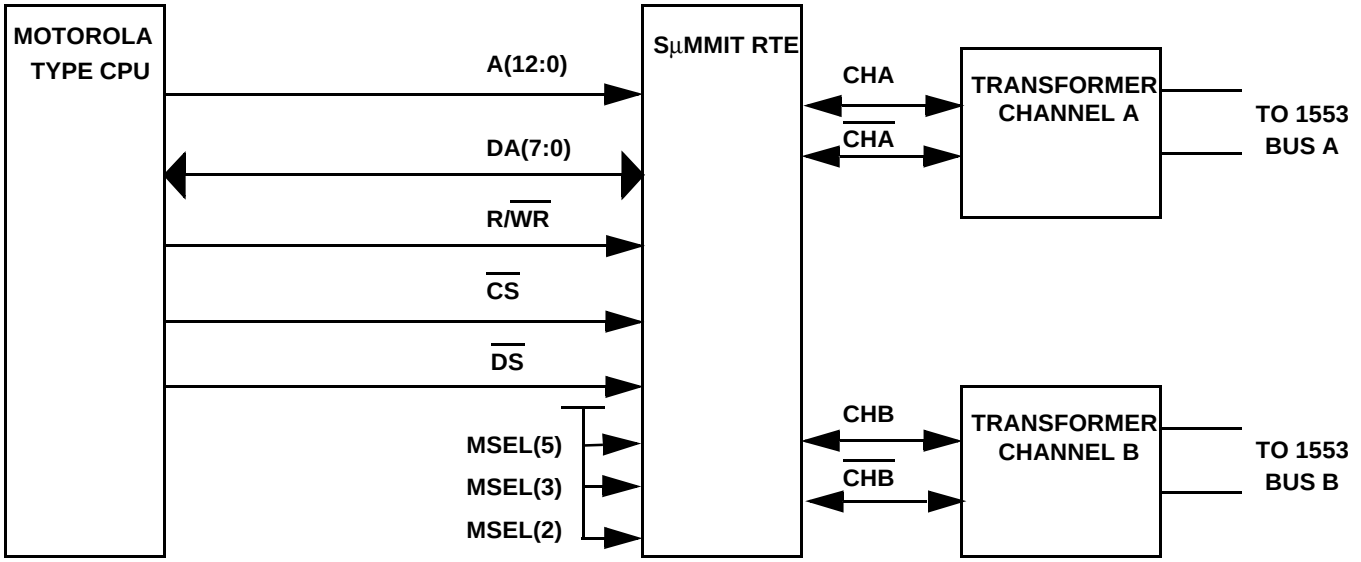


Figure 13d. 8-bit Interface (Motorola Type)

8.0 SERIAL DATA BUS INTERFACE

The SµMMIT RTE Manchester encoder/decoder interfaces directly to the MIL-STD-1553 bus via transformers, using CHA-$\overline{\text{CHA}}$ and CHB-$\overline{\text{CHB}}$. The designer can connect the SµMMIT RTE to the data bus via a short-stub (direct-coupling) connection or a long-stub (transformer-coupling) connection. Use a short-stub connection when the distance from the isolation transformer to the data bus does not exceed a one-foot maximum. Use a long-stub connection when the distance from the isolation transformer exceeds the one-foot maximum and is less than twenty feet. Figure 14 shows an example of a bus coupling configuration. The SµMMIT RTE is designed to function with MIL-STD-1553A and 1553B compatible transformers.

8.1 Transmitter

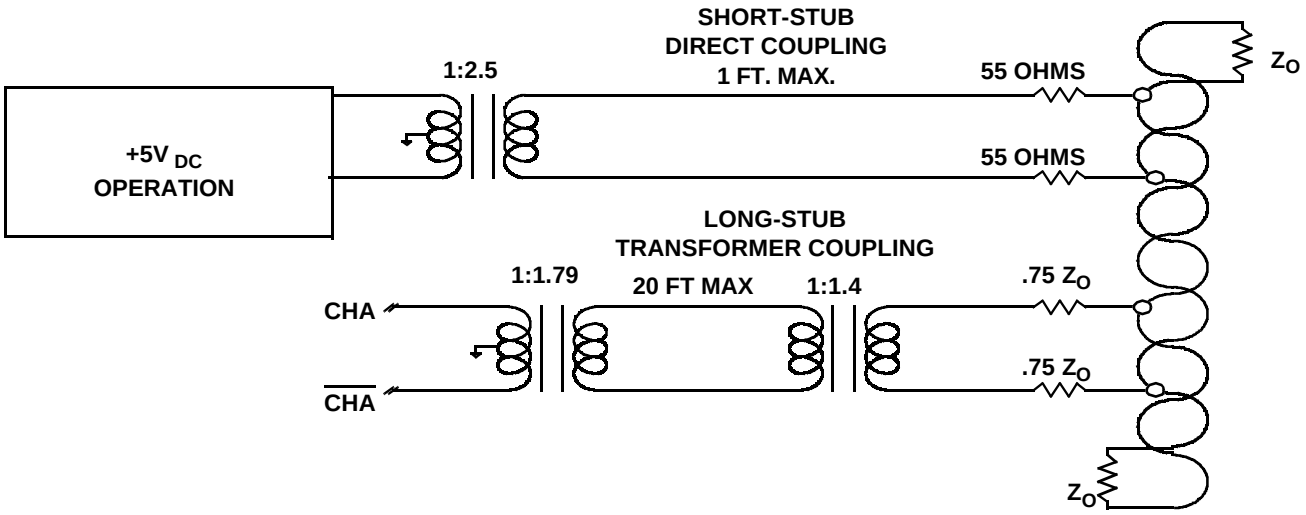
The transmitter section accepts Manchester II biphase TTL data and converts this data into differential phase-modulated current drive. Transmitter current drivers are coupled to a MIL-STD-1553 data bus via a transformer driven from the CHA (CHB) and $\overline{\text{CHA}}$ ($\overline{\text{CHB}}$) terminals. The SµMMIT RTE internally generates a signal to the transceiver for the MIL-STD-1553 fail-safe timer requirement.

8.2 Receiver

The receiver section accepts biphase differential data from a MIL-STD-1553 data bus at its CHA (CHB) and $\overline{\text{CHA}}$ ($\overline{\text{CHB}}$) inputs. The receiver converts input data to biphase Manchester II TTL format at internal RXOUT and $\overline{\text{RXOUT}}$ terminals. The internal outputs RXOUT and $\overline{\text{RXOUT}}$ represent positive and negative excursions (respectively) of the inputs CHA (CHB) and $\overline{\text{CHA}}$ ($\overline{\text{CHB}}$).

8.3 Recommended Thermal Protection

All packages should mount to or contact a heat removal rail located in the printed circuit board. To insure proper heat transfer between the package and the heat removal rail, use a thermally-conductive material between the package and the heat removal rail. Use a material such as Mereco XLN-589 or equivalent to insure heat transfer between the package and heat removal rail.



Note:
Z_O defined per MIL-STD-1553B in section 4.5.1.5.2.1.

Figure 14. SμMMIT RTE Bus Coupling Configuration

Table 15. Transformer Requirements Versus Power Supplies

COUPLING TECHNIQUE	$+5V_{DC}$
DIRECT-COUPLED: Isolation	1:2.5
TRANSFORMER-COUPLED: Isolation Transformer Ratio	1:1.79
Coupling Transformer Ratio	1:1.4

9.0 SμMMIT RTE PIN IDENTIFICATION AND DESCRIPTION

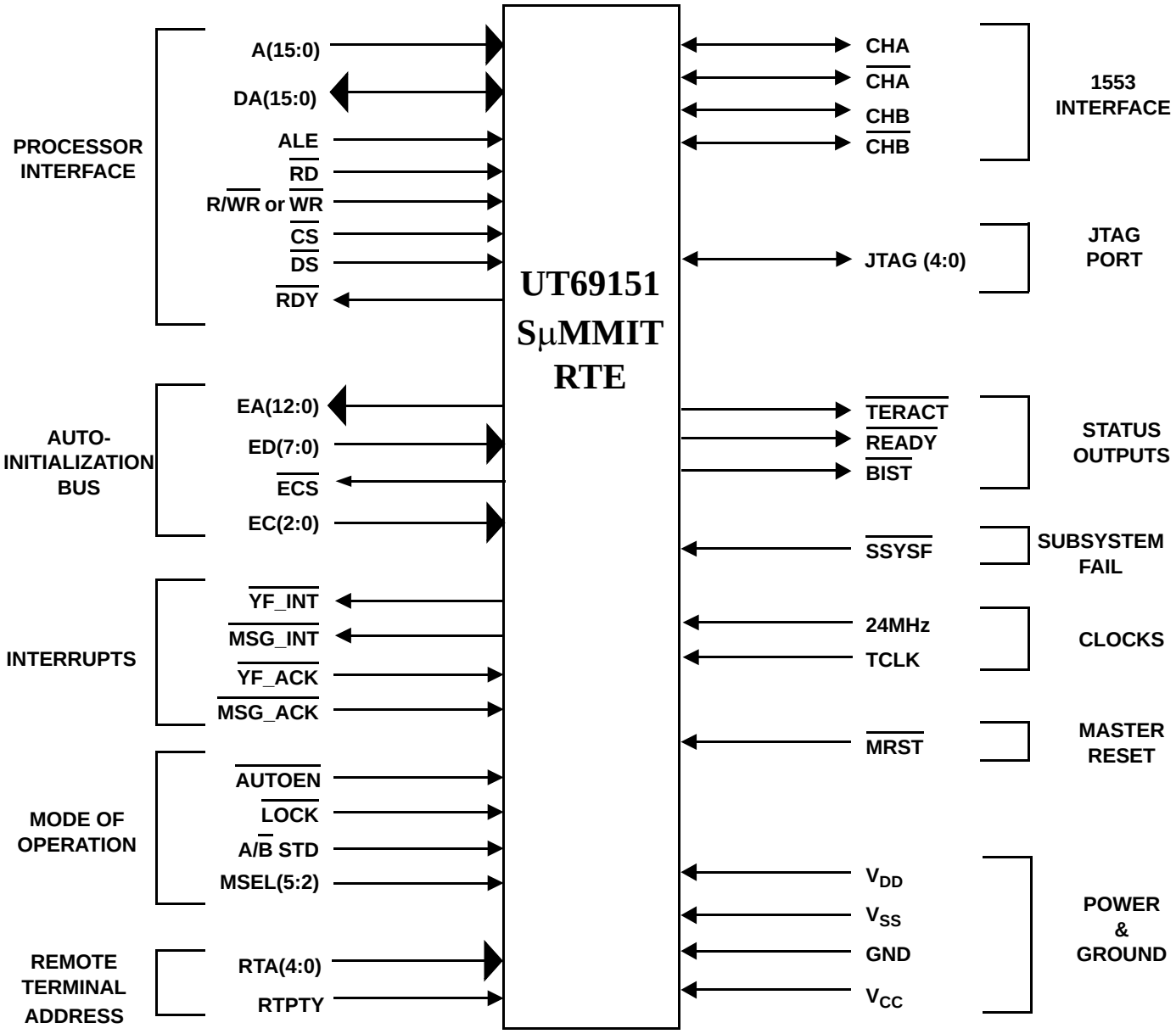


Figure 15. SμMMIT RTE Functional Pin Diagram

9.1 SμMMIT RTE Functional Pin Description

Legend for TYPE and ACTIVE fields:
TO = TTL output
TTB = Three-state TTL bidirectional
CI = CMOS input
TUI = TTL input (internally pulled high)
AH = Active high
AL = Active low
TI = TTL input
TTO = Three-state TTL output
PGA = Pingrid Array
FP = Flatpack
DIO = Differential input/output

9.1.1 Data Bus DA (15:0)

Bit Number	Type	Active	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
15	TTB	--	128	17	N11	Bit 15 (MSB) of the bidirectional Data bus.
14	TTB	--	1	18	L10	Bit 14 of the bidirectional Data bus.
13	TTB	--	2	19	M11	Bit 13 of the bidirectional Data bus.
12	TTB	--	3	20	L11	Bit 12 of the bidirectional Data bus.
11	TTB	--	5	21	N12	Bit 11 of the bidirectional Data bus.
10	TTB	--	11	22	M12	Bit 10 of the bidirectional Data bus.
9	TTB	--	12	23	L12	Bit 9 of the bidirectional Data bus.
8	TTB	--	16	24	L13	Bit 8 of the bidirectional Data bus.
7	TTB	--	17	25	M13	Bit 7 of the bidirectional Data bus.
6	TTB	--	24	26	L14	Bit 6 of the bidirectional Data bus.
5	TTB	--	19	28	K11	Bit 5 of the bidirectional Data bus.
4	TTB	--	26	29	K13	Bit 4 of the bidirectional Data bus.
3	TTB	--	29	30	K12	Bit 3 of the bidirectional Data bus.
2	TTB	--	31	31	J11	Bit 2 of the bidirectional Data bus.
1	TTB	--	38	32	J12	Bit 1 of the bidirectional Data bus.
0	TTB	--	37	33	J13	Bit 0 (LSB) of the bidirectional Data bus.

9.1.2 Address Bus A(15:0)

Bit Number	Type	Active	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
15	TI	--	105	38	J14	Always drive logic zero.
14	TI	--	106	39	H11	Always drive logic zero.
13	TI	--	107	40	H12	Always drive logic zero.
12	TI	--	108	41	H13	Drive to logic zero if 16-bit mode.
11	TI	--	111	42	G11	Bit 11 of the Address bus.
10	TI	--	112	43	G12	Bit 10 of the Address bus.
9	TI	--	113	45	G13	Bit 9 of the Address bus.
8	TI	--	114	46	G14	Bit 8 of the Address bus.
7	TI	--	117	47	F11	Bit 7 of the Address bus.
6	TI	--	118	48	F12	Bit 6 of the Address bus.
5	TI	--	119	49	F13	Bit 5 of the Address bus.
4	TI	--	120	50	D13	Bit 4 of the Address bus.
3	TI	--	123	51	E13	Bit 3 of the Address bus.
2	TI	--	124	52	C13	Bit 2 of the Address bus.
1	TI	--	125	54	E14	Bit 1 of the Address bus.
0	TI	--	126	55	C14	Bit 0 (LSB) of the Address bus.

9.1.3 Auto-initialization Address Bus EA(12:0)

Bit Number	Type	Active	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
12	TO	--	35	85	F9	Bit 12 (MSB) of the auto-init Address bus.
11	TO	--	34	84	F10	Bit 11 of the auto-init Address bus.
10	TO	--	36	83	G10	Bit 10 of the auto-init Address bus.
9	TO	--	46	82	C11	Bit 9 of the auto-init Address bus.
8	TO	--	47	81	G9	Bit 8 of the auto-init Address bus.
7	TO	--	48	80	E11	Bit 7 of the auto-init Address bus.
6	TO	--	49	79	E10	Bit 6 of the auto-init Address bus.
5	TO	--	50	78	E9	Bit 5 of the auto-init Address bus.
4	TO	--	51	77	G8	Bit 4 of the auto-init Address bus.
3	TO	--	52	76	H8	Bit 3 of the auto-init Address bus.
2	TO	--	54	75	J7	Bit 2 of the auto-init Address bus.
1	TO	--	55	74	J9	Bit 1 of the auto-init Address bus.
0	TO	--	62	73	J10	Bit 0 (LSB) of the auto-init Address bus.

9.1.4 Auto-initialization Data Bus ED(7:0)

Bit Number	Type	Active	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
7	TUI	--	20	68	K10	Bit 7 (MSB) of the auto-init data.
6	TUI	--	18	67	M7	Bit 6 of the auto-init data.
5	TUI	--	22	66	N3	Bit 5 of the auto-init data.
4	TUI	--	21	65	N8	Bit 4 of the auto-init data.
3	TUI	--	25	64	M8	Bit 3 of the auto-init data.
2	TUI	--	30	63	L8	Bit 2 of the auto-init data.
1	TUI	--	27	62	N9	Bit 1 of the auto-init data.
0	TUI	--	32	61	M9	Bit 0 (LSB) of the auto-init data.

9.1.5 Remote Terminal Address Inputs

Name	Type	Active	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
RTA4	TUI	--	75	115	E2	Remote Terminal Address 4. This is the most significant bit for the RT address.
RTA3	TUI	--	76	116	G3	Remote Terminal Address 3. This is bit 3 of the RT address.
RTA2	TUI	--	78	117	F3	Remote Terminal Address 2. This is bit 2 of the RT address.
RTA1	TUI	--	79	118	G2	Remote Terminal Address 1. This is bit 1 of the RT address.
RTA0	TUI	--	73	119	F2	Remote Terminal Address 0. This input is the least significant bit of the RT address.
RTPTY	TUI	--	70	120	G1	Remote Terminal Parity. This is an odd parity input for the RT address.

9.1.6 JTAG Testability Pins

Name	Type	Active	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
TDO	TTO	--	96	134	K3	TDO. This input performs the operation of Test Data Output as defined in IEEE Standard 1149.1.
TDI	TUI	--	90	135	K2	TDI. This input performs the operation of Test Data Input as defined in IEEE Standard 1149.1.
TMS	TUI	--	97	136	J2	TMS. This input performs the operation of Test Mode Select as defined in IEEE Standard 1149.1.
TCK	TUI	--	91	137	L2	TCK. This input performs the operation of Test Clock as defined in IEEE Standard 1149.1.
$\overline{\text{TRST}}$	TUI	AL	89	133	L3	$\overline{\text{TRST}}$. This input provides the RESET to the TAP controller as defined in the IEEE Standard 1149.1. This non-inverting input buffer is optimized for driving TTL input levels. When not exercising JTAG, tie $\overline{\text{TRST}}$ to a logical 0.

9.1.7 Biphase Inputs/Outputs

Name	Type	Active	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
CHA	DIO	--	40, 41	92	B7	Channel A (True). This is the Manchester-encoded true signal for Channel A.
$\overline{\text{CHA}}$	DIO	--	42, 43	93	A7	Channel A (Complement). This is the Manchester-encoded complement signal for Channel A.
CHB	DIO	--	57, 58	102	A3	Channel B (True). This is the Manchester-encoded true signal for Channel B.
$\overline{\text{CHB}}$	DIO	--	59, 60	103	A2	Channel B (Complement). This is the Manchester-encoded complement signal for Channel B.

9.1.8 Control Signals

Name	Type	Active	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
$\overline{CS}$	TI	AL	104	14	A10	Chip Select. This pin selects the SμMMIT RTE's internal memory and registers.
$\overline{DS}$	TI	AL	85	12	A12	Data Strobe. During a write cycle, assert $\overline{DS}$ to indicate that data is valid on the data bus. During a read cycle assert $\overline{DS}$ to signal the SμMMIT RTE to drive the data bus.
$\overline{RD}$	TI	AL	84	10	K8	Read Strobe. During a read cycle, assert $\overline{RD}$ to signal the SμMMIT RTE to drive the data bus.
R/$\overline{WR}$ or $\overline{WR}$	TI	--	103	11	K7	Read/Write or Write Strobe. During a write cycle assert $\overline{WR}$ to signal the SμMMIT RTE that data is valid on the data bus. R/$\overline{WR}$ indicates the direction of data flow with respect to the SμMMIT RTE. R/$\overline{WR}$ high indicates the SμMMIT RTE will drive the data bus. R/$\overline{WR}$ low indicates an outside source will drive the data bus.
MSEL(5)	TUI	--	63	124	D12	Mode Select 5. A logical zero enables the SμMMIT RTE's 16-bit interface. A logical one enables the 8-bit interface. Latched on the rising edge of $\overline{MRST}$.
MSEL(4)	TUI	--	66	125	B13	Mode Select 4. A logical zero enables a pulsed interrupt output. A logical one enables a level interrupt output. Latched on the rising edge of $\overline{MRST}$.
MSEL(3)	TUI	--	71	126	C12	Mode Select 3. A logical zero enables the SμMMIT RTE's multiplexed address and data bus interface. A logical one enables the non-multiplexed interface. Latched on the rising edge of $\overline{MRST}$.
MSEL(2)	TUI	--	67	127	A11	Mode Select 2. A logical zero selects control signals $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{DS}$, and $\overline{RDY}$. A logical one selects control signals R/$\overline{WR}$, $\overline{CS}$, $\overline{DS}$, and $\overline{RDY}$. Latched on the rising edge of $\overline{MRST}$.
EC(2)	TUI	--	8	97	B10	Latched on the rising edge of $\overline{MRST}$ this input sizes the auto-initialization cycle.
EC(1)	TUI	--	9	98	D11	Latched on the rising edge of $\overline{MRST}$ this input sizes the auto-initialization cycle.
EC(0)	TUI	--	10	99	B12	Latched on the rising edge of $\overline{MRST}$ this input sizes the auto-initialization cycle.

24 MHz	CI	--	115	7	N7	24 MHz Clock. The 24MHz input clock requires a 50% ± 5% duty cycle with an accuracy of ± 0.01%.
$\overline{\text{MRST}}$	TUI	AL	88	130	J8	Master Reset. This input pin resets the internal encoder, decoder, all registers, and associated logic.
ALE	TI	AH	95	13	E12	Address Latch Enable. The falling edge of this strobe latches address information into the SμMMIT RTE when operating with a multiplexed address and data bus.
TCLK	TI	--	127	138	L7	Timer Clock. The internal timer is a 16-bit counter with a 64μs resolution when using the 24MHz input clock. For applications requiring a different resolution, the user may input a clock from 0 to 6MHz to establish the timer resolution. (Duty cycle equals 50% ± 10%).
A/$\overline{\text{B}}$ STD	TUI	--	81	122	H2	A/$\overline{\text{B}}$. Military Standard A or B. This pin defines whether the SμMMIT RTE operates per MIL-STD-1553A or MIL-STD-1553B. Input is latched on the rising edge of $\overline{\text{MRST}}$.
$\overline{\text{LOCK}}$	TUI	AL	80	121	H3	Lock. A logical zero applied to this pin prevents software from changing the RT address, A/$\overline{\text{B}}$ STD, or mode of operation. Input is latched on the rising edge of $\overline{\text{MRST}}$.
$\overline{\text{AUTOEN}}$	TUI	AL	102	131	M2	Auto Enable. When active this pin enables the SμMMIT RTE's auto-initialization function. Input is latched on the rising edge of $\overline{\text{MRST}}$.
$\overline{\text{YF\_ACK}}$	TUI	AL	129	3	H9	You Failed Interrupt Acknowledge. Assertion of this input resets interrupt output $\overline{\text{YF\_INT}}$ when operating in the level mode.
$\overline{\text{MSG\_ACK}}$	TUI	AL	130	5	K9	Message Interrupt Acknowledge. Assertion of this input resets interrupt output $\overline{\text{MSG\_INT}}$ when operating in the level mode.
$\overline{\text{SSYSF}}$	TUI	AL	68	113	D1	Subsystem Fail. Upon assertion, this signal propagates directly to the RT's 1553 Status Word.

9.1.9 Status Signals

Name	Type	Active	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
$\overline{\text{YF\_INT}}$	TTO[1]	AL	99	4	M3	You Failed Interrupt. This pin asserts upon the occurrence of interrupt events which are not masked. Either a level output or pulse output.
$\overline{\text{MSG\_INT}}$	TTO[1]	AL	98	6	L1	Message Interrupt. This pin asserts upon the occurrence of interrupt events which are not masked. Either a level output or pulse output.
$\overline{\text{READY}}$	TO	AL	65	110	D9	$\overline{\text{READY}}$. Assertion of this output indicates the SμMMIT RTE has completed initialization or BIT, and regular operation may begin.
$\overline{\text{ECS}}$	TO	AL	15	96	B11	Chip Select. Auto-initialization device select.
$\overline{\text{RDY}}$	TTO	AL	92	15	H10	Access Ready. Assertion of this output indicates that the host can complete the SμMMIT RTE access.
$\overline{\text{TERACT}}$	TO	AL	64	111	F7	$\overline{\text{TERACT}}$. This output indicates that the terminal is actively processing a 1553 command.
$\overline{\text{BIST}}$	TTO[1]	AL	4	114	D10	Built-In Test. Assertion of this output indicates the SμMMIT RTE is performing an internal memory test.

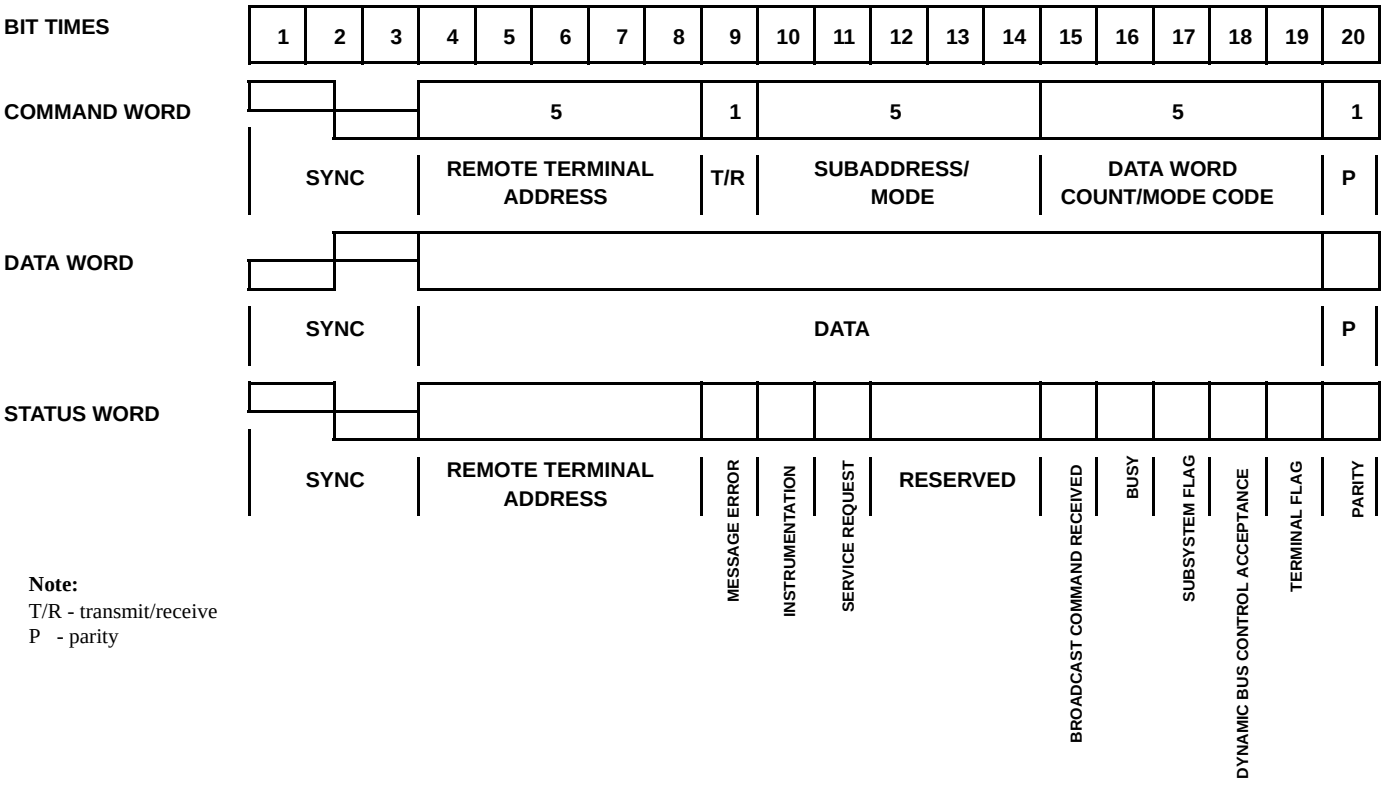
Note:
1. This output may tri-state and should be connected to V_{DD} through ane xternal bias resistor.

9.1.10 No Connects

Name	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
NC	--	8, 56, 59, 86, 91, 100, 104, 109	C2, D2, D7, D8, N10	No Connect

9.1.11 Power/Ground The following shows package location of all power and ground pins associated with the SµMMIT RTE.

Pin Number	Pin Number 132FP	Pin Number 140FP	Pin Number PGA	Description
V_{DD}	6, 13, 83, 86, 93, 100, 109, 121, 131	2 ,9, 16 ,34, 37, 44, 60, 69, 72, 129, 139	A8, B3, B14, F1, F14, G7, K1, J1, K14, N2, N13	+5 Volt Logic Power (±10%)
V_{CC}	CHA: 23, 28, 39, 44 CHB: 56, 61, 72, 77	CHA: 87, 94 CHB: 101, 107	CHA: C9, C10, E8 CHB: C1, D3, F8	+5 Volt Transceiver Power (±10%) Recommended de-coupling capacitors: 4.7µF and .1µF
V_{SS}	7, 14, 53, 82, 87, 94, 101, 110, 116, 122, 132	1, 27, 35, 36, 53 57, 58, 70, 71, 123, 128, 132, 140	A9, A13, B2, B8, D14, H1, H7, J3, H14, L9, M1, M10, M14	Digital Ground
GND	CHA: 33, 45 CHB: 69, 74	CHA: 88, 89, 90, 95 CHB: 105, 106, 108, 112	CHA: B9, C7, C8, E7 CHB: B1, C3, E1, E3	Transceiver Ground



Note:
T/R - transmit/receive
P - parity

Figure 16. MIL-STD-1553B Word Formats

10.0 SμMMIT RTE ABSOLUTE MAXIMUM RATINGS [1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMIT	UNIT
V_{DD}	Logic supply voltage	-0.3 to 7.0	V
P_D	Maximum power dissipation	5	W
V_{CC}	Transceiver supply voltage	-0.3 to 7.0	V
V_{DR}	Input voltage range (receiver)	10	$V_{P, L-L}$
$V_{I/O}$	Logic voltage on any pin	-.3 to V_{DD} +.3	V
I_I	Logic input current	±10	mA
I_O	Peak output current (transmitter)	1000	mA
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Maximum junction temperature	+150	°C
T_S	Lead temperature (soldering, 5 seconds)	+300	°C
T_C	Operating temperature case	-55 to + 125	°C
Θ_{JC}	Thermal resistance, junction-to-case [2]	7	°C/W

Note:

1. Stress outside the listed absolute maximum rating may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Mounting per MIL-STD-883, Method 1012.

11.0 SμMMIT RTE RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNIT
V_{CC}	Transceiver supply voltage range	4.5 to 5.5	V
V_{DD}	Logic supply voltage	4.5 to 5.5	V
V_{DR}	Receiver differential voltage	8.0	V_{P-P}
V_{IN}	Logic DC input voltage	0 to V_{DD}	V
V_{IC}	Receiver common mode input voltage range	±5.0	V
I_O	Driver peak output current	700	mA
S_D	Serial data rate	0 to 1	MHz
D_C	Clock Duty cycle	50 ± 5	%
T_C	Case operating temperature range	-55 to + 125	°C
F_{IN}	Operating frequency	24 ± .01%	MHz

12.0 SμMMIT RTE DC ELECTRICAL CHARACTERISTICS

12.1 SμMMIT RTE DC Electrical Characteristics

V_{DD} = 5.0V±10%
V_{CC} = 5.0V ± 10% (RTE5)

V_{SS} = 0V[1]
GND = 0V[1]
-55°C < T_C < +125°C

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}[1]	Low-level input voltage			.8	V
V_{IL}[2]	Low-level input voltage TCK input only			.7	V
V_{IH}	High-level input voltage		2.2		V
V_{ILC}	Low-level input voltage [2]			.3V_{DD}	V
V_{IHC}	High-level input voltage [2]		.7V_{DD}		V
I_{IN}	Input leakage current TTL driven inputs Inputs with pull-up resistors Inputs with pull-up resistors	V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS}	-10 -10 -167	+10 +10 -27	μA
V_{OL}	Low-level output voltage TTL output loads Single-drive buffer CMOS output loads[7]	 I_{OL} = 4.0mA I_{OL} = 1.0μA		 .4 0.05	V
V_{OH}	High-level output voltage TTL output loads Single-drive buffer CMOS output loads[7]	 I_{OH} = 4.0mA I_{OH} = 1.0μA	 2.4 V_{DD}-0.05		V
I_{OZ}	Three-state output leakage current TTL outputs loads Single-drive buffer	 V_O = V_{DD} or V_{SS}	 -10	 +10	μA
I_{OS}	Short-circuit output current [3,4] TTL output loads Single-drive buffer	V_{DD} = 5.5V, V_O = 0V V_{DD} = 5.5V, V_O = V_{DD}	 -100	 +100	mA
C_{IN}	Input capacitance [5]	*f* = 1MHz @ 0V		45	pF
C_{OUT}	Output capacitance [5] Single-drive buffer	*f* = 1MHz @ 0V		45	pF
C_{IO}	Bidirectional capacitance [5,6]	*f* = 1MHz @ 0V		45	pF

Notes:
1. Maximum allowable relative shift = 50mV.
2. CMOS input only.
3. Supplied as a design limit but not guaranteed or tested.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification or design changes which may affect the value.
6. For all pins except CHA, $\overline{\text{CHA}}$, CHB, and $\overline{\text{CHB}}$.
7. Guaranteed by design, not tested.

12.2 SμMMIT RTE Operating Current [1,2]

V_{DD} = 5.0V±10%
V_{CC} = 5.0V ±10%
V_{SS} = 0V[1]

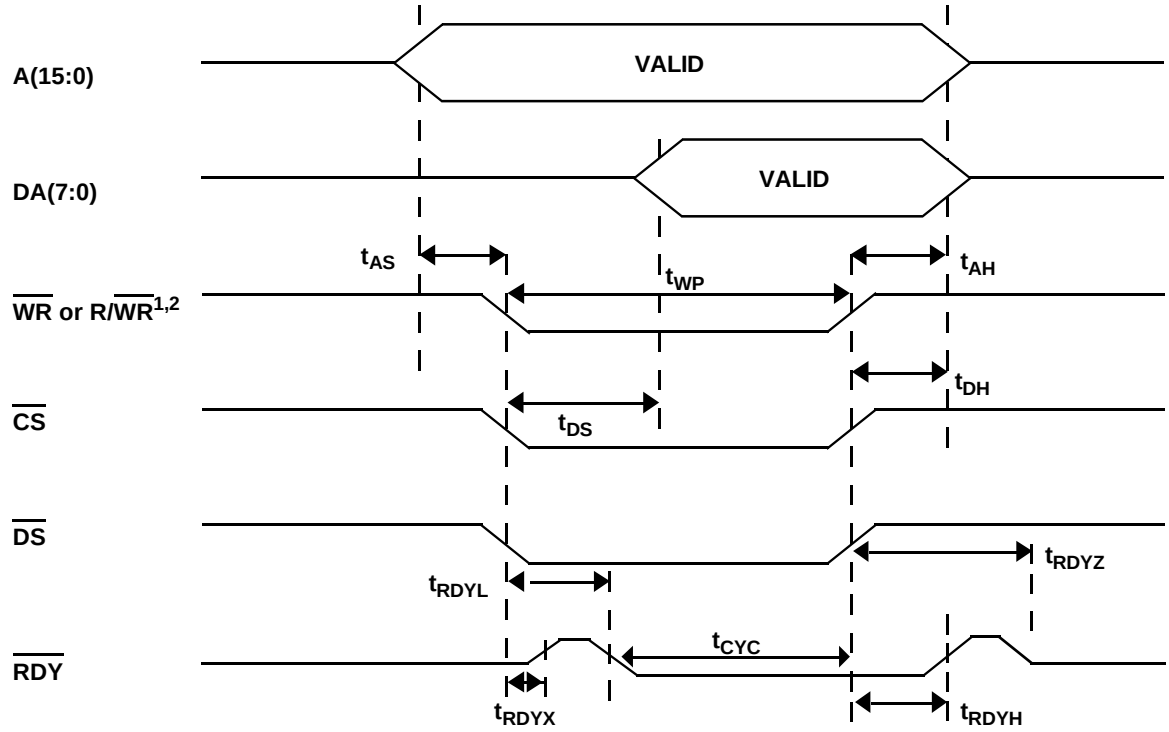
GND = 0V[1]
-55°C < T_C < +125°C

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
I_{CC}	V_{CC} supply current	0% duty cycle (non-transmitting) 25% duty cycle (f = 1MHz) [3] 50% duty cycle (f = 1MHz) [3] 87.5% duty cycle (f = 1MHz) [3] 100% duty cycle (f = 1MHz) [3]		55 250 410 650 855	mA mA mA mA mA
Q_{IDD}	Quiescent current [2]	f = 0MHz		1	mA
S_{IDD}	Standby operating current	f = 24MHz		40	mA

Notes:
1 Maximum allowable relative shift = 50mV.
2. All inputs tied to V_{DD}.
3. Guaranteed by characterization, not tested.

13.0 SµMMIT RTE AC ELECTRICAL CHARACTERISTICS

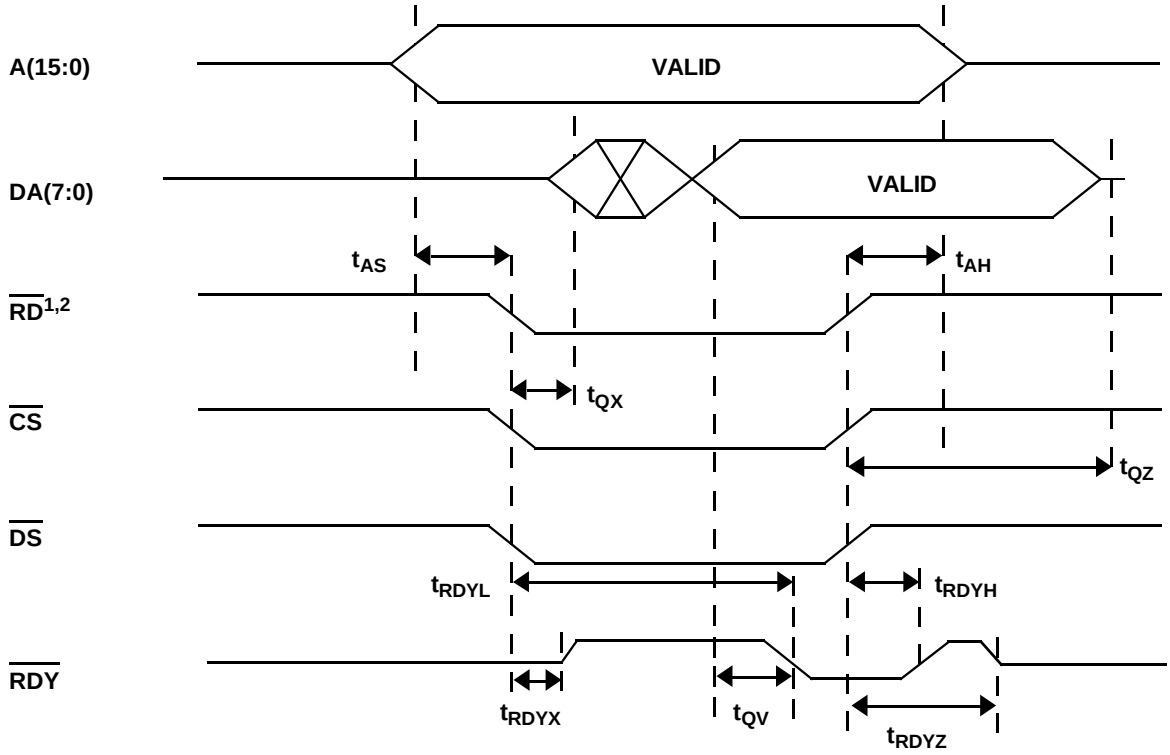
(f= 24MHz ±0.01%, Duty Cycle 50%±5%)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time[5]	5	--	ns
t_{DS}	Date setup time[5]	--	20	ns
t_{WP}	Write pulse width (non-contended)[5]	230 [4]	--	ns
t_{WP}	Write pulse width (contended)[5]	1700 [3,4]	--	ns
t_{AH}	Address hold time[5]	0	--	ns
t_{DH}	Data hold time[5]	0	--	ns
t_{RDYL}[1]	$\overline{RDY}$ low time (non-contended)	--	245	ns
t_{RDYL}[2]	$\overline{RDY}$ low time (contended)	--	1700 [3]	ns
t_{RDYH}	$\overline{RDY}$ high time[5]	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z[5]	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z[5]	--	33	ns
t_{CYC}	Minimum cycle time[5]	20	--	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.
4. For applications not using $\overline{RDY}$ signal.
5. Guaranteed be design; not tested.

Figure 17. Non-Multiplexed Memory/Register Write (8-Bit)

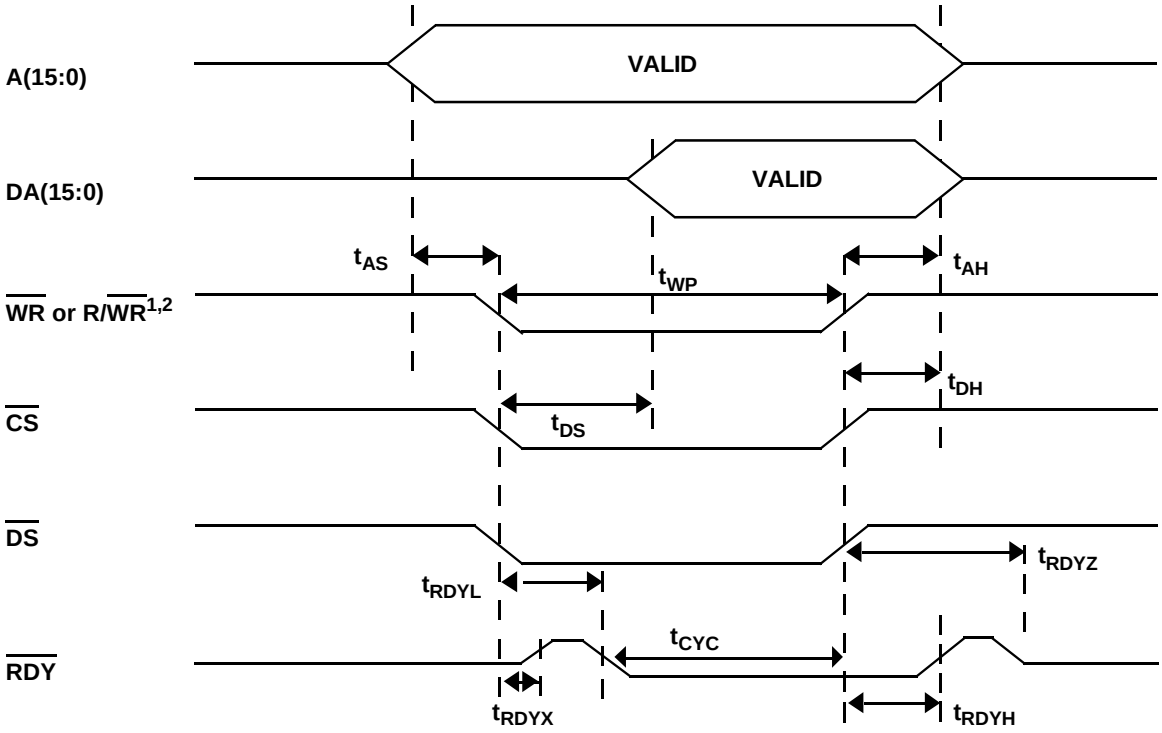


SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time[4]	5	--	ns
t_{QX}	Data low Z[4]	0	30	ns
t_{AH}	Address hold time[4]	0	--	ns
t_{QV}	Data valid[4]	12	--	ns
t_{QZ}	Data high Z[4]	0	32	ns
t_{RDYL}	$\overline{RDY}$ low time (non-contended)[4]		245	ns
t_{RDYL}	$\overline{RDY}$ low time (contended)[4]		1700 [3]	ns
t_{RDYH}	$\overline{RDY}$ high time[4]	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z[4]	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z[4]	--	33	ns

Note:

1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
3. Non-buffered mode of operation.
4. Guaranteed by design; not tested.

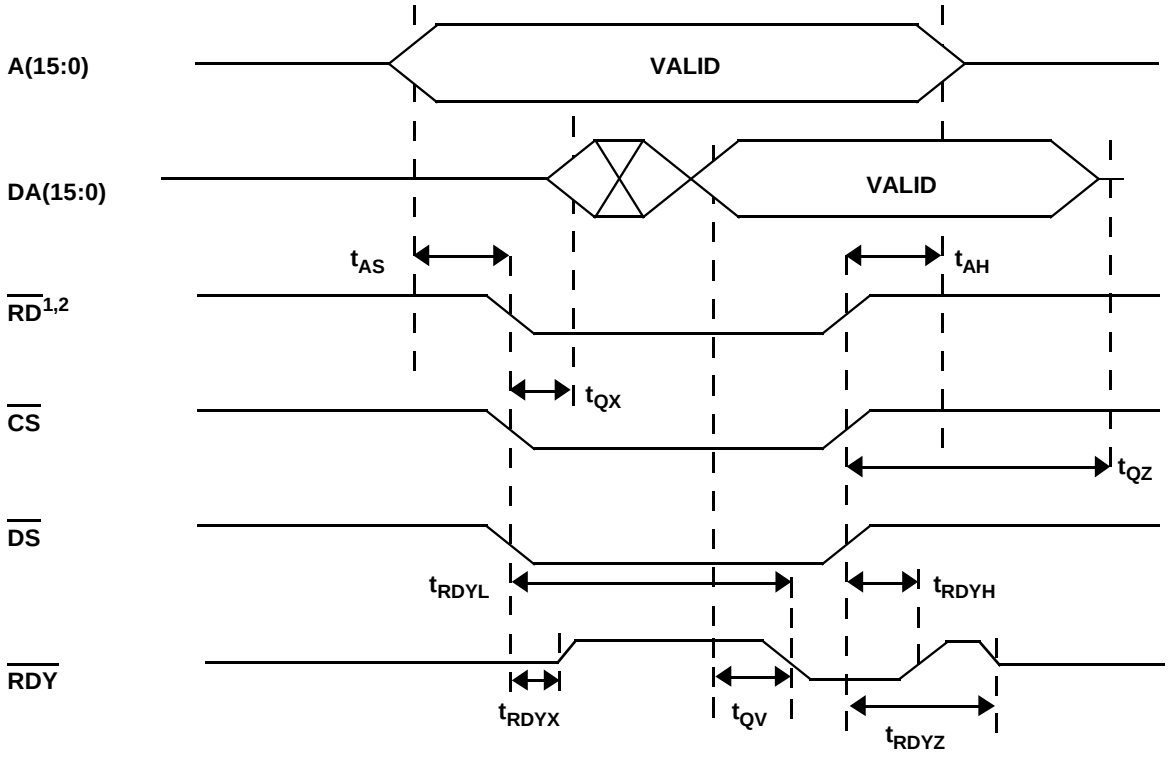
Figure 18. Non-Multiplexed Memory/Register Read (8-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time[5]	5	--	ns
t_{DS}	Data setup time[5]	--	20	ns
t_{WP}	Write pulse width (non-contended)[6]	230 [4]	--	ns
t_{WP}	Write pulse width (contended)[6]	1700 [3,4]	--	ns
t_{AH}	Address hold time[5]	0	--	ns
t_{DH}	Data hold time[5]	0	--	ns
t_{RDYL}	$\overline{RDY}$ low time (non-contended)	--	245	ns
t_{RDYL}	$\overline{RDY}$ low time (contended)[6]	--	1700 [3]	ns
t_{RDYH}	$\overline{RDY}$ high tim[5]	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z[5]	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns
t_{CYC}	Minimum cycle time[6]	20	--	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.
4. For applications not using $\overline{RDY}$ signal.
5. Guaranteed by characterization; not tested.
6. Guaranteed by design; not tested.

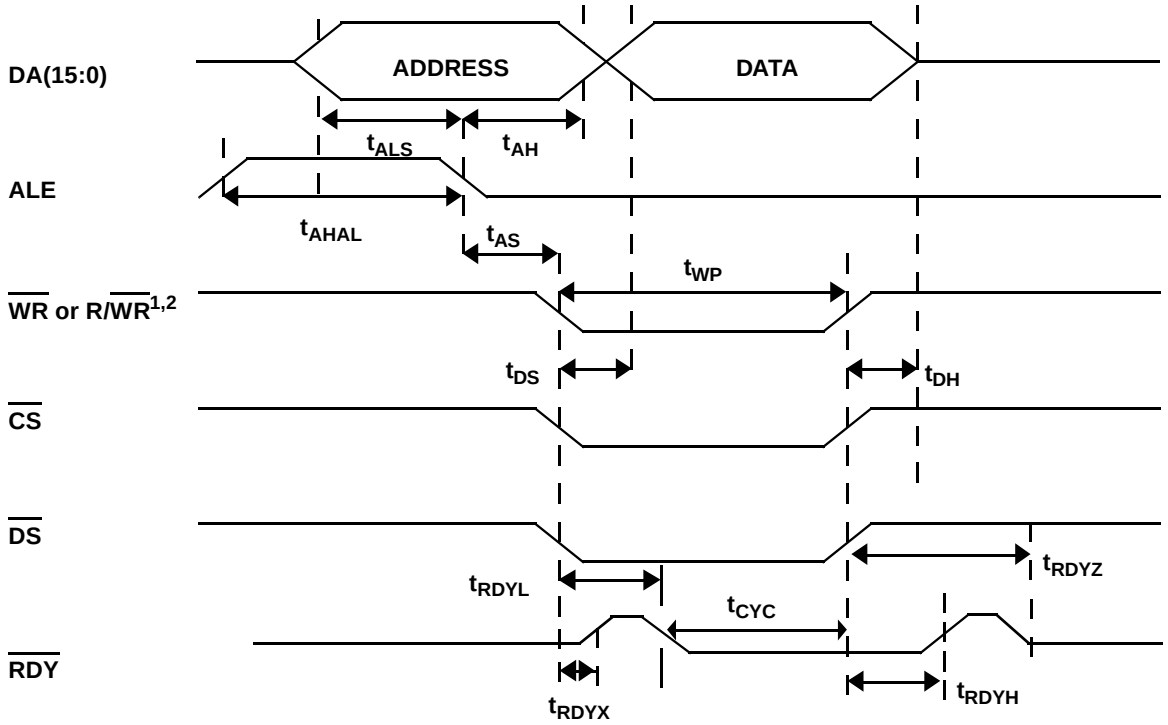
Figure 19. Non-Multiplexed Memory/Register Write (16-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time[4]	5	--	ns
t_{QX}	Data low Z[4]	0	30	ns
t_{AH}	Address hold time[4]	0	--	ns
t_{QV}	Data valid[4]	20	--	ns
t_{QZ}	Data high Z[4]	0	32	ns
t_{RDYL}	$\overline{RDY}$ low time (non-contended)	--	245	ns
t_{RDYL}	$\overline{RDY}$ low time (contended)[5]	--	1700 [3]	ns
t_{RDYH}	$\overline{RDY}$ high time[4]	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z[4]	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
3. Non-buffered mode of operation.
4. Guaranteed by characterization; not tested.
5. Guaranteed by design; not tested.

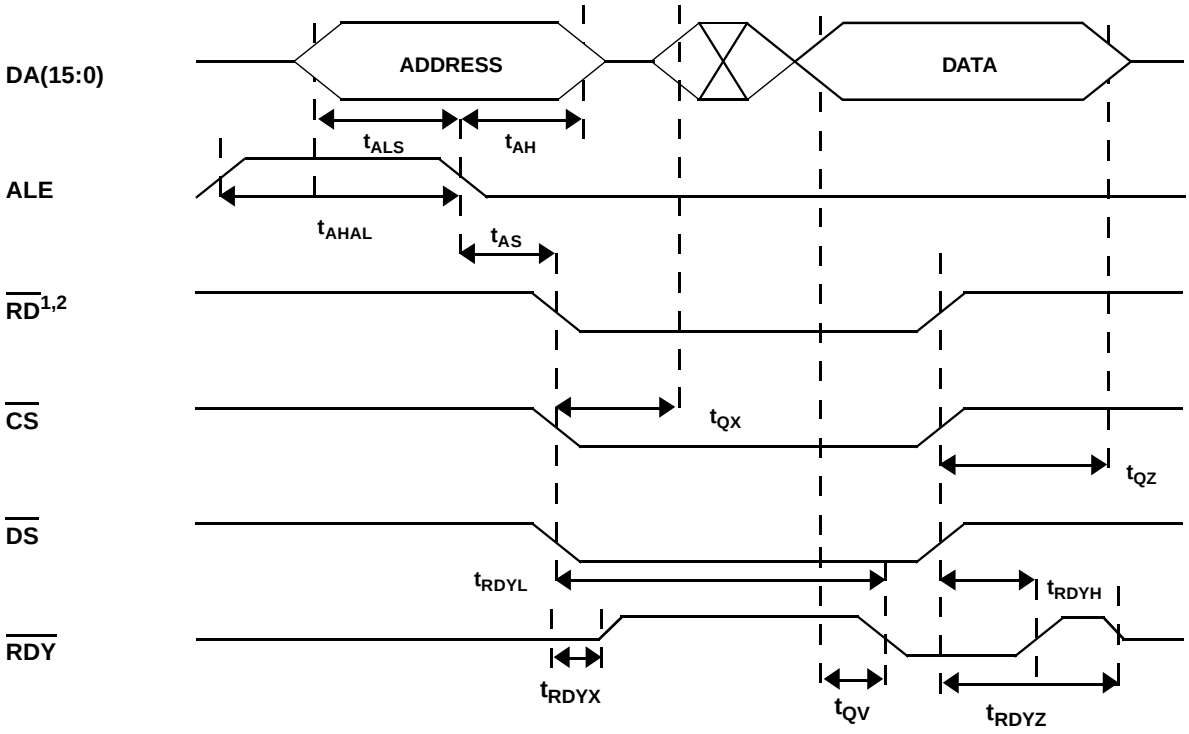
Figure 20. Non-Multiplexed Memory/Register Read (16-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time[5]	0	--	ns
t_{AHAL}	ALE pulse width[5]	20	--	ns
t_{DS}	Data setup time[6]	--	20	ns
t_{WP}	Write pulse width (non-contended)[5]	230 [4]	--	ns
t_{WP}	Write pulse width (contended)[5]	1700 [3,4]	--	ns
t_{AH}	Address hold time[6]	5	--	ns
t_{DH}	Data hold time[6]	0	--	ns
t_{RDYL}	$\overline{RDY}$ low time (non-contended)[6]	--	245	ns
t_{RDYL}	$\overline{RDY}$ low time (contended)[5]	--	1700 [3]	ns
t_{RDYH}	$\overline{RDY}$ high time[5]	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z[5]	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z[5]	--	33	ns
t_{ALS}	Address latch setup time[6]	5	--	ns
t_{CYC}	Minimum cycle time[5]	20	--	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.
4. For applications not using $\overline{RDY}$ signal.
5. Guaranteed by design; not tested.
6. Guaranteed by characterization; not tested.

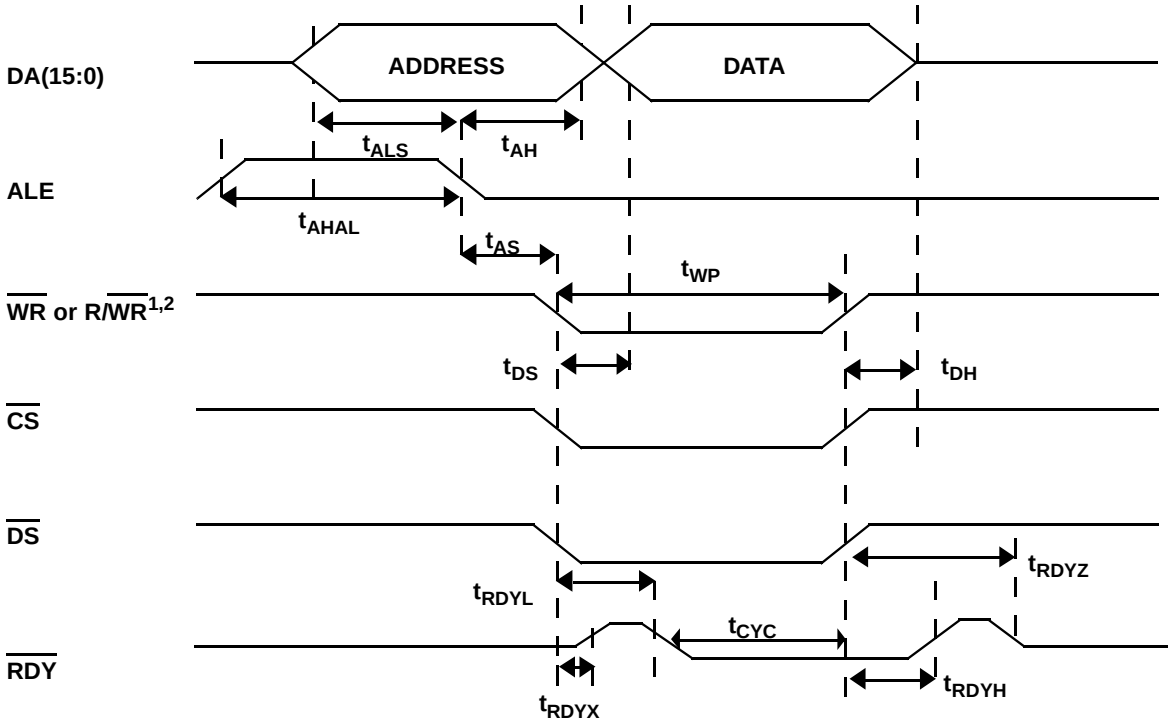
Figure 21. Multiplexed Memory/Register Write (8-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time[4]	0	--	ns
t_{AHAL}	ALE pulse width[4]	20	--	ns
t_{QX}	Data low Z[4]	0	30	ns
t_{AH}	Address hold time[4]	5	--	ns
t_{QV}	Data valid[4]	12	--	ns
t_{QZ}	Data high Z[4]	3	32	ns
t_{RDYL}	$\overline{RDY}$ low time (non-contended)[4]	--	245	ns
t_{RDYL}	$\overline{RDY}$ low time (contended)[4]	--	1700 [3]	ns
t_{RDYH}	$\overline{RDY}$ high time[4]	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z[4]	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z[4]	--	33	ns
t_{ALS}	Address latch setup time[4]	5	--	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
3. Non-buffered mode of operation.
4. Guaranteed by design; not tested.

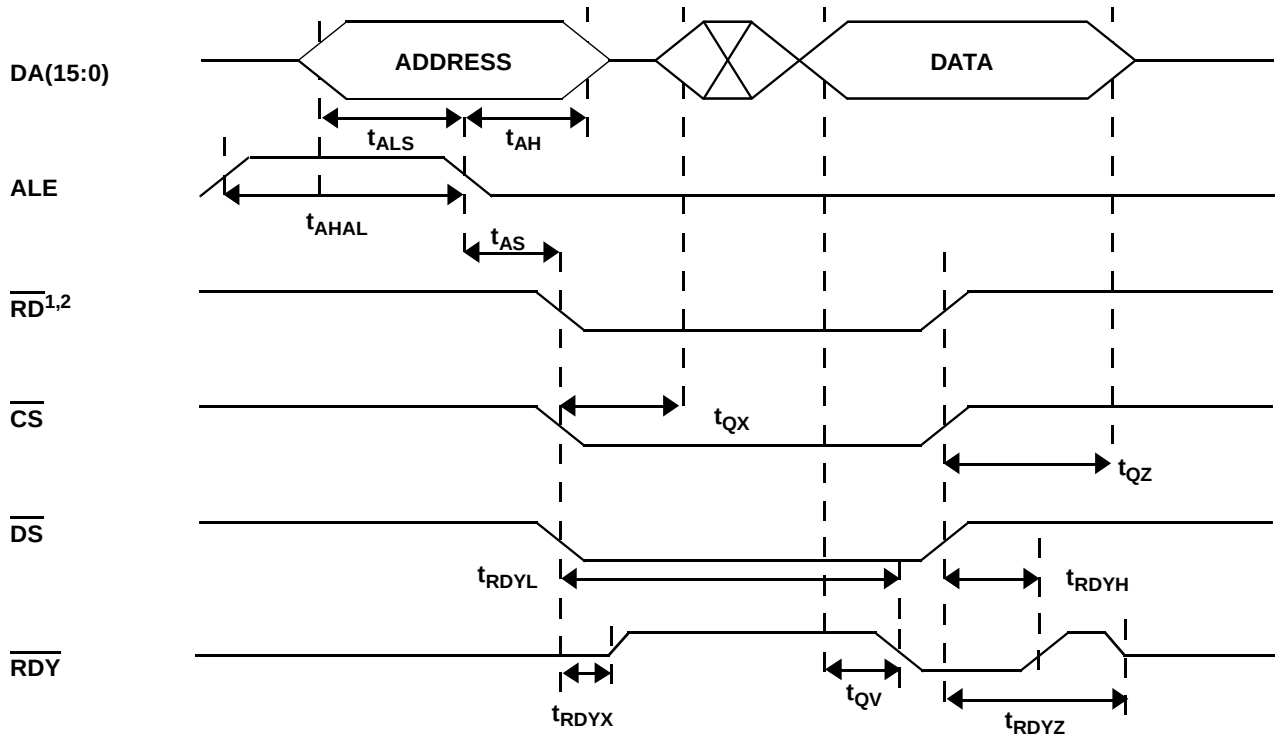
Figure 22. Multiplexed Memory/Register Read (8-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time[5]	0	--	ns
t_{AHAL}	ALE pulse width[5]	20	--	ns
t_{DS}	Data setup time[5]	--	20	ns
t_{WP}	Write pulse width (non-contended)[5]	230 [4]	--	ns
t_{WP}	Write pulse width (contended)[5]	1700 [3,4]	--	ns
t_{AH}	Address hold time[5]	5	--	ns
t_{DH}	Data hold time[5]	0	--	ns
t_{RDYL}	$\overline{RDY}$ low time (non-contended)[5]	--	245	ns
t_{RDYL}	$\overline{RDY}$ low time (contended)[5]	--	1700 [3]	ns
t_{RDYH}	$\overline{RDY}$ high time[5]	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z[5]	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z[5]	--	33	ns
t_{ALS}	Address latch setup time[5]	5	--	ns
t_{CYC}	Minimum cycle time[5]	20	--	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.
4. For applications not using $\overline{RDY}$ signal.
5. Guaranteed by design; not tested.

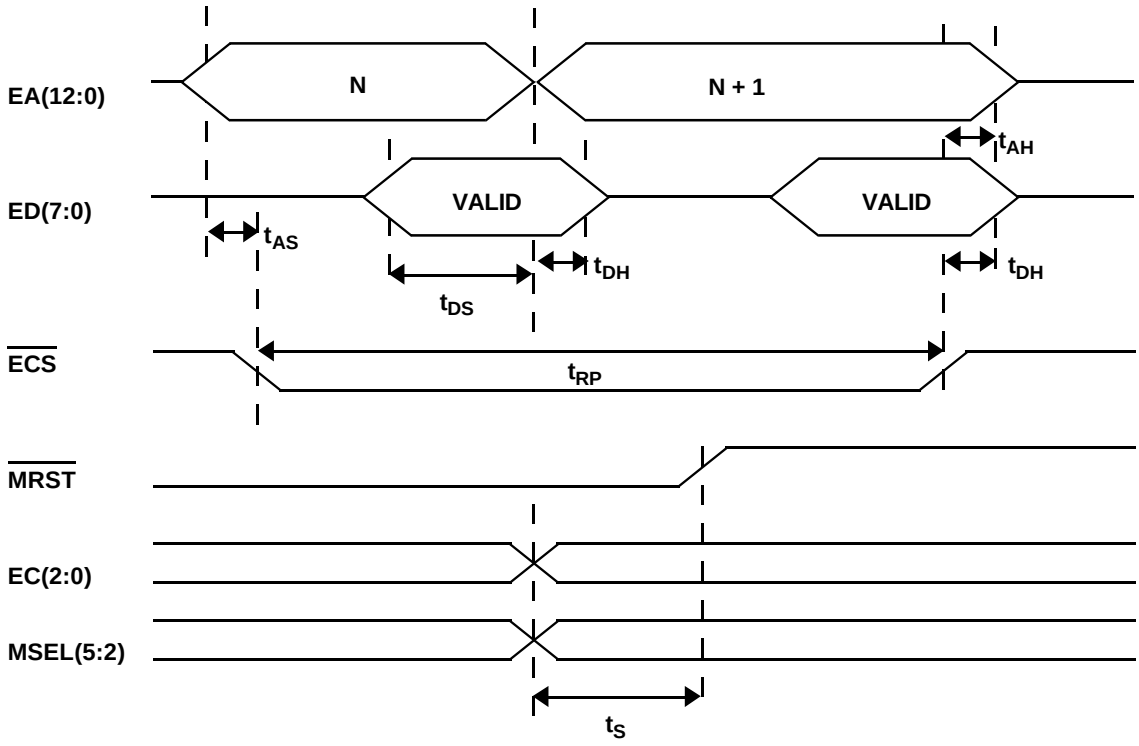
Figure 23. Multiplexed Memory/Register Write (16-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time[4]	0	--	ns
t_{AHAL}	ALE pulse width[4]	20	--	ns
t_{QX}	Data low Z[4]	0	30	ns
t_{AH}	Address hold time[4]	5	--	ns
t_{QV}	Data valid[4]	20	--	ns
t_{QZ}	Data high Z[4]	3	32	ns
t_{RDYL}	$\overline{RDY}$ low time (non-contended)[4]	--	245	ns
t_{RDYL}	$\overline{RDY}$ low time (contended)[4]	--	1700 [3]	ns
t_{RDYH}	$\overline{RDY}$ high time[4]	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z[4]	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z[4]	--	33	ns
t_{ALS}	Address latch setup time[4]	5	--	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$
3. Non-buffered mode of operation.
4. Guaranteed by design; not tested.

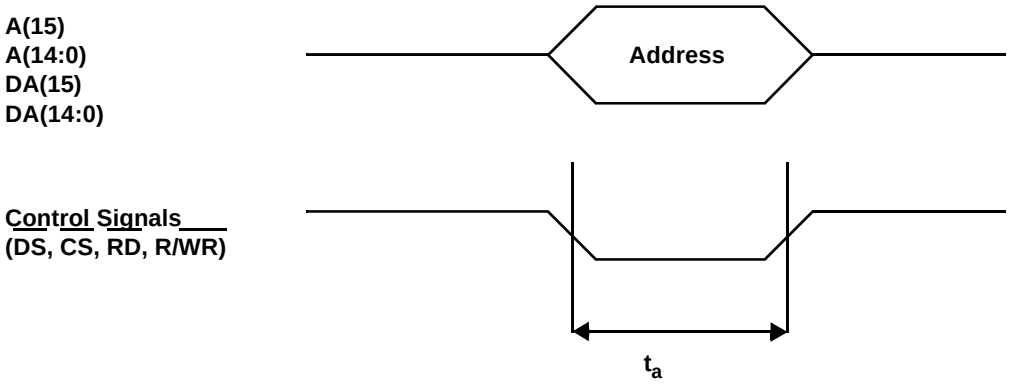
Figure 24. Multiplexed Memory/Register Read (16-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time[1]	35	--	ns
t_{AH}	Address hold time[1]	35	--	ns
t_{DS}	Data setup time[2]	41	--	ns
t_{DH}	Data hold time[2]	5	--	ns
t_{RP}	Read pulse width[2]	160	--	ns
t_S	Setup time[2]	45	--	ns

Figure 25. Auto-Initialization Read Cycle

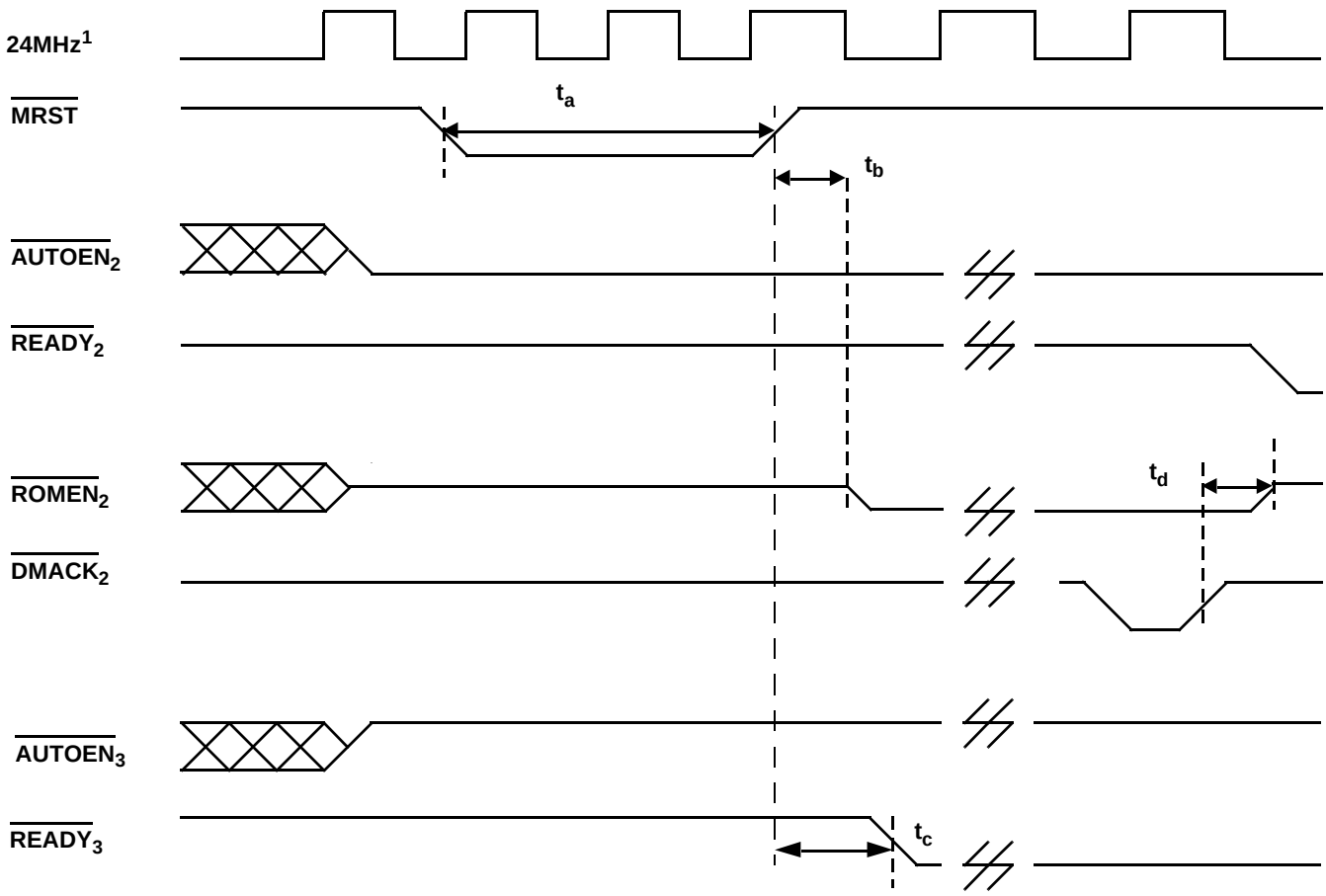
Notes:
1. Guaranteed by characterization; not tested.
2. Guaranteed by design; not tested.



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_a[1]	Maximum Register/Memory Time	--	7	µs

Figure 26. Maximum Cycle Time

Notes:
1. Guaranted by design; not tested.



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_a	$\overline{\text{MRST}}$ pulse width	500	--	ns
t_b	$\overline{\text{MRST}}$ negation to $\overline{\text{ROMEN}}$ assertion	--	5	µs
t_c	$\overline{\text{MRST}}$ negation to $\overline{\text{READY}}$ assertion	--	10	µs
t_d	$\overline{\text{DMACK}}$ negation to $\overline{\text{ROMEN}}$ negation	--	500	ns

Note:
1. SµMMIT must receive at least 3 24MHz clock cycles before deassertion of $\overline{\text{MRST}}$.
2. Power-up Master Reset Timing with Auto-initialization enabled.
3. Power-up Master Reset Timing with Auto-initialization disabled.

Figure 27. Power-up Master Reset Timing

14.0 SμMMIT RTE RECEIVER ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0V±10% GND = 0V
V_{CC} = 5.0V±10% -55°C < T_C < +125°C
V_{SS} = 0V

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IC}[1]	Common mode input voltage	Direct-coupled stub; input 1.2V_{PP}, 200ns rise/fall time ±25ns, *f* = 1MHz	-5	5	V
V_{TH}	Input threshold voltage (no response)[1]	Transformer-coupled stub; input at *f* = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)		0.20	$V_{PP,L-L}$
	Input threshold voltage (no response)	Direct-coupled stub; input at *f* = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)		0.28	$V_{PP,L-L}$
	Input threshold voltage (response)[1]	Transformer-coupled stub; input at *f* = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)	0.86	14.0	$V_{PP,L-L}$
	Input threshold voltage (response)[1]	Direct-coupled stub; input at *f* = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)	1.20	20.0	$V_{PP,L-L}$
CMRR [1,2]	Common mode rejection ratio		Pass/Fail		N/A

Notes:
1. Guaranteed by design; not tested.
2. Pass/fail criteria per the test method described in MIL-HDBK-1553 Appendix A, RT Validation Test Plan, Section 5.1.2.2, Common Mode Rejection.

15.0 SμMMIT RTE TRANSMITTER ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0V±10% GND = 0V
V_{CC} = 5.0V ±10% -55°C < T_C < +125°C
V_{SS} = 0V

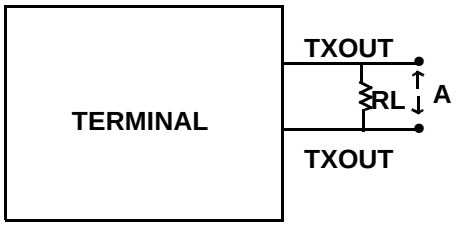
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
V_O	Output voltage swing per MIL-STD-1553B [1] (see figure 52)	18	27	$V_{PP,L-L}$	Transformer-coupled stub, figure 27, Point A; input *f* = 1MHz, R_L = 70 ohms
	per MIL-STD-1553B (see figure 52)	6.0	9	$V_{PP,L-L}$	Direct-coupled stub, figure 27, Point A; input *f* = 1MHz, R_L = 35 ohms
	per MIL-STD-1553A [1] (see figure 52)	6.0	20	$V_{PP,L-L}$	
V_{NS}[1]	Output noise voltage differential (see figure 52)		14	mV-RMS $_{L-L}$	Transformer-coupled stub, figure 27, Point A; input *f* = DC to 10MHz, RL = 70 ohms
			5	mV-RMS $_{L-L}$	Direct-coupled stub, figure 27, Point A; input *f* = DC to 10MHz, R_L = 35 ohms
V_{OS}[1]	Output symmetry (see figure 52)	-250	+250	$mV_{PP,L-L}$	Transformer-coupled stub, figure 27, Point A; R_L = 70 ohms, measurement taken 2.5μs after end of transmission
		-90	+90	$mV_{PP,L-L}$	Direct-coupled stub, figure 27, Point A; R_L = 35 ohms, measurement taken 2.5μs after end of transmission
V_{DIS}[1]	Output voltage distortion (overshoot or ring) (see figure 52)	-900	+900	$mV_{peak,L-L}$	Transformer-coupled stub, figure 27, Point A; R_L = 70 ohms
		-300	+300	$mV_{peak,L-L}$	Direct-coupled stub, figure 27, Point A; R_L = 35 ohms
T_{IZ}[2]	Terminal input impedance	1		Kohm	Transformer-coupled stub, figure 27, Point A; input *f* = 75KHz to 1MHZ (power on or power off; non-transmitting, R_L removed from circuit).
		2		Kohm	Direct-coupled stub, figure 27, Point A; input *f* = 75KHz to 1MHZ (power on or power off; non-transmitting, R_L removed from circuit).

Note:
1. Guaranteed by design; not tested.
2. Guaranteed by characterization; not tested.

16.0 SµMMIT RTE AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0V±10% GND = 0V
V_{CC} = 5.0V ±10% -55°C < T_C < +125°C
V_{SS} = 0V

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
t_R, t_F	Transmitter output rise/ fall time (see figure 53)	100	300	ns	Input *f* = 1MHz 50% duty cycle: direct-coupled RL = 35 ohms output at 10% through 90% points TXOUT, $\overline{\text{TXOUT}}$. Figure 29.
t_{RZCD}	Zero crossing distortion (see figure 54)	-150	150	ns	Direct-coupled stub; input *f* = 1MHz, 3 V_{PP} (skew INPUT ±150ns), rise/fall time 200ns.
t_{TZCS}	Zero crossing stability (see figure 54)	-25	25	ns	Input TXIN and $\overline{\text{TXIN}}$ should create Transmitter output zero crossings at 500ns, 1000ns, 1500ns, and 2000ns. These zero crossings should not deviate more than ±25ns.



Notes:
1. Transformer Coupled Stub:
   Terminal is defined as transceiver plus isolation transformer.
2. Direct Coupled Stub:
   Terminal is defined as transceiver plus isolation transformer and fault resistors.

Figure 28. Transceiver Test Circuit MIL-STD-1553B

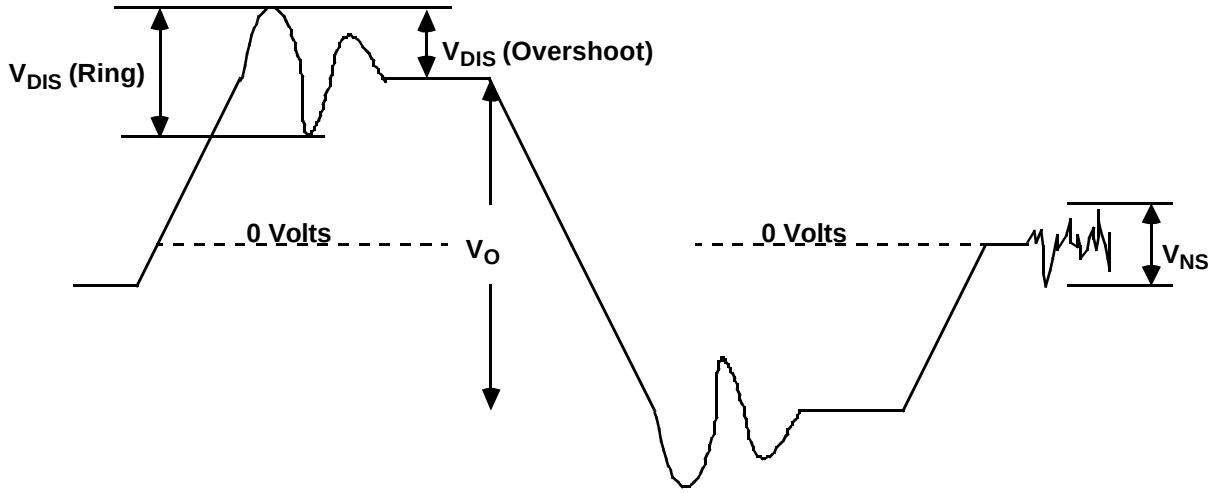


Figure 29. Transmitter Output Characteristics (V_{DIS}, V_{OS}, V_{NS}, V_O)

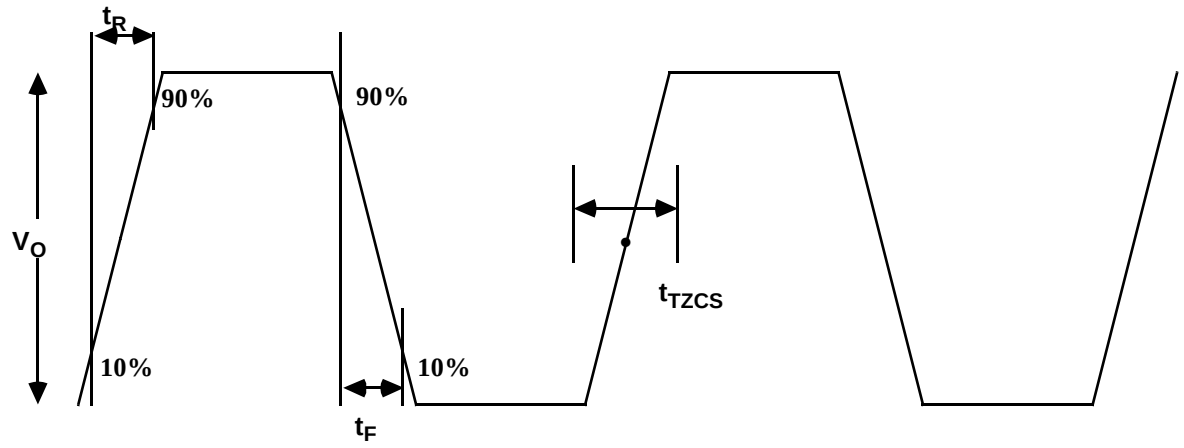


Figure 30. Transmitter Output Zero Crossing Stability, Rise Time, Fall Time (t_{TZCS}, t_R, t_F)

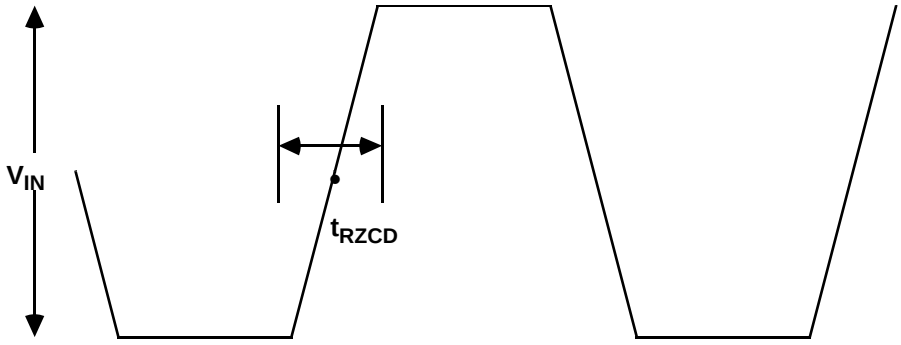


Figure 31. Receiver Input Zero Crossing Distortion (t_{RZCD})

17.0 PACKAGING

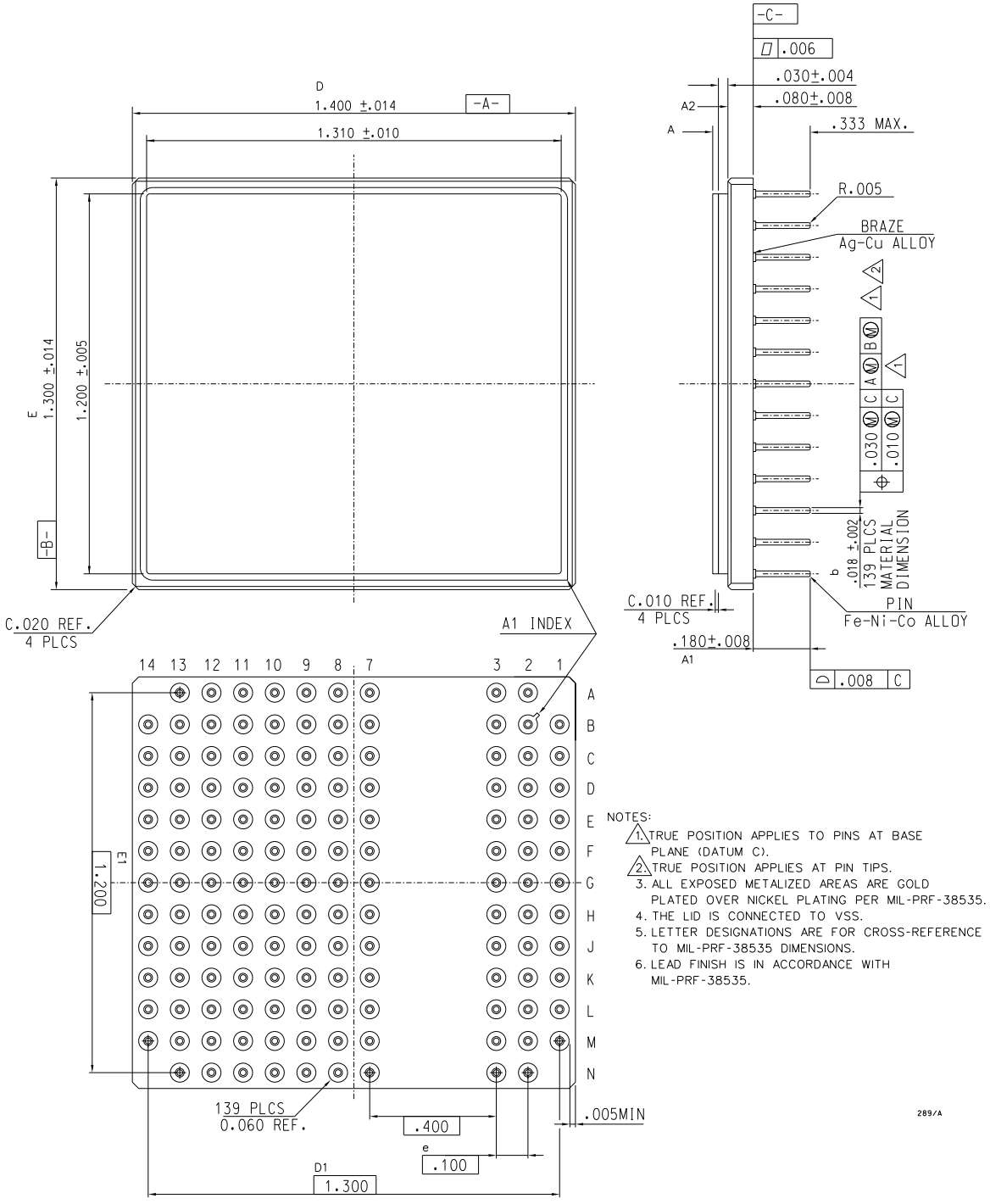


Figure 31. SμMMIT RTE 139-Pingrid Array

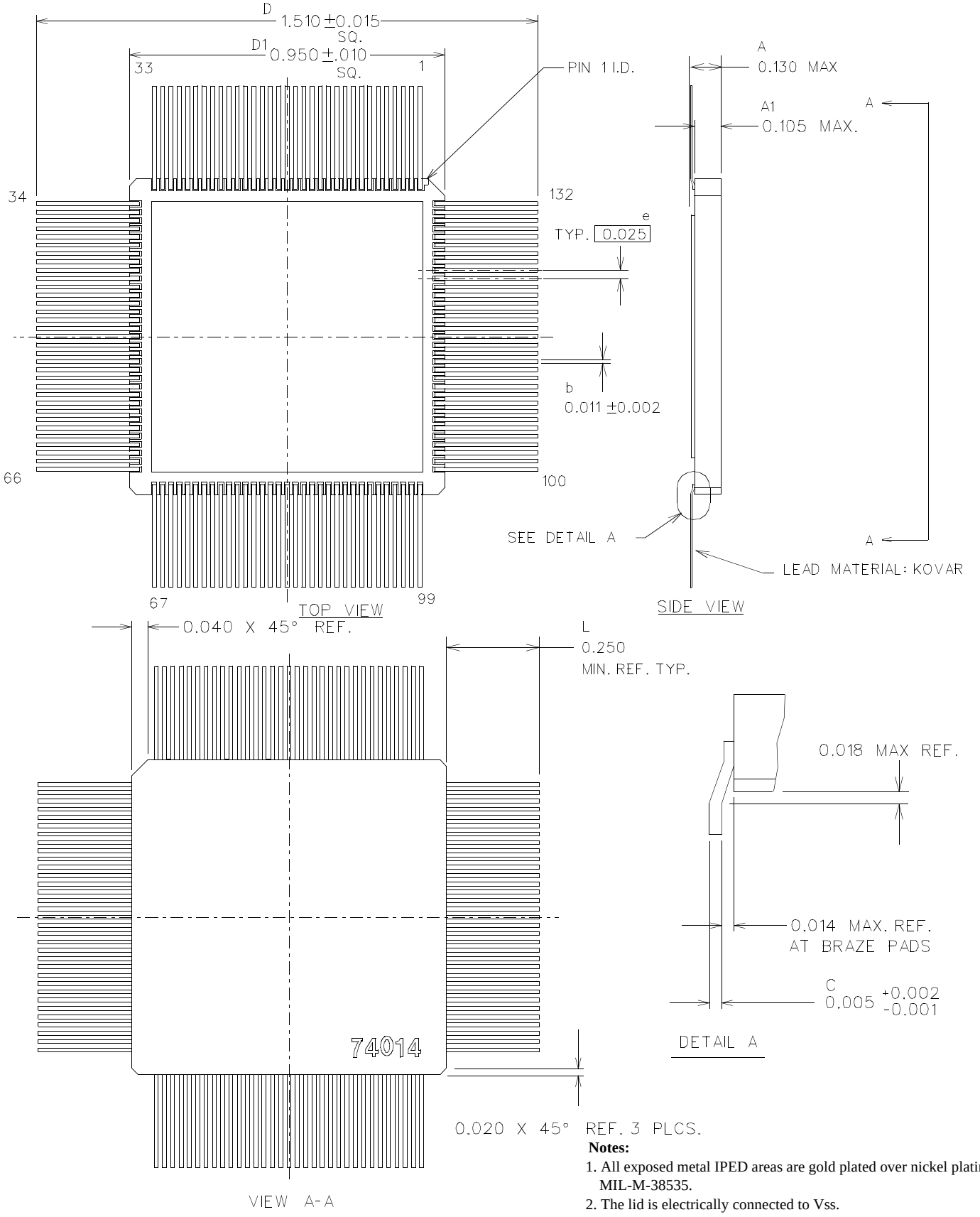
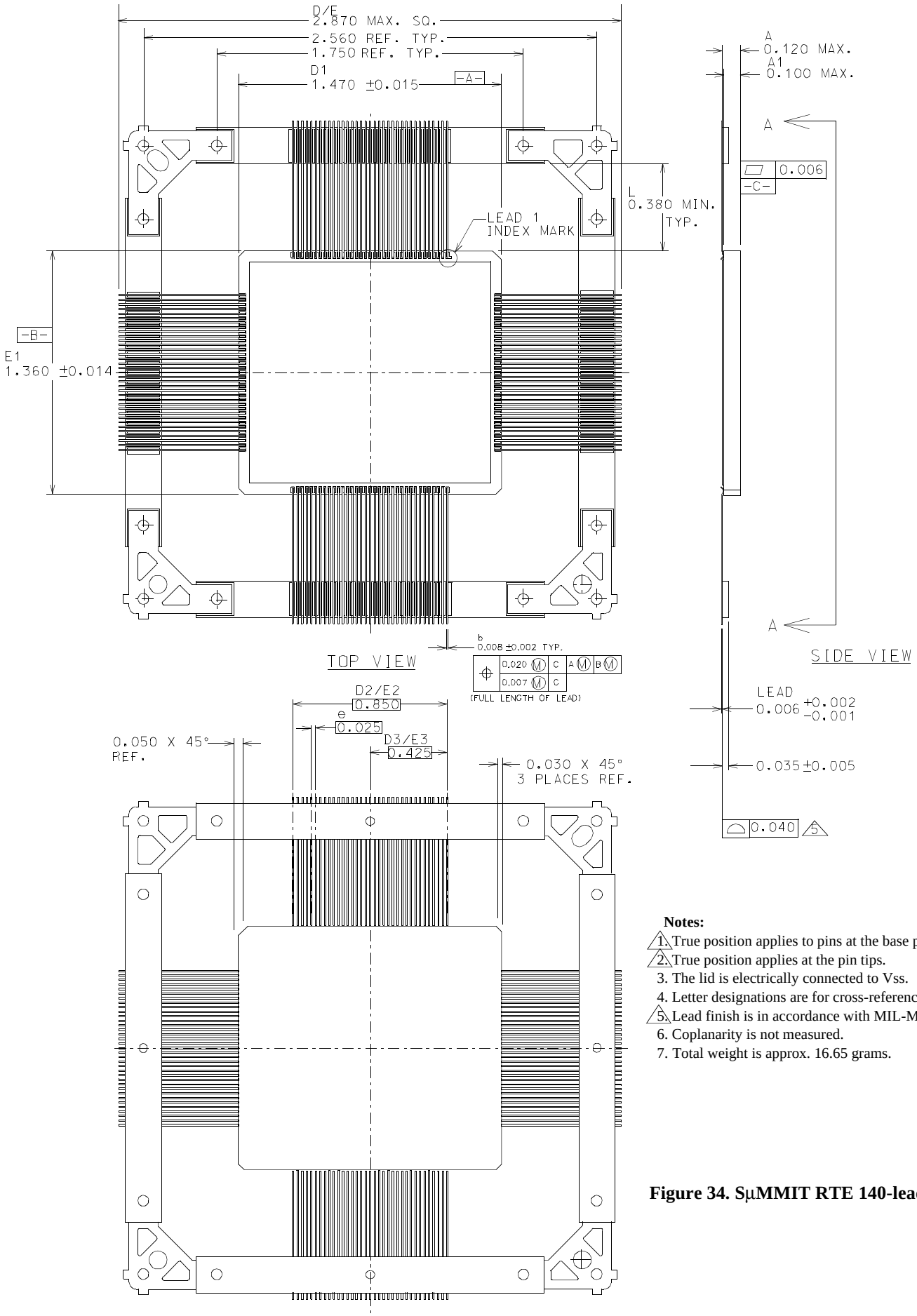


Figure 33. SµMMIT RTE 132-Lead Flatpack

Notes:

1. All exposed metal IPED areas are gold plated over nickel plating per MIL-M-38535.
2. The lid is electrically connected to Vss.
3. Lead finish is in accordance with MIL-PRF-38535.
4. Letter designations are to cross-reference to MIL-STD-1835.
5. Lead true position tolerances and coplanarity are not measured.



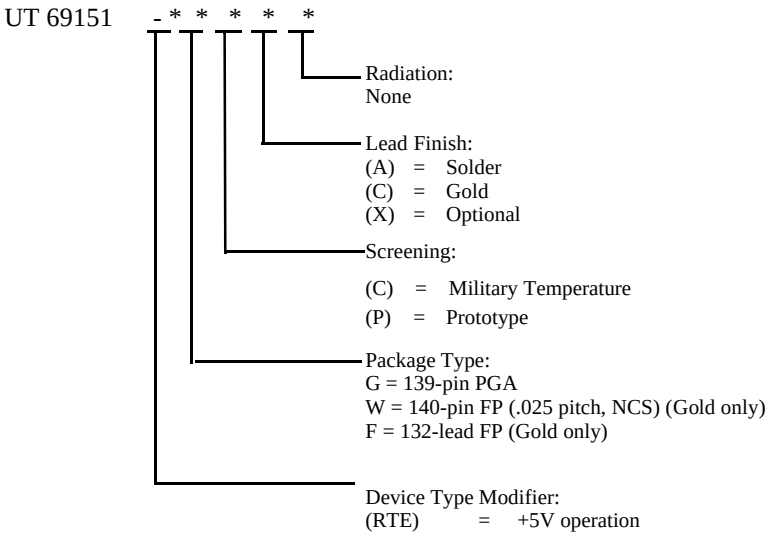
Notes:

1. True position applies to pins at the base plane (Datum C).
2. True position applies at the pin tips.
3. The lid is electrically connected to Vss.
4. Letter designations are for cross-reference to MIL-STD-1835.
5. Lead finish is in accordance with MIL-M-38535.
6. Coplanarity is not measured.
7. Total weight is approx. 16.65 grams.

Figure 34. SµMMIT RTE 140-lead Flatpack

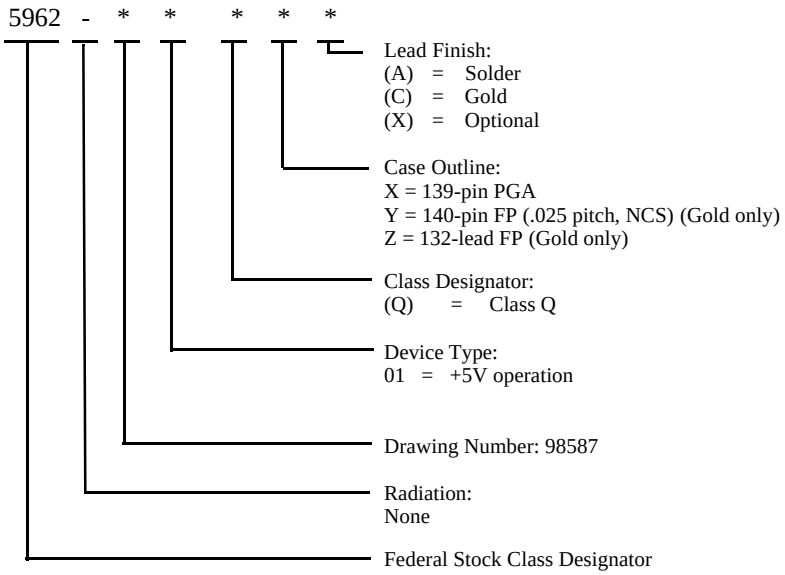
18.0 ORDERING INFORMATION

SμMMIT RTE MIL-STD-1553 Dual Redundant Remote Terminal w/Integrated Bus Transceivers & Memory



Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Military Temperature Range flow per UTMC's Manufacturing Flows documents. Devices have 48 hours of burn-in and are tested at -55°C, room temperature, and +125°C.
4. Prototypes are produced to UTMC's prototype flow, and are tested at 25°C only. Lead finish is gold only.
5. 132 FP and 140 FP only available with gold lead finish.

SμMMIT RTE MIL-STD-1553 Dual Redundant Remote Terminal w/Integrated Bus Transceivers & Memory: SMD



Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. 132 FP and 140FP only available with gold lead finish.