Standard Products

UT32BS1X833 Matrix-D™ 32-Channel 1:8 Bus Switch

Advanced Data Sheet

November 12, 2014

www.aeroflex.com/busswitch

FEATURES

- Interfaces to standard processor memory busses
- Single-chip interface that provides memory paging to industry-standard SDRAMS
- Eliminates need for additional logic or FPGA
- I/O channels functional to 3.3V
- R_{ON} 5 Ohms typical
- Flat R_{ON} characteristics over channel voltage
- Propagation delay 300ps through switch
- Transmission gate technology allows for true bi-directional operation
- Internal pull-up resistors on the first 8 outputs of each bank to ensure memory devices remain in off state when channels de-selected
- Bus holders maintain output states on all other outputs when channels de-selected
- Logic power 1mW/MHz
- Temperature range -55°C to 125°C
- Operational environment:
  - Intrinsic total-dose: up to 300 krad(Si)
  - SEL Immune $\leq$100 MeV-cm^2/mg
- Packaging options:
  - 400-pin Ceramic Land Grid, Column Grid and Ball Grid Array packages; 1mm pitch
- Standard Microcircuit Drawing 5962-TBD
  - QML Q and V (pending)

APPLICATIONS

- Microprocessor interfaces that require large amounts of SDRAM memory
- High-speed applications or systems with large bus capacitance
- Cost-sensitive applications that require bus isolation without an expensive FPGA
- Large SDRAM paging architecture

INTRODUCTION

The UT32BS1X833 Matrix-D™ is a 32-Channel, 1:8 Bus Switch, that provides bus isolation for up to eight banks of 32 I/O connections. By providing bus isolation, the UT32BS1X833 can significantly reduce the amount of load capacitance seen by a host processor and memory devices. The enable to output delay time is only 4.1ns (typical). The reduction in both load capacitance and delay time significantly increase speed and performance compared with a discrete logic or FPGA memory interface solution.

The UT32BS1X833 operates from a single 3.3V supply. The bus channels can pass any voltage between V_{SS} and V_{DD}, allowing the switching of signals using other standards, such as LVCMOS 1.8V. The input and output banks connect via analog channels that have an R_{ON} that is nominally 5 Ohms over the entire input voltage range. The flat R_{ON} eliminates the need to add external series resistors for source impedance termination.

The UT32BS1X833 has a “broadcast mode” that is enabled by driving both $\overline{SDCS[1]}$ and $\overline{SDCS[0]}$ low. In this mode, all banks are active, which facilitates SDRAM refresh and initialization cycles.

Each UT32BS1X833 can interface up to eight of the Aeroflex 2.5Gb or 3.0Gb SDRAM MCM devices with any Aeroflex LEON processor without the need for additional logic.

INTRODUCTION

The UT32BS1X833 32-Channel 1:8 Bus Switch is built on the Aeroflex 0.35µm process. The device incorporates control logic that electrically connects input bank A to the output banks B0-B7, depending upon the selected channel. Figure 1 shows a block diagram of the device. The $\overline{CS}$ input is a master device select input that enables the device when asserted low. When high, the device is in active, and all outputs are turned off, except in the case of a refresh or initialization cycle. Refresh and initialization cycles are automatically passed on to all connected SDRAM devices when $\overline{SDCS[1]}$ and $\overline{SDCS[0]}$ are both asserted low. During either of these cycles, all output banks are turned on. The select inputs SEL[2:0] determine which bank is turned on for normal SDRAM read and write operations.

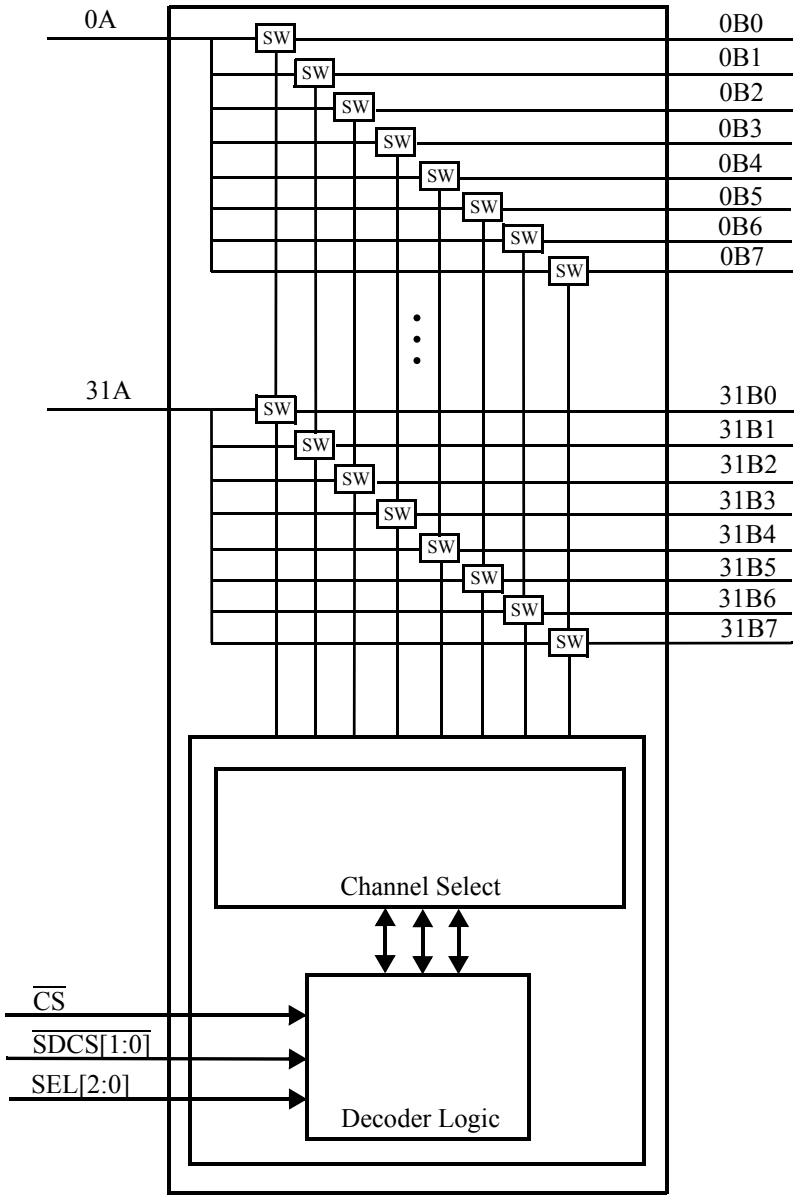


Figure 1. UT32BS1X833 Functional Block Diagram

FUNCTIONAL TABLES

Table 1. Truth Table for Digital Inputs and Channels												
Inputs					Selected Banks							
$\overline{CS}$	$\overline{SDCS[1:0]}$	SEL[2]	SEL[1]	SEL[0]	7	6	5	4	3	2	1	0
1	X1b or 1Xb	X	X	X								
X	00b	X	X	X	•	•	•	•	•	•	•	•
0	X1b or 1Xb	0	0	0								•
0	X1b or 1Xb	0	0	1							•	
0	X1b or 1Xb	0	1	0						•		
0	X1b or 1Xb	0	1	1					•			
0	X1b or 1Xb	1	0	0				•				
0	X1b or 1Xb	1	0	1			•					
0	X1b or 1Xb	1	1	0		•						
0	X1b or 1Xb	1	1	1	•							

The table above indicates which banks are active based upon the selected input logic. All banks are in a high-Z state when unselected.

PIN IDENTIFICATION and DESCRIPTION

Logic Pins

Pin Name	Direction	Pin Number	Description
$\overline{CS}$	I	M11	Master chip select for device
$\overline{SDCS[0]}$	I	M10	Enables broadcast mode when 00b. Otherwise, normal operation.
$\overline{SDCS[1]}$	I	N10	Enables broadcast mode when 00b. Otherwise, normal operation.
SEL[0]	I	P9	Bit 0 of bank select logic.
SEL[1]	I	P10	Bit 1 of bank select logic.
SEL[2]	I	R10	Bit 2 of bank select logic.

Channel Pins

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
0A	T4	0B0	R3	0B1	U4	0B2	U3	0B3	T3
1A	M3	1B0	R1	1B1	P3	1B2	N3	1B3	P2
2A	L1	2B0	U2	2B1	V1	2B2	L2	2B3	M2
3A	M4	3B0	N6	3B1	N5	3B2	N8	3B3	M5
4A	M8	4B0	P5	4B1	R4	4B2	N4	4B3	P4
5A	K9	5B0	L10	5B1	L8	5B2	L9	5B3	K8
6A	G5	6B0	G4	6B1	F5	6B2	H4	6B3	F6
7A	H7	7B0	J4	7B1	H5	7B2	J6	7B3	H6
8A	D2	8B0	K1	8B1	K2	8B2	C1	8B3	D1
9A	E1	9B0	H3	9B1	G2	9B2	G3	9B3	G1
10A	D5	10B0	C6	10B1	D4	10B2	C4	10B3	C5
11A	C9	11B0	A6	11B1	C7	11B2	C8	11B3	B7
12A	A10	12B0	B4	12B1	A3	12B2	B10	12B3	B9
13A	D9	13B0	F8	13B1	E8	13B2	F9	13B3	E9
14A	H9	14B0	E7	14B1	D6	14B2	D8	14B3	D7
15A	H11	15B0	J10	15B1	K11	15B2	H10	15B3	J11
16A	D15	16B0	F12	16B1	D13	16B2	D14	16B3	E14
17A	E13	17B0	E12	17B1	D12	17B2	H13	17B3	F13
18A	A17	18B0	B12	18B1	A11	18B2	B11	18B3	A18
19A	A15	19B0	B13	19B1	C13	19B2	B14	19B3	C14
20A	E18	20B0	D18	20B1	F18	20B2	F17	20B3	E17
21A	H19	21B0	G20	21B1	G18	21B2	G19	21B3	H18
22A	J19	22B0	D20	22B1	C20	22B2	K19	22B3	K20
23A	J16	23B0	H15	23B1	J15	23B2	H16	23B3	J17
24A	K14	24B0	J12	24B1	K15	24B2	J13	24B3	J14
25A	M15	25B0	L11	25B1	L15	25B2	L14	25B3	M14
26A	L16	26B0	P16	26B1	R16	26B2	L18	26B3	L17
27A	M20	27B0	N15	27B1	P15	27B2	N14	27B3	N20
28A	N19	28B0	U19	28B1	U20	28B2	V19	28B3	W19
29A	T19	29B0	R20	29B1	P20	29B2	T20	29B3	R19
30A	V16	30B0	V17	30B1	V15	30B2	U15	30B3	U16
31A	W13	31B0	Y15	31B1	V14	31B2	W14	31B3	V13
0B4	T2	0B5	R2	0B6	T1	0B7	P1		

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
1B4	N2	1B5	W2	1B6	V2	1B7	U1		
2B4	M1	2B5	N1	2B6	N7	2B7	P6		
3B4	L5	3B5	L4	3B6	L3	3B7	R5		
4B4	M6	4B5	M7	4B6	L7	4B7	L6		
5B4	K7	5B5	J7	5B6	J8	5B7	K6		
6B4	K4	6B5	K3	6B6	K5	6B7	J5		
7B4	G6	7B5	J1	7B6	H1	7B7	J2		
8B4	C3	8B5	C2	8B6	J3	8B7	H2		
9B4	F1	9B5	E2	9B6	F2	9B7	E3		
10B4	B5	10B5	B6	10B6	A5	10B7	A7		
11B4	B8	11B5	B2	11B6	B3	11B7	A4		
12B4	A9	12B5	A8	12B6	G8	12B7	F7		
13B4	E10	13B5	D10	13B6	C10	13B7	E6		
14B4	H8	14B5	G9	14B6	G10	14B7	F10		
15B4	F11	15B5	G12	15B6	G11	15B7	H12		
16B4	E15	16B5	D11	16B6	C11	16B7	E11		
17B4	G13	17B5	F14	17B6	A12	17B7	A13		
18B4	B17	18B5	B19	18B6	B18	18B7	C12		
19B4	A16	19B5	A14	19B6	B16	19B7	B15		
20B4	F19	20B5	E19	20B6	F20	20B7	E20		
21B4	J18	21B5	C19	21B6	C18	21B7	D19		
22B4	H20	22B5	J20	22B6	G15	22B7	H14		
23B4	K16	23B5	K18	23B6	K17	23B7	G16		
24B4	K12	24B5	K13	24B6	L12	24B7	L13		
25B4	M13	25B5	P17	25B6	N7	25B7	R17		
26B4	M17	26B5	M16	26B6	N13	26B7	N16		
27B4	L20	27B5	M19	27B6	L19	27B7	V20		
28B4	M18	28B5	P19	28B6	N18	28B7	P18		
29B4	T17	29B5	T18	29B6	U18	29B7	U17		
30B4	W15	30B5	W16	30B6	Y14	30B7	Y16		
31B4	V12	31B5	W18	31B6	V18	31B7	W17		

Power and Ground Pins

Pin Name	Pin Number	Description
V_{DD}	A2, A20, B1, E5, G14, P7, T16, W20, Y1, Y19	Power Supply
V_{SS}	A1, A19, B20, E16, G7, P14, T5, U5, W01, Y02, Y20, R15	Ground
NC	K10, V4,	No Connect
Spare[0:81]	J9, E4, F4, F3, D3, C16, D16, D17, C15, C17, F15, H17, F16, G17, R18, Y17, Y18, W11, Y11, W12, Y13, Y12, R14, P13, T13, R13, R12, U12, T12, T11, V11, U11, U14, T15, T14, P12, U13, N12, P11, N11, M12, R11, M9, N9, U7, U8, U6, T7, T6, V10, U10, T10, U9, T9, R9, T8, R8, R7, P8, Y8, Y9, Y10, W9, W10, V3, W4, Y4, W3, Y3, W8, V9, W7, V8, V7, Y6, Y7, Y5, W6, W5, V5, R6, V6	Tie to ground

ABSOLUTE MAXIMUM RATINGS

(Referenced to V_{SS})[1]

SYMBOL	PARAMETERS	VALUE	UNITS
V_{DD}	Supply voltage[2]	-0.3 to 4.8	V
V_{IO}	Input voltage any pin[2]	V_{SS}-0.3 to V_{DD}+0.3	V
V_{CH}	Input voltage any bussed pin[2]	V_{SS}-0.3 to V_{DD}+0.3	V
I_{IO}	Maximum dc I/O current any logic pin	-10 to 10	mA
P_D	Maximum power dissipation permitted @ T_C=125C[3]	5	W
T_J	Junction temperature	150	°C
θ_{JC}	Thermal resistance, junction to case	5	°C/W
T_{STG}	Storage temperature	-65 to 150	°C
ESD	ESD protection (human body model) Class 2	2000	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. All voltages are referenced to V_{SS}
3. Power dissipation capability depends on package characteristics and use environment.

RECOMMENDED OPERATING CONDITIONS
(Referenced to V_{SS})

SYMBOL	DESCRIPTION	CONDITIONS	VALUE	UNITS
V_{DD}	Supply voltage		3.0 to 3.6	V
V_{IN}	Input voltage any pin		0 to V_{DD}	V
T_C	Case operating temperature		-55 to 125	°C
t_R	Rise time, logic inputs	Transition from V_{IL} to V_{IH}	5	ns
t_F	Fall time, logic inputs	Transition from V_{IH} to V_{IL}	5	ns
I_{CH}	DC Continuous channel current		-60 to 60	mA

OPERATIONAL ENVIRONMENT

OPERATIONAL ENVIRONMENT		
PARAMETER	**LIMIT**	**UNITS**
TID	3.0E5	Rad(Si)
Single Event Latchup Immune (SEL)	≤100	MeV-cm^2/mg

POWER SUPPLY OPERATING CHARACTERISTICS (Pre and Post-Radiation)*
(V_{DD} = 3.3V ± 0.3V; $V_{SS} \leq V_{IN} \leq V_{DD}$; -55°C < T_C < 125°C); Unless otherwise noted, T_C is per the temperature range ordered

SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS
I_{DD}	Active supply current	V_{DD}=3.6V One SEL input toggling once per period.	--	1.2	mA/MHz
I_{DDS}	Standby supply current	V_{DD}=3.6V $\overline{CS}$=V_{DD}, $\overline{SDCS[1:0]}$=V_{DD}	-55°C & 25°C	25	uA
			125°C	250	

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up toup to the maximum TID level procured.

DC CHARACTERISTICS FOR LOGIC SIGNALS(Pre and Post-Radiation)*

(V_{DD} = 3.3V ± 0.3V; $V_{SS} \leq V_{IN} \leq V_{DD}$; -55°C < T_C < 125°C); Unless otherwise noted, T_C is per the temperature range ordered

SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS
V_{IH}	High-level input voltage	V_{DD} = 3.6V	2.0	--	V
V_{IL}	Low-level input voltage	V_{DD} =3.0V	--	0.8	V
I_{IN}	Input leakage current	$V_{IN}=V_{DD,}$ V_{DD} = 3.6V	--	1	uA
		$V_{IN}=V_{SS,}$ V_{DD} = 3.6V	-1	--	
C_{IN}[1]	Input capacitance	V_{DD}=0V *f*=1MHz	--	TBD	pF
C_{OUT}[1]	Output capacitance	V_{DD}=0V *f*=1MHz	--	TBD	pF

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up toup to o the maximum TID level procured.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.

DC CHARACTERISTICS FOR BUSSED SIGNALS (Pre and Post-Radiation)*

(V_{DD} = 3.3V ± 0.3V; $V_{SS} \leq V_{IN} \leq V_{DD}$; -55°C < T_C < 125°C); Unless otherwise noted, T_C is per the temperature range ordered

SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS
C_{ON1}[1]	Switch ON capacitance	Output is open *f*=1MHz, $0.1V_{DD} \leq V_i \leq 0.9V_{DD}$	--	25	pF
C_{ON2}[1]	Switch ON capacitance	Broadcast mode, all outputs open *f*=1MHz, $0.1V_{DD} \leq V_i \leq 0.9V_{DD}$	--	50	pF
C_{OFF1}[1]	Switch OFF capacitance at input *m*A	Output is open *f*=1MHz	--	19	pF
C_{OFF2}[1]	Switch OFF capacitance at output *m*B*n*	Input is open *f*=1MHz	--	2	pF
R_{ON}[2]	Switch ON resistance	$V_o=V_{SS}$, V_{DD}, and $V_{DD}/2$ I_{in}=40mA	--	12	Ω
$R_{ON(flat)}$[2]	Switch ON resistance flatness	$V_o=V_{SS}$, V_{DD}, and $V_{DD}/2$ I_{in}=-40mA	--	5	Ω
I_{OFF}	Switch OFF leakage current	$V_i=V_{SS}$ and $V_o=V_{DD}$, or $V_i=V_{DD}$ and $V_o=V_{SS}$	-2	2	uA
I_L	Leakage current for outputs with pull-up resistors (0B0-7B0, 0B1-7B1, 0B2-7B2, 0B3-7B3, 0B4-7B4, 0B5-7B5, 0B6-7B6, 0B7-7B7)	Output is off $V_o=V_{DD}$ $V_o=V_{SS}$	 -4 -100	 4 -60	 uA uA
I_{BHHL}[3]	Bus holder switch current high to low (8B0-31B0, 8B1-31B1, 8B2-31B2, 8B3-31B3, 8B4-31B4, 8B5-31B5, 8B6-31B6, 8B7-31B7)	Output is off	-500	-150	uA
I_{BHLH}[3]	Bus holder switch current low to high (8B0-31B0, 8B1-31B1, 8B2-31B2, 8B3-31B3, 8B4-31B4, 8B5-31B5, 8B6-31B6, 8B7-31B7)	Output is off	150	500	uA

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up toup to o the maximum TID level procured.

1. Guaranteed by design.
2. Guaranteed by device characterization.

3. Guaranteed by functional test only.

AC CHARACTERISTICS (Pre and Post-Radiation)*

(V_{DD} = 3.3V ± 0.3V; $V_{SS} \leq V_{IN} \leq V_{DD}$; -55°C < T_C < 125°C); Unless otherwise noted, T_C is per the temperature range ordered

Symbol	Description	Conditions	MIN	MAX	Units
$t_{P,BUS}$[1]	Bussed signals propagation delay	From any *m*A input to any *m*B*n* output	--	300	ps
t_{ON1}	Bussed signals ON time	From $\overline{CS}$ or SEL to any *m*B*n* output; $\overline{SDCS}$ static R_L=50Ω, C_L=50pF	1.7	5.2	ns
t_{OFF1}	Bussed signals OFF time	From $\overline{CS}$ or SEL to any *m*B*n* output; $\overline{SDCS}$ static R_L=50Ω, C_L=50pF	1.7	5.2	ns
t_{ON2}[2]	Bussed signals ON time	From $\overline{SDCS}$ to any *m*B*n* output; $\overline{CS}$ and SEL static R_L=50Ω, C_L=50pF	1.7	3.2	ns
t_{OFF2}[2]	Bussed signals OFF time	From $\overline{SDCS}$ to any *m*B*n* output; $\overline{CS}$ and SEL static R_L=50Ω, C_L=50pF	1.7	5.2	ns

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Not tested. The propagation delay through the channel is based upon the RC time constant of the maximum channel resistance and switch ON capacitance, 12Ω and 25pF.
2. Guaranteed by design

PARAMETER MEASUREMENT INFORMATION

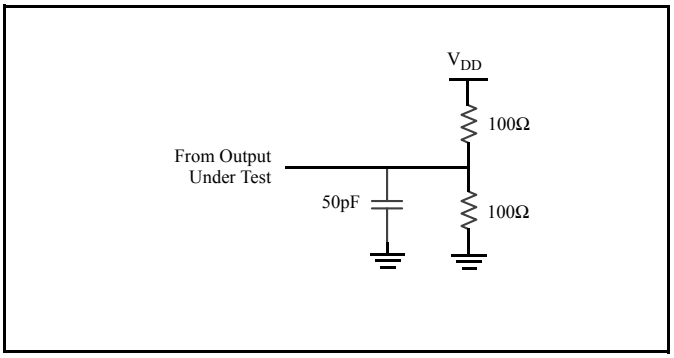


Figure 2. Load Circuit

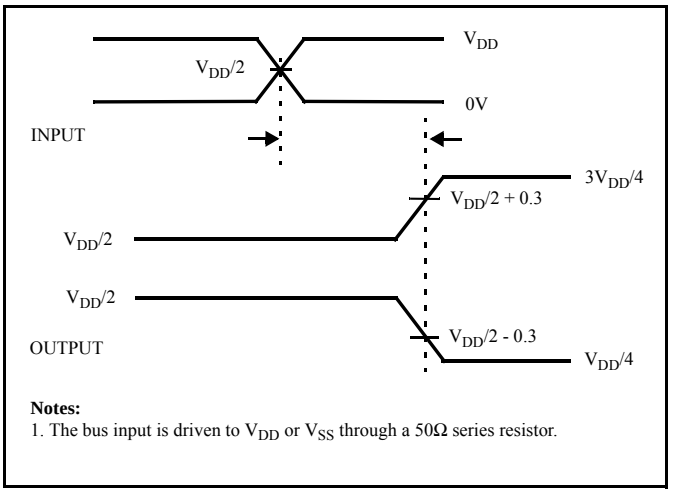


Figure 3. Bussed Signals Turn-on Time

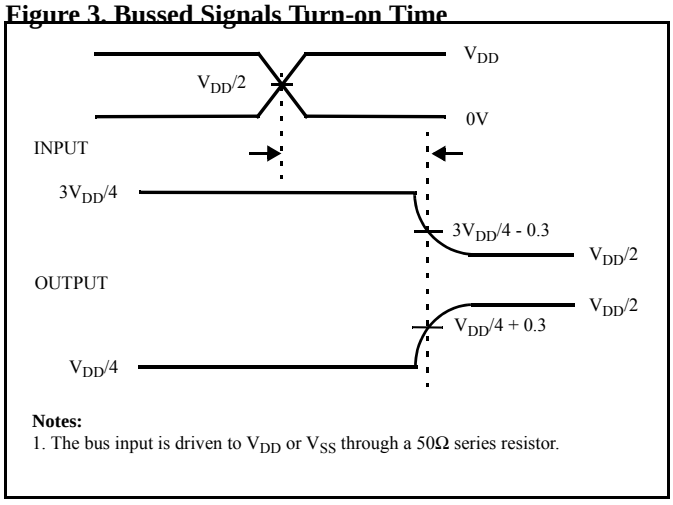


Figure 4. Bussed Signals Turn-off Time

PACKAGING

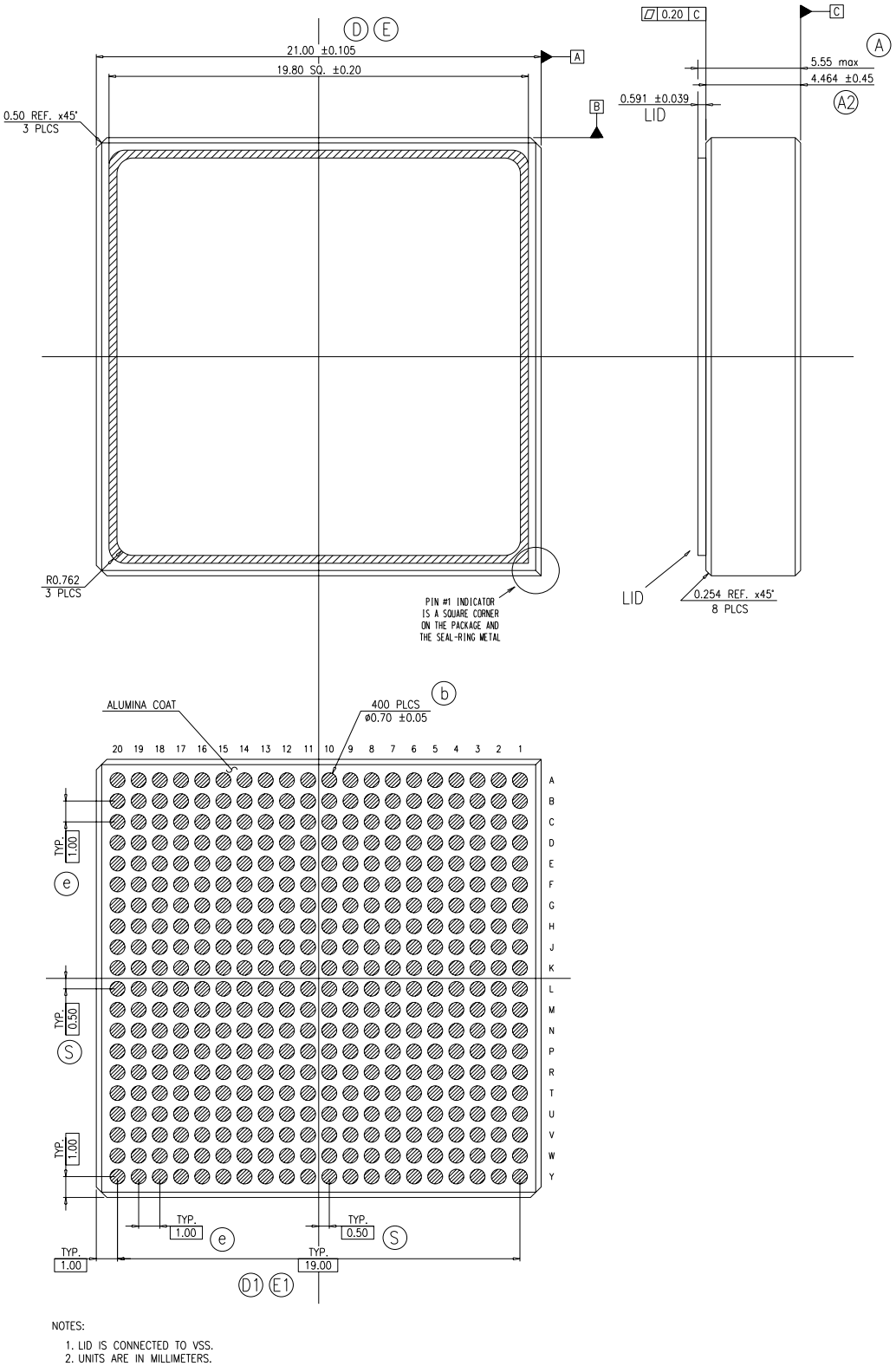


Figure 6: 400 pin Ceramic Land Grid Array Package (Case Outline Z)

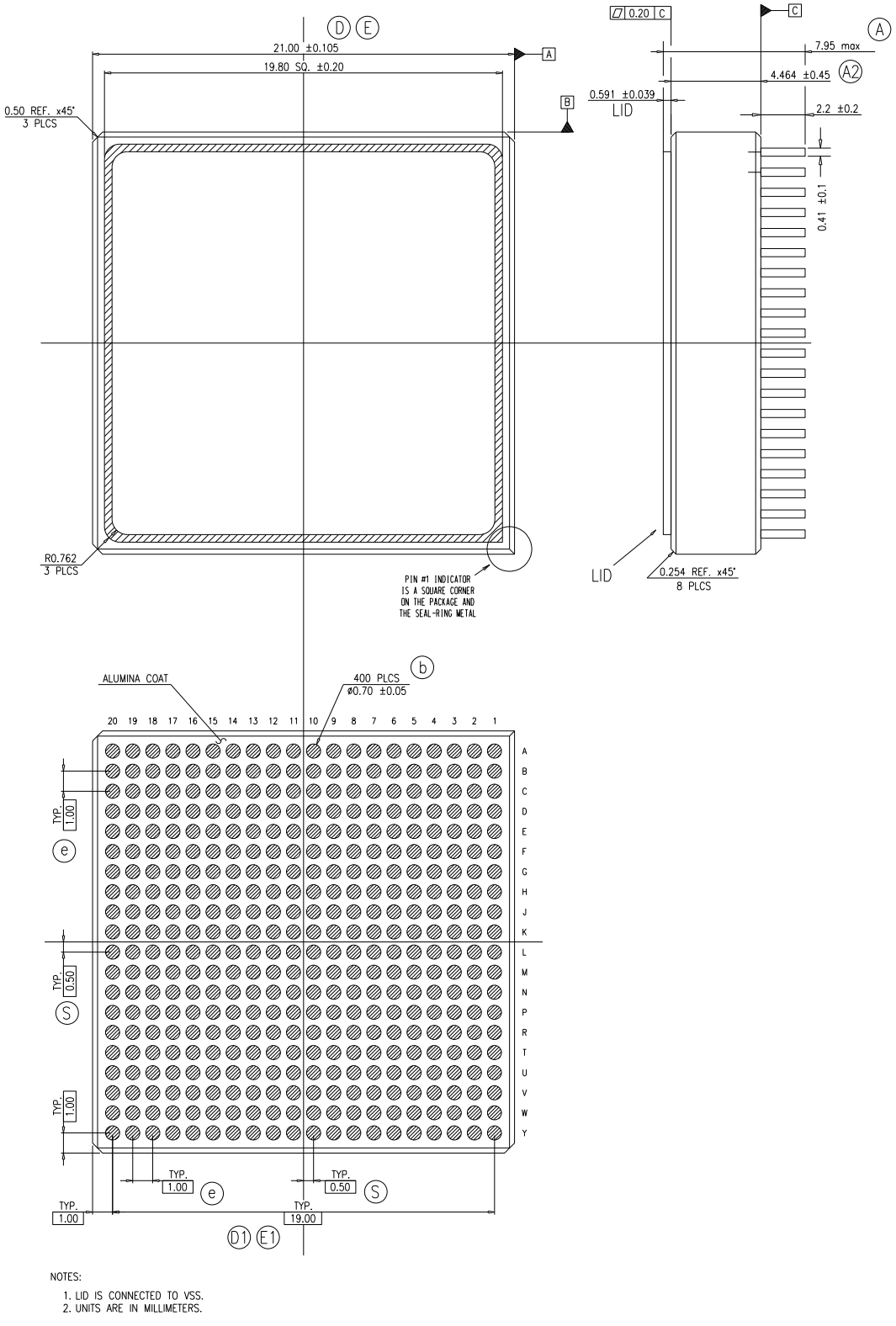
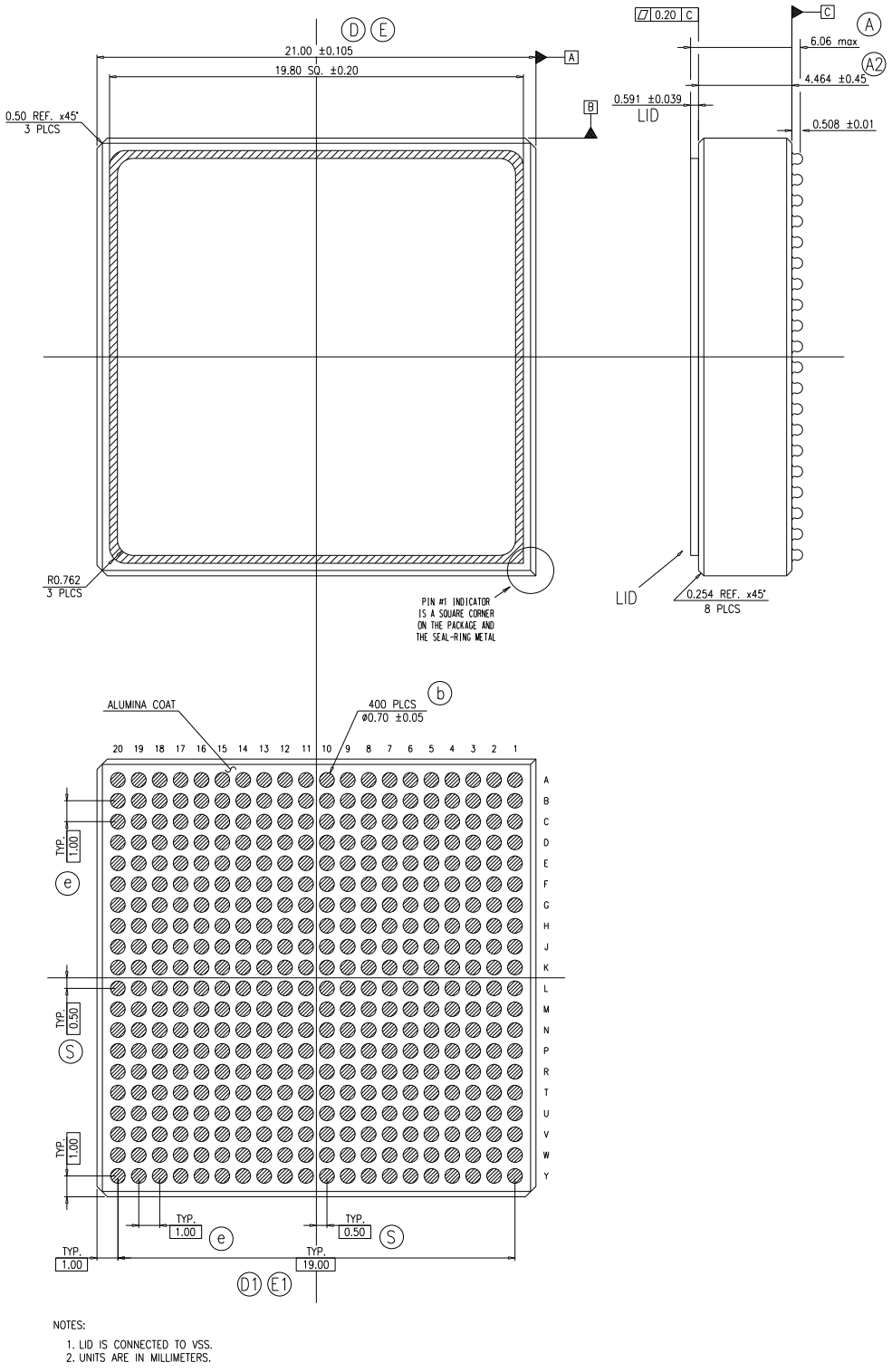


Figure 7. 400-pin Ceramic Column Grid Array Package (Case Outline S)



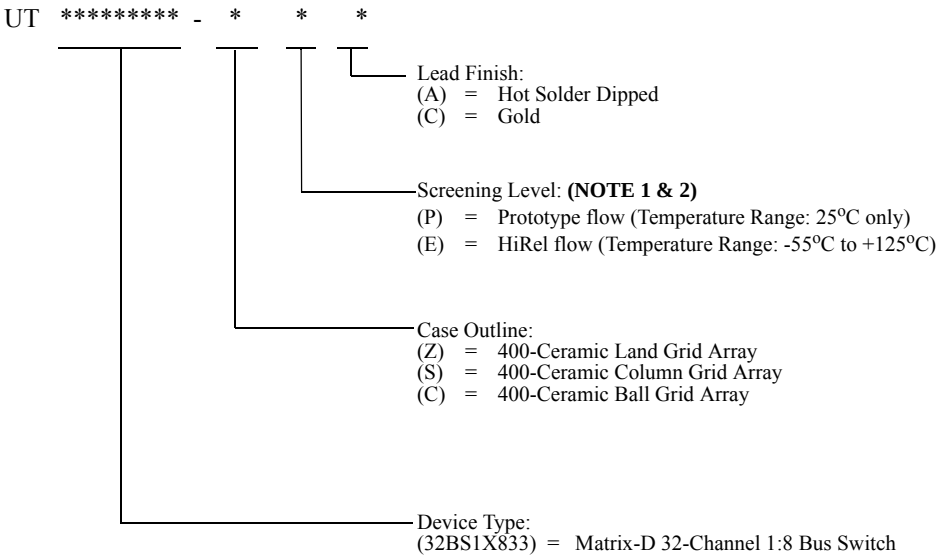
NOTES:

1. LID IS CONNECTED TO VSS.
2. UNITS ARE IN MILLIMETERS.

Figure 8. 400-pin Ceramic Ball Grid Array Package (Case Outline C)

ORDERING INFORMATION

UT32BS1X833 Matrix-D

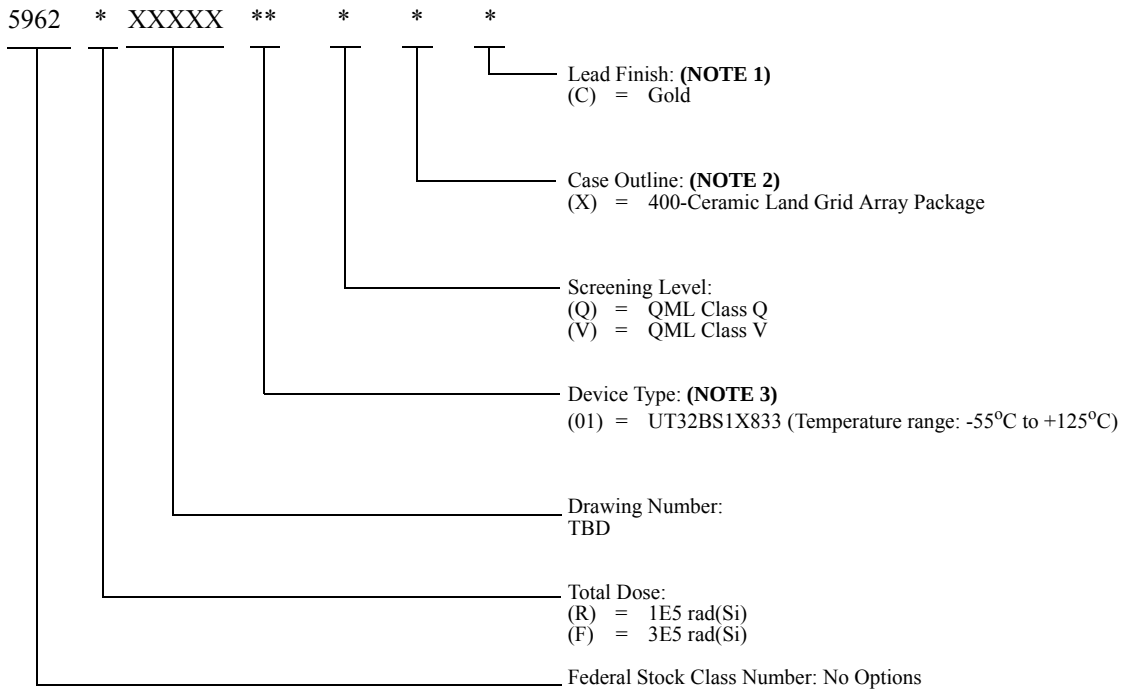


Notes:

1. Prototype Flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25°C only. Radiation is neither tested nor guaranteed.
2. HiRel Flow per Aeroflex Manufacturing Flows Document. Radiation is neither tested nor guaranteed.

Package Option	Associated Lead Finish
(Z) 400-CLGA	(C) Gold
(S) 400-CCGA	(A) Hot Solder Dipped
(C) 400-CBGA	(A) Hot Solder Dipped

UT32BS1X833 Matrix-D: SMD



Notes:

1. Lead finish is “C” (gold) only.
2. Aeroflex offers Column Attachment as an additional service for the Ceramic Land Grid Array (Case outline "Y"). If needed, please ask for COLUMN ATTACHMENT when submitting your request for quotation.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Government is required prior to the export of this product from the United States.

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AEROFLEX
A passion for performance.

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused