MIL-STD-1553

UT1553BCRTM Version B

Released Datasheet

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FEATURES

- Comprehensive MIL-STD-1553B dual-redundant Bus Controller (BC) and Remote Terminal (RT) and Monitor (M) functions
- MIL-STD-1773 compatible
- Multiple message processing capability in BC, RT and M modes
- Time-tagging and message logging in RT and M modes
- Automatic polling and intermessage delay in BC mode
- Programmable interrupt scheme and internally generated interrupt history list
- Register-oriented architecture to enhance programmability
- DMA or pseudo-dual-port memory interface with 64K addressability
- Internal wraparound self-test
- Remote terminal operations in ASD/ENASD-certified (SEAFAC)
- Architecturally and pin-compatible with UTMC's UT1553B BCRTM
- Available in 84-pin pingrid array and 84-lead flatpack
- Standard Microcircuit Drawing 5962-89577
- Available - QML Q

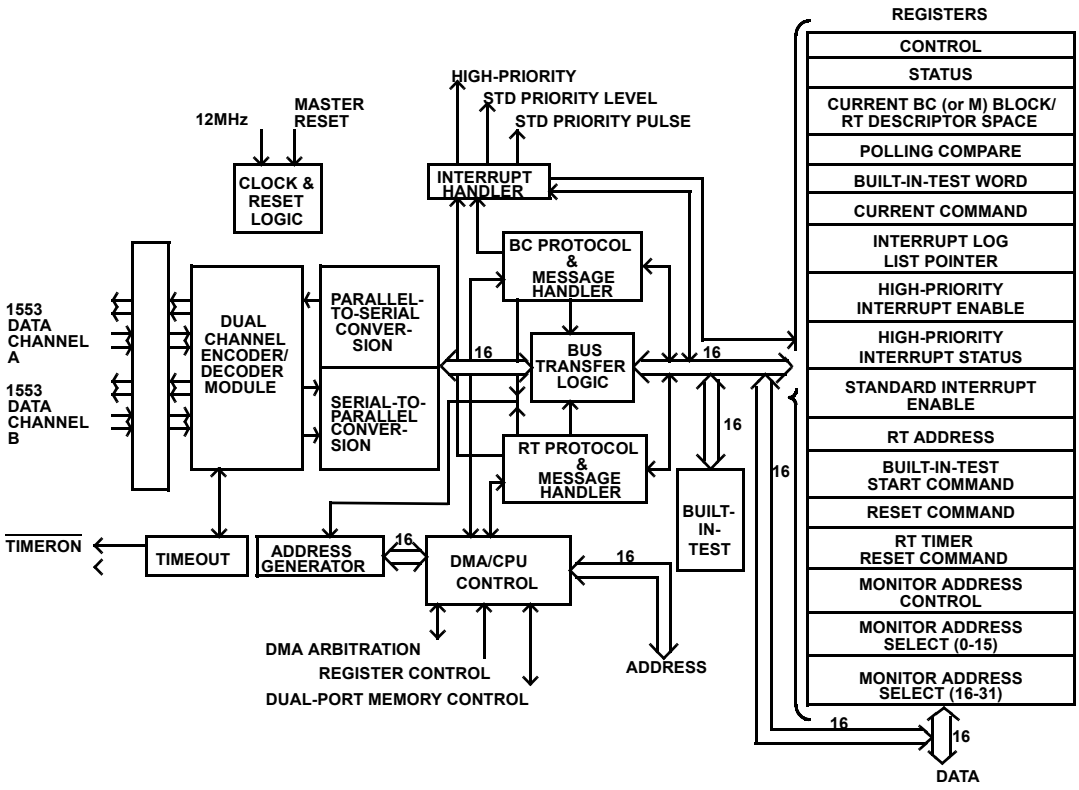

Figure 1. BCRTM Block Diagram

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1.0 INTRODUCTION

The monolithic CMOS UT1553 BCRTM provides the system designer with an intelligent solution to MIL-STD-1553B multiplexed serial data bus design problems. The UT1553B BCRTM is a single-chip device that implements all three of defined MIL-STD-1553B functions - Bus Controller, Remote Terminal, and Monitor. Designed to reduce host CPU overhead, the BCRTM's powerful state machines automatically execute message transfers, provide interrupts, and generate status information. Multiple registers offer many programmable functions as well as extensive information for host use. In the BC mode, the BCRTM uses a linked-list message scheme to provide the host with message chaining capability. The BCRTM enhances memory use by supporting variable-size, relocatable data blocks. In the RT mode, the BCRTM implements time-tagging and message history functions. It also supports multiple (up to 128) message buffering and variable length messages to any subaddress.In the Monitor (M) mode, the BCRTM's powerful linked list command block structure allows it to process a series of monitored 1553 messages without the intervention of the host. The BCRTM can store as much bus traffic as can be contained in its 64K memory space. In addition, the host has the capability of instructing the BCRTM to monitor and store data for only selected remote terminals.

The UT1553 BCRTM is an intelligent, versatile, and easy to implement device -- a powerful asset to system designers.

1.1 Features - Remote Terminal (RT) Mode

Indexing
The BCRTM is programmable to index or buffer messages on a subaddress-by-subaddress basis. The BCRTM, which can index as many as 128 messages, can also assert an interrupt when either the selected number of messages is reached or every time a specified subaddress is accessed.

Variable Space Allocation
The BCRTM can use as little or as much memory (up to 64K) as needed.

Selectable Data Storage
Address programmability within the BCRTM provides flexible data placement and convenient access.

Sequential Data Storage
The BCRTM stores/retrieves, by subaddress, all messages in the order in which they are transacted.

Sequential Message Status Information
The BCRTM provides message validity, time-tag, and word-count information, and stores it sequentially in a separate, cross-referenced list.

Illegalizing Mode Codes and Subaddresses
The host can declare mode codes and subaddresses illegal by setting the appropriate bit(s) in memory.

Programmable Interrupt Selection
The host CPU can select various events to cause an interrupt with provision for high and standard priority interrupts.

Interrupt History List
The BCRTM provides an Interrupt History List that records, in the order of occurrence, the events that caused the interrupts. The list length is programmable.

1.2 Features - Bus Controller (BC) Mode

Multiple Message Processing
The BCRTM autonomously processes any number of messages or lists of messages that may be stored in a 64K memory space.

Automatic Intermessage Delay
When programmed by the host, the BCRTM can delay a host-specified time before executing the next message in sequence.

Automatic Polling
When polling, the BCRTM interrogates the remote terminals and then compares their status word responses to the contents of the Polling Compare Register. The BCRTM can interrupt the host CPU if an erroneous remote terminal status word response occurs.

Automatic Retry
The BCRTM can automatically retry a message on busy, message error, and/or response time-out conditions. The BCRTM can retry up to four times on the same or on the alternate bus.

Programmable Interrupt Selection
The host CPU can select various events to cause an interrupt with provision for high and standard priority interrupts.

Interrupt History List
The BCRTM provides an Interrupt History List that records, in the order of occurrence, the events that caused the interrupts. The list length is program- mable.

Variable Space Allocation
The BCRTM uses as little or as much memory (up to 64K) as needed.

Selectable Data Storage
Address programmability within the BCRTM provides flexible data placement and convenient access.

1.3 Features - Monitor (M) Mode

Command History List
The BCRTM's linked list command block structure permits the BCRTM to process a series of monitored messages without host intervention.

Monitor Selected Terminal Address
The host can select the remote terminals to be monitored by programming the proper bits in the Terminal Address Select registers (Registers16 and 17). The BCRTM can monitor any or all remote terminals.

Variable Space Allocation
The BCRTM can use as little or as much memory (up to 64K) as needed

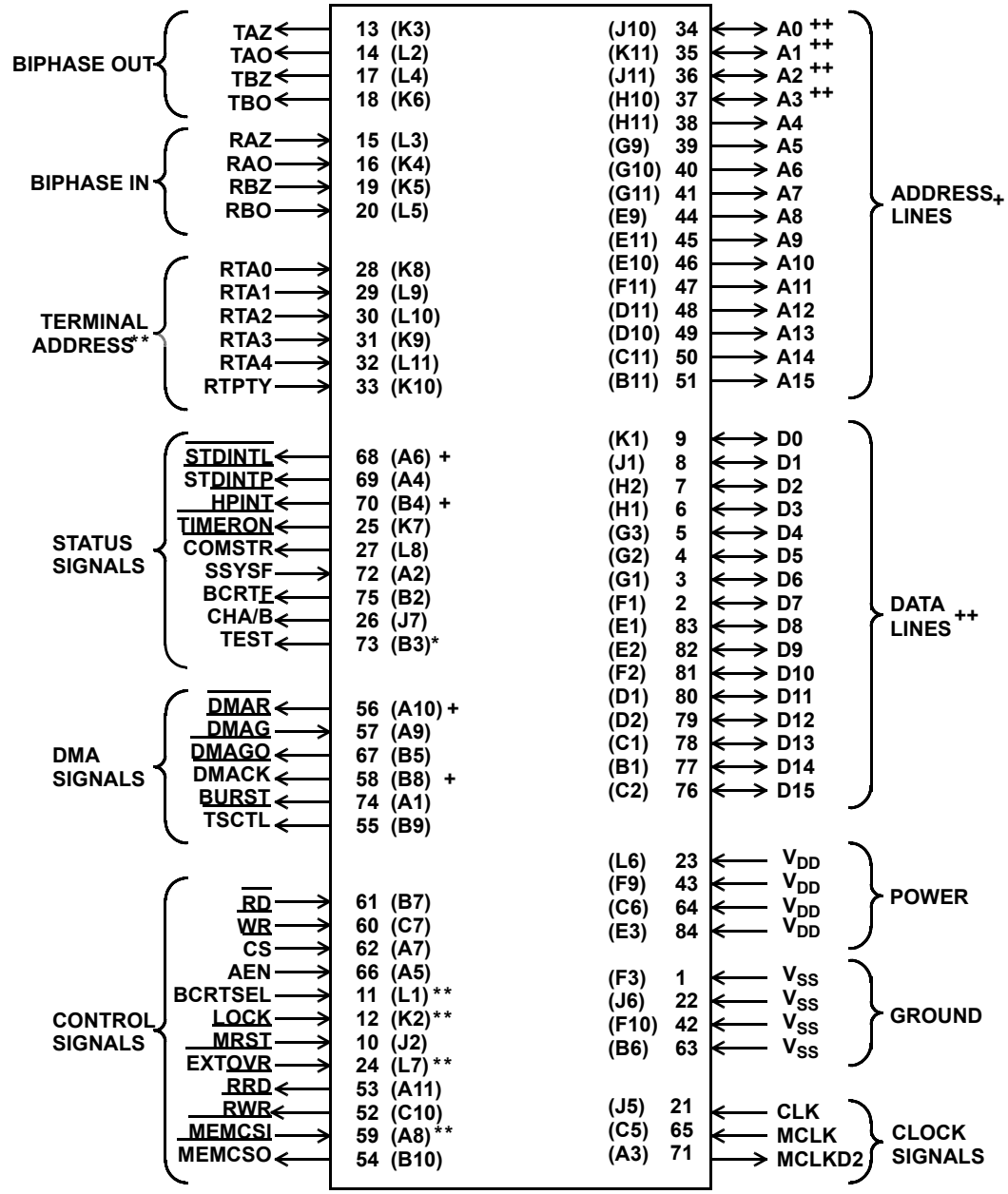
Selectable Data Storage
Address programmability within the BCRTM provides flexible data placement and convenient access.

Sequential Data Storage
The BCRTM stores, by Terminal Address, all 1553 messages in the order in which they are transacted.

Programmable Interrupt Selection
The host can select a wide variety of events that may cause an interrupting event.

Interrupt History List
The BCRTM stores, chronologically in memory, an Interrupt History List of each event that causes an interrupt.

2.0 PIN IDENTIFICATION AND DESCRIPTION



** Pin internally pulled up.
\+ Pin at high impedance when not asseted
++ Bidirectional pin.
* Formerly MEMWIN.

( ) Pingrid arraylead identification in parentheses.
LCC, flatpack pin number not in parentheses.

Figure 2a. BCRTM 84-lead Functional Pin Description

Legend for TYPE and ACTIVE fields:
TUI = TTL input (pull-up)
AL = Active low
AH = Active high
ZL = Active low - inactive state is high impedance
TI = TTL input
TO = TTL output
TTO = Three-state TTL output
TTB = Bidirectional

Notes:
1. Address and data buses are in the high-impedance state when idle.

ADDRESS BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
A0	34	J10	TTB	--	Bit 0 (LSB) of the Address Bus
A1	35	K11	TTB	--	Bit 1 of the Address Bus
A2	36	J11	TTB	--	Bit 2 of the Address Bus
A3	37	H10	TTB	--	Bit 3 of the Address Bus
A4	38	H11	TTO	--	Bit 4 of the Address Bus
A5	39	G9	TTO	--	Bit 5 of the Address Bus
A6	40	G10	TTO	--	Bit 6 of the Address Bus
A7	41	G11	TTO	--	Bit 7 of the Address Bus
A8	44	E9	TTO	--	Bit 8 of the Address Bus
A9	45	E11	TTO	--	Bit 9 of the Address Bus
A10	46	E10	TTO	--	Bit 10 of the Address Bus
A11	47	F11	TTO	--	Bit 11 of the Address Bus
A12	48	D11	TTO	--	Bit 12 of the Address Bus
A13	49	D10	TTO	--	Bit 13 of the Address Bus
A14	50	C11	TTO	--	Bit 14 of the Address Bus
A15	51	B11	TTO	--	Bit 15 (MSB) of the Address Bus

DATA BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
D0	9	K1	TTB	--	Bit 0 (LSB) of the Data Bus
D1	8	J1	TTB	--	Bit 1 of the Data Bus
D2	7	H2	TTB	--	Bit 2 of the Data Bus
D3	6	H1	TTB	--	Bit 3 of the Data Bus
D4	5	G3	TTB	--	Bit 4 of the Data Bus
D5	4	G2	TTB	--	Bit 5 of the Data Bus
D6	3	G1	TTB	--	Bit 6 of the Data Bus
D7	2	F1	TTB	--	Bit 7 of the Data Bus
D8	83	E1	TTB	--	Bit 8 of the Data Bus
D9	82	E2	TTB	--	Bit 9 of the Data Bus
D10	81	F2	TTB	--	Bit 10 of the Data Bus
D11	80	D1	TTB	--	Bit 11 of the Data Bus
D12	79	D2	TTB	--	Bit 12 of the Data Bus
D13	78	C1	TTB	--	Bit 13 of the Data Bus
D14	77	B1	TTB	--	Bit 14 of the Data Bus
D15	76	C2	TTB	--	Bit 15 (msb) of the Data Bus

TERMINAL ADDRESS INPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
RTA0	28	K8	TUI	--	Remote Terminal Address Bit 0 (LSB). The entire RT address is strobed in at Master Reset. Verify it by reading the Remote Terminal Address Register. All the Remote Terminal Address bits are internally pulled up.
RTA1	29	L9	TUI	--	Remote Terminal Address Bit 1. This is bit 1 of the Remote Terminal Address.
RTA2	30	L10	TUI	--	Remote Terminal Address Bit 2. This is bit 2 of the Remote Terminal Address.
RTA3	31	K9	TUI	--	Remote Terminal Address Bit 3. This is bit 3 of the Remote Terminal Address.
RTA4	32	L11	TUI	--	Remote Terminal Address Bit 4. This is bit 4 (MSB) of the Remote Terminal Address.
RTPTY	33	K10	TUI	--	Remote Terminal (Address) Parity. This is odd of the Remote Terminal Address.

CONTROL SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
$\overline{RD}$	61	B7	TI	AL	Read. The host uses this in conjunction with $\overline{CS}$ to read an internal BCRTM register.
$\overline{WR}$	60	C7	TI	AL	Write. The host uses this in conjunction with $\overline{CS}$ to write an internal BCRTM register.
$\overline{CS}$	62	A7	TI	AL	Chip Select. This selects theBCRT when accessing the BCRTM 's internal register.
AEN	66	A5	TI	AH	Address Enable. The host CPU uses AEN to indicate to the BCRTM that the BCRTM 's addresslines can be asserted; this is a precautionary signal provided to avoid address bus crash. If not used, it must be tied high.
BCRTSEL	11	L1	TUI	--	BC/$\overline{RT}$ Select. This selects between either the Bus Controller or Remote Terminal mode. The BC/RT Mode Select bit in the Control Register overrides this input if the Lock pin is not high. This pin is internally pulled high.
LOCK	12	K2	TUI	AH	Lock. When set, this pin prevents internal changes to both the RT address and BC/RT mode select functions. This pin is internally pulled high.
$\overline{EXTOVR}$	24	L7	TUI	AL	External Override. Use this in multi-redundant applications. Upon receipt, the BCRTM aborts all current activity. $\overline{EXTOVR}$ should be connected to COMSTR output of the adjacent BCRTM when used. This pin is internally pulled high.
$\overline{MRST}$	10	52	TI	AL	Master Reset. This resets all internal state machines, encoders, decoders, and registers. The minimum pulse width for a successful Master Reset is 500ns.
$\overline{MEMCSO}$	54	B10	TO	AL	Memory Chip Select Out. This is the regenerated $\overline{MEMCSI}$ inout for external RAM during the pseudo-dual-port RAM mode. The BCRTM also uses it to select external memory during memory accesses.
$\overline{MEMCSI}$	59	A8	TUI	AL	Memory Chip Select In. Used in the pseudo-dual-port RAM mode only, $\overline{MEMCSI}$ is received from the host and is propagated through to MEMCSO.
$\overline{RRD}$	53	A11	TO	AL	RAM Read. In the pseudo-dual-port RAM mode, the host uses this signal in conjunction with MEMCSO to read from external RAM through the BCRTM . It is also the signal the BCRTM uses to read from memory. It is asserted following receipt of DMAG. When the BCRTM performs multiple reads, this signal is pulsed.
$\overline{RWR}$	52	C10	TO	AL	RAM Write. In the pseudo-dual-port RAM mode, the CPU and BCRTM use this to write to external RAM. This signal is asserted following receipt of DMAG. For multiple writes, this signal is pulsed.

CONTROL SIGNALS Cont'd

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
$\overline{\text{STDINTL}}$	68	A6	TTO	ZL	Standard Interrupt Level. This is a level interrupt. It is asserted when one or more events enabled in either the Standard Interrupt Enable Register, RT Descriptor, or BC Command Block occur. Resetting the Standard Interrupt bit in the High-Priority Interrupt Status/Reset Register clears the interrupt.
$\overline{\text{STDINTP}}$	69	A4	TO	AL	Standard Interrupt Pulse. $\overline{\text{STDINTP}}$ pulses when an interrupt is logged.
$\overline{\text{HPINT}}$	70	B4	TTO	ZL	High-Priority Interrupt. The High Priority Interrupt level is asserted upon occurance of events enabled in the High-Priority Interrupt Enable Register. The corresponding bit(s) in the High-Priority Interrupt Status/Reset Register reset $\overline{\text{HPINT}}$.
$\overline{\text{TIMERON}}$	25	K7	TO	AL	(RT) Timer On. This is a 760-microsecond fail-safe transmitter enable timer. Started at the beginning of a transmission, $\overline{\text{TIMERON}}$ goes inactive 760 microseconds later or is reset automatically with the receipt of a new command. Use it in conjunction with CHA/B output to provide a fail-safe timer for Channels A and B transmitters.
$\overline{\text{COMSTR}}$	27	L8	TO	AL	(RT) Command Strobe. The BCRTM asserts this signal after receiving a valid command. The BCRTM deactivates it after servicing the command.
SSYSF	72	A2	TI	AH	(RT) Command Strobe. The BCRTM asserts this signal after receiving a valid command. The BCRTM deactivates it after servicing the command.
BCRTF	75	B2	TO	AH	BCRTM Fail. This indicates a Built-in-Test (BIT) failure. In the RT mode, the Terminal Flag bit in 1553 status word is also set.
CHA/$\overline{\text{B}}$	26	59	TO	--	Channel A/$\overline{\text{B}}$. This indicates the active or last active channel.
TEST	73	B3	TO	AL	BCRTM Fail. This indicates a Built-in-Test (BIT) failure. In the RT mode, the Terminal Flag bit in 1553 status word is also set.

BIPHASE INPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
RAO	16	K4	TI	--	Receive Channel A One. This is the Manchester-encoded true signal input from Channel A of the bus receiver.
RAZ	15	L3	TI	--	Receive Channel A Zero. This is the Manchester-encoded complementary signal input from Channel A of the bus receiver.
RBO	20	L5	TI	--	Receive Channel B One. This is the Manchester-encoded true signal input from Channel B of the bus receiver.
RBZ	19	K5	TI	--	Receive Channel B Zero. This is the Manchester-encoded complementary signal input from Channel B of the bus receiver.

BIPHASE OUTPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
TAO	14	L2	TO	--	Transmit Channel A One. This is the Manchester-encoded true output to be connected to the Channel A bus transmitter input. This signal is idle low.
TAZ	13	K3	TO	--	Transmit Channel A Zero. This is the Manchester-encoded complementary output to be connected to the Channel A bus transmitter input. This signal is idle low.
TBO	18	K6	TO	--	Transmit Channel B One. This is the Manchester-encoded true output to be connected to the Channel B bus transmitter input. This signal is idle low.
TBZ	17	L4	TO	--	Transmit Channel B Zero. This is the Manchester-encoded complementary output to be connected to the Channel B bus transmitter input. This signal is idle low.

DMA SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
$\overline{\text{DMAR}}$	56	A10	TTO	ZL	DMA Request. The BCRTM issues this signal when access to RAM is required. It goes inactive after receiving a DMAG signal.
$\overline{\text{DMAG}}$	57	A9	TI	AL	DMA Grant. This input to the BCRTM allows the BCRTM to access RAM. It is recognized 45ns before the rising edge of MCLKD2.
$\overline{\text{DMAGO}}$	67	B5	TO	AL	DMA Grant Out. If $\overline{\text{DMAG}}$ is received but not needed, it passes through to this output.
$\overline{\text{DMACK}}$	58	B8	TTO	ZL	DMA Acknowledge. The BCRTM asserts this signal to confirm receipt of DMAG, it stays low until memory access is complete.
BURST	74	A1	TO	AH	Burst (DMA Cycle). This indicates that the current DMA cycle transfers at least two words; worst case is five words plus a "dummy" word.
$\overline{\text{TSCTL}}$	55	B9	TO	AL	Three-State Control. This signal indicates when the BCRTM is actually accessing memory. The host subsystem's address and data lines must be in the high-impedance state when the signals active. This signal assists in placing the external data and address buffers into the high-impedance state.

CLOCK SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
CLK	21	J5	TI	--	Clock. The 12MHz input clock requires a 50% ± 10% duty cycle with an accuracy of ± 0.01%. The accuracy is required in order to meet the Manchester encoding/decoding requirements of MIL-STD-1553B.
MCLK	65	C5	TI	--	Memory Clock. This is the input clock frequency the BCRTM uses for memory accesses. The memory cycle time is equal to two MCLK cycles. Therefore, RAM access time is dependent upon the chosen MCLK frequency (6MHz minimum, 12MHz maximum). Please see the BCRTM DMA timing diagrams in this chapter.
MCLKD2	71	A3	TO	--	Memory Clock Divided by Two. This signal is the Memory Clock input divided by two. It assists the host subsystem in synchronizing DMA events.

POWER AND GROUND

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	FP	PGA			
VDD	23, 43, 64, 84	L6, F9, C6, 'E3	PWR	--	+5V
VSS	1, 22, 42, 63	F3, J6, F10, B6	GND	--	Ground

3.0 INTERNAL REGISTERS

The BCRTM's internal registers (see table 1 on pages 19-20) enable the CPU to control the actions of the BCRTM while maintaining low DMA overhead by the BCRTM. All functions are active high and ignored when low unless stated otherwise. Functions and parameters are used in both RT and BC modes except where indicated. Registers are addressed by the binary equivalent of their decimal number. For example, Register 1 is addressed as 0001B. Register usage is defined as follows:

#0 Control Register

Bit Number	Description
BIT 15	Reserved.
BIT 14	Rt Address 31. When RT31=0, the BCRTM recognizes RT Address 31 as a Broadcast command. When RT31=1,the BCRTM treats RT Address 31 as a normal terminal address.
BIT 13	Subaddress 31. When SA31=0, the BCRTM recognizes a command word with either subaddress 0 or 31 as being a valid code. When SA31=1, the BCRTM only recognizes a command word with a subaddress of 0 as a valid mode code.
BIT 12	Bus Controller Time out. When the BCRTM is a BC and BCTO=0, the BCRTM allows an RT up to 16us to respond with a status word before it declares a bus time-out. If BCTO=1, the BCRTM allows an RT up to 32us to respond with a status word before it declares a bus time-out. In the remote terminal mode of operation, this bit controls to RT to RT response time-out. To support the requirements of MIL-STD-1553B, this bit is set to a logical zero.
BIT 11	Enable External Override. For use in multi-redundant systems. This bit enables the $\overline{\text{EXTOVR}}$ pin.
BIT 10	BC/$\overline{\text{RT}}$ Select. This function selects between the Bus Controller and Remote Terminal/Monitor operation modes. It overrides the external BCRTSEL input setting if the Change Lock-Out function is not used. A reset operation must be performed when changing between BC and RT/M modes. For monitor operation this bit must be "0". This bit is write-only.
BIT 9	(BC) Retry on Alternate Bus. This bit enables an automatic retry to operate on alternate buses. For example, if on bus A, with two automatic retries programmed, the automatic retries occur on bus B.
BIT 8	(RT,M) Channel B Enable. When set, this bit enables Channel B operation. (BC) No significance.
BIT 7	(RT,M) Channel A Enable. When set, this bit enables Channel A operation. (BC) Channel Select A/$\overline{\text{B}}$. When set, this bit selects Channel A.
BITs 6-5	(BC) Retry Count. These bits program the number (1-4) of retries to attempt. (00 = 1 retry, 11 = 4 retries)
BIT 4	(BC) Retry on Bus Controller Message Error. This bit enables automatic retries on an error the Bus Controller detects (see the Bus Controller Architecture section, page 29).
BIT 3	(BC) Retry on Time-Out. This bit enables an automatic retry on a response time-out condition.
BIT 2	(BC) Retry on Message Error. This bit enables an automatic retry when the Message Error bit is set in the RT's status word response.
BIT 1	(BC) Retry on Busy. This bit enables automatic retry on a received Busy bit in an RT status word response.
BIT 0	Start Enable. In the BC mode, this bit starts/restarts Command Block execution. In the RT or M mode, It enables the BCRTM to receive a valid command. RT operation does not start until a valid command is received. When using this function: • Restart the BCRTM after each Master Reset or programmed reset. • This bit is not readable; verify operation by reading bit 0 of the BCRTM's Status Register.

#1 Status Register (Read Only)

These bits indicate the BCRTM's current status.

Bit Number	Description
BIT 15	TEST. This bit reflects the inverse of the TEST output. It changes state simultaneously with the TEST output.
BIT 14	(RT,M) Remote Terminal (or Monitor) Active. Indicates that the BCRTM, in the Remote Terminal (or Monitor) mode, is presently servicing a command. This bit reflects the inverse of the $\overline{\text{COMSTR}}$ pin.

BIT 13 (RT) Dynamic Bus Control Acceptance. This bit reflects the state of the Dynamic Bus Control Acceptance bit in the RT status word (see Register 10 on page 17).

BIT 12 (RT) Terminal Flag bit is set in RT status word. This bit reflects the result of writing to Register 10, bit 11

BIT 11 (RT) Service Request bit is set in RT status word.This bit reflects the result of writing to Register 10, bit 10.

BIT 10 (RT) Busy bit is set in RT status word.This bit reflects the result of writing to Register 10, bits 9 or 14.

BIT 9 BIT is in progress.

BIT 8 Reset is in progress. This bit indicates that either a write to Register 12 has just occurred or the BCRTM has just received a Reset Remote Terminal (#01000) Mode Code. This bit remains set less than 1ms.

BIT 7 BC/($\overline{RT}$) Mode. Indicates the current mode of operation. A reset operation must be performed when changing between BC and RT modes.

BIT 6 Channel A/$\overline{B}$. Indicates either the channel presently in use or the last channel used.

BIT 5 Subsystem Fail Indicator. Indicates receiving a subsystem fail signal from the host subsystem on the SSYSF input.

BITs 4-1 Reserved.

BIT 0 (BC) Command Block Execution is in progress. (RT) Remote Terminal is in operation. This bit reflects bit 0 of Register 0.

#2 Current Command Block Register (BC,M)/Remote Terminal Descriptor Space Address Register (RT)
(BC) This register contains the address of the head pointer of the Command Block being executed. Accessing a new Command Block updates it.

(RT) The host CPU initializes this register to indicate the starting location of the RT Descriptor Space. The host must allocate 320 sequential locations following this starting address. For proper operation, this location must start on an I x 512 decimal address boundary, where I is an integer multiple.

(M) This register contains the address of the control/status word of the current Monitor Command Block. Accessing a new Command Block updates it.

#3 Polling Compare Register
In the polling mode, the CPU sets the Polling Compare Register to indicate the RT response word on which the BCRTM should interrupt. This register is 11 bits wide, corresponding to bit times 9 through 19 of the RT's 1553 status word response. The sync, Remote Terminal Address, and parity bits are not included (see the section on Polling, page 32).

#4 BIT (Built-In-Test) Word Register
The BCRTM uses the contents of this register when it responds to the Transmit BIT Word Mode Code (#10011). In addition, the BCRTM writes to the two most significant bits of the BIT Word Register in response to either an Initiate Self-Test Mode Code (RT mode) or a write to Register 11 (BIT Start Command) to indicate a BIT failure. If the BIT Word needs to be modified, it can be read out, modified, then rewritten to this register. Note that if the processor writes a "1" to either bit 14 or 15 of this register, it effectively induces a BIT failure.

Bit Number	Description
BIT 15	Channel B failure.
BIT 14	Channel A failure.
BIT 13-0	BIT Word. The least significant fourteen bits of the BIT Word are user programmable.

#5 Current Command Register (Read Only)
In the RT or Monitor mode, this register contains the command currently being processed. When not processing a command, the BCRTM stores the last command or status word transmitted on the 1553B bus in this register. This register is updated only when bit 0 of Register 0 is set. In the BC mode, this register contains the most current command sent out on the 1553B bus.

#6 Interrupt Log List Pointer Register
Initialized by the CPU, the Interrupt Log List Pointer Register indicates the start of the Interrupt Log List. After each list entry, the BCRTM updates this register with the address of the next entry in the list. (See page 38.)

#7 High-Priority Interrupt Enable Register (Read/Write)
Setting the bits in this register causes a High-Priority Interrupt when the enabled event occurs. To service the High-Priority Interrupt, the user reads Register 8 to determine the cause of the interrupt, then writes to Register 8 to clear the appropriate bits. The BCRTM also provides a Standard Priority Interrupt Scheme that does not require host intervention. If High-Priority Interrupt service is not possible in a given application, it is advisable to use the Standard Priority features.

Bit Number	Description
BITs 15-9	Reserved.
BIT 8	Data Overrun Enable. When set, this bit enables an interrupt when $\overline{\text{DMAG}}$ was not received by the BCRTM within the allotted time needed for a successful data transfer to memory.
BIT 7	(BC) Illogical Command Error Enable. This bit enables a High-Priority Interrupt to be asserted upon the occurrence of an Illogical Command. Illogical commands include incorrectly formatted RT-RT Command Blocks.
BIT 6	(RT) Dynamic Bus Control Mode Code Interrupt Enable. When set, an interrupt is asserted when the Dynamic Bus Control Mode Code is received.
BIT 5	Subsystem Fail Enable. When set, a High-Priority Interrupt is asserted after receiving a Subsystem Fail (SSYSF) input pin.
BIT 4	End of BIT Enable. This bit indicates the end of the internal BIT routine.
BIT 3	BIT Word Fail Enable. This bit enables an interrupt indicating that the BCRTM detected a BIT failure.
BIT 2	(BC) End of Command Block List Enable (see Command Block Control Word, page 31.) This interrupt can be superseded by other high-priority interrupts.
BIT 1	Message Error Enable. If enabled, a High-Priority Interrupt is asserted at the occurrence of a message error. If a High-Priority Interrupt condition occurs, as the result of an enabled message error, the device will halt operation until the user clears the interrupt by writing a "1" to Bit 1 of the High-Priority Interrupt Status/Reset Register (Reg. #8). If this interrupt is not cleared, the BCRTM remains in the HALTED state (appearing to be "locked up"), even if it receives a valid message. This High-Priority Interrupt scheme is necessary in order to maintain the BCRTM's state of operation so that the host CPU has this information available at the time of interrupt service.
BIT 0	Standard Interrupt Enable. Setting this bit enables the $\overline{\text{STDINTL}}$ pin, but does not cause a high-priority interrupt. If low, only the STDINTL pin is asserted when a Standard Interrupt occurs.

#8 High-Priority Interrupt Status/Reset Register

When a High-Priority Interrupt is asserted, this register indicates the event that caused it. To clear the interrupt signal and reset the bit, write a "1" to the appropriate bit. See the corresponding bit definitions of Register 7, High-Priority Interrupt Enable Register.

Bit Number	Description
BITs 15-9	Reserved.
BIT 8	Data Overrun.
BIT 7	Illogical Command.
BIT 6	Dynamic Bus Control Mode Received
BIT 5	Subsystem Fail.
BIT 4	End of BIT.
BIT 3	BIT Word Fail.
BIT 2	End of Command Block.
BIT 1	Message Error.
BIT 0	Standard Interrupt. The BCRTM sets this bit when any Standard Interrupt occurs, providing bit 0 of Register 7 is enabled.(Reset STDINTL output.)

#9 Standard Interrupt Enable Register

This register enables Standard Interrupt logging for any of the following enabled events (Standard Interrupt logging can also occur for events enabled in the BC Command Block or RT Subaddress/Mode Code Descriptor):

Bit Number	Description
BITs 15-6	Reserved.
BIT 5	(RT) Illegal Broadcast Command. When set, this bit enables an interrupt indicating that an Illegal Broadcast Command has been received.
BIT 4	(RT) Illegal Command. When set, this bit enables an interrupt indicating that an illegal command has been received.
BIT 3	(BC) Polling Comparison Match. This enables an interrupt indicating that a polling event has occurred. The user must also set bit 12 in the BC Command Block Control Word for this interrupt to occur.
BIT 2	(BC) Retry Fail. This bit enables an interrupt indicating that all the programmed number of retries have failed.
BIT 1	(BC, RT,M) Message Error Event. This bit enables a standard interrupt for message errors.
BIT 0	(BC,M) Command Block Interrupt and Continue. This bit enables an interrupt indicating that a Command Block, with the Interrupt and Continue Function enabled, has been executed.

#10 Remote Terminal Address Register

This register sets the Remote Terminal Address via software. The Change Lock-Out Enable feature, when set, prevents the Remote Terminal Address or the BCRTM Mode Selection from changing.

Bit Number	Description
BIT 15	(RT) Instrumentation. Setting this bit sets the RT status word Instrumentation bit.
BIT 14	(RT) Busy. Setting this bit sets the RT status word Busy bit. It does not inhibit data transfers to the subsystem.
BIT 13	(RT) Subsystem Fail. Setting this bit sets the RT status word Subsystem Flag bit. In the RT mode, the Subsystem Fail is also logged into the Message Status Word.
BIT 12	(RT) Dynamic Bus Control Acceptance. Setting this bit sets the RT status word Dynamic Bus Control Acceptance bit when the BCRTM receives the Dynamic Bus Control Mode Code from the currently active Bus Controller. Host intervention is required for the BCRTM to take over as the active Bus Controller.
BIT 11	(RT) Terminal Flag. Setting this bit sets the RT status word Terminal Flag bit; the Terminal Flag bit in the RT status word is also internally set if the BIT fails.
BIT 10	(RT) Service Request. Setting this bit sets the RT status word Service Request bit.
BIT 9	(RT) Busy Mode Enable. Setting this bit sets the RT status word Busy bit and inhibits all data transfers to the subsystem.
BIT 8	BC/$\overline{RT}$ Mode Select. This bit's state reflects the external pin BCRTSEL. It does not necessarily reflect the state of the chip, since the BC/$\overline{RT}$ Mode Select is software-programmable via bit 10 of Register 0. This bit is read-only.
BIT 7	Change Lock-Out. This bit's state reflects the external pin LOCK. When set, this bit indicates that changes to the RT address or the BC/$\overline{RT}$ Mode Select are not allowed using internal registers. This bit is read-only.
BIT 6	Remote Terminal Address Parity Error. This bit indicates a Remote Terminal Address Parity Error. It appears after the Remote Terminal Address is latched if a parity error exists.
BIT 5	Remote Terminal Address Parity. This is an odd parity input bit used with the Remote Terminal Address. It ensures accurate recognition of the Remote Terminal Address.
BITs 4-0	Remote Terminal Address (Bit 0 is the LSB). This reflects the RTA4-0 inputs at Master Reset. Modify the Remote Terminal Address by writing to these bits.

#11 BIT Start Register (Write Only)

Any write (i.e., data = don't care) to this register's address location initiates the internal BIT routine, which lasts 100ms. Verify using the BIT-in-Progress bit in the Status Register. A programmed reset (write to Register 12) must precede a write to this register to initiate the internal BIT.A failure of the BIT will be indicated in Register 4 and the BCRTF pin.

The BCRTM's self-test performs an internal wrap-around test between its Manchester encoder and its two Manchester decoders. If the BCRTM detects a failure on either the primary or the secondary channel, it flags this failure by setting bit 14 of Register 4 (BIT Word Register) for Channel A and/or bit 15 for Channel B. When in the Remote Terminal mode, while the BCRTM is performing its self-test, it ignores any commands on the 1553 bus until it has completed the self-test.

#12 Programmed Reset Register (Write Only)

Any write (i.e., data = don't care) to this register's address location initiates a reset sequence of the encoder/decoder and protocol sections of the BCRTM which lasts less than 1 microsecond. This is identical to the reset used for the Reset Remote Terminal Mode Code except that command processing halts. For a total reset (i.e., including registers), see the $\overline{MRST}$ signal description.

#13 RT Timer Reset Register (Write Only)

Any write (i.e., data = don't care) to this register's address location resets the RT Time Tag timer to zero. The BCRTM 's Remote Terminal Timer time-tags message transactions. The time tag is generated from a free-running eight-bit timer of 64 microseconds resolution. This timer can be reset to zero simply by writing to Register 13. When the timer is reset, it immediately starts running.

#14 Activity Status/Operational Mode Register

BIT 15 Bus Monitor Select. This bit should be cleared for RT mode operation. The host sets this bit to enable the BCRTM's Monitor mode of operation. Bit 10 of Register 0 must also be "0" to enable the Monitor mode.

BIT 14 Monitor All Terminals. When this bit is set, the BCRTM monitors all remote terminal activity.If this bit is not set, then bit 13 must be set. This bit should be cleared for RT Mode operation.

BIT 13 Monitor Declared Terminals. When this bit is set, the BCRTM monitors all remote terminal bus activity. If this bit is not set, then bit 13 must be set.This bit should be cleared for RT mode operation.

BITs 12-0 Reserved

#15 Reserved Register

This register is reserved for BCRTM use only and the host should not access it.

#16 Monitor Selected Remote Terminal Address 15-0

BITs 15-0 Monitor Selected Remote Terminal Addresses 15-0. By setting the appropriate bit in this register, the host can determine which or the Remote terminals, from RT 0 through RT 15, the BCRTM will monitor. For example, by setting bit 5 in this register, the host instructs the BCRTM to only monitor the bus activity for remote terminal 5. These bits are not mutually exclusive, therefore, the host can monitor any number of different remote terminals by selecting the proper combination of bits.

#17 Monitor Selected Remote Terminal Address 31-16

BITs 15-0 Monitor Selected Remote Terminal Addresses 31-16. By setting the appropriate bit in this register, the host can determine which or the Remote terminals, from RT 16 through RT 31, the BCRTM will monitor. For example, by setting bit 21 in this register, the host instructs the BCRTM to only monitor the bus activity for remote terminal 21. These bits are not mutually exclusive, therefore, the host can monitor any number of different remote terminals by selecting the proper combination of bits on this register and Register 16.

Table 1. BCRTM Registers

#0 BC/RT CONTROL REGISTER

15	14	13	12	11	10	9	8
UNUSED	RT31	SA31	BCTO	EXTOVR	BC/RT	RTYALTB	BUSBEN
7	6	5	4	3	2	1	0
CHNSEL BUSAEN	RTYCNT		RTYBCME	RTYTO	RTYME	RTYBSY	STEN

#1 BC/RT STATUS REGISTER

15	14	13	12	11	10	9	8
TEST	RTACT	DYNBUS	RT FLAG	SRQ	BUSY	BIT	RESET
7	6	5	4	3	2	1	0
BC/RT	BUSA/B	SSFAIL	UNUSED	UNUSED	UNUSED	UNUSED	CMBKPG

#2 (BC) CURRENT COMMAND BLOCK REGISTER
(RT) REMOTE TERMINAL DESCRIPTOR SPACE ADDRESS REGISTER

15	14	13	12	11	10	9	8
A15	A14	A13	A12	A11	A10	A9	A8
7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

#3 POLLING COMPARE REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	MSGERR	INSTR	SRQ
7	6	5	4	3	2	1	0
SWBT12	SWBT13	SWBT14	BRDCST	BUSY	SS FLAG	DBC	TF

#4 BIT WORD REGISTER

15	14	13	12	11	10	9	8
CHBFAIL	CHAFAIL	D13	D12	D11	D10	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

#5 CURRENT COMMAND REGISTER

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

#6 INTERRUPT LOG LIST POINTER REGISTER

15	14	13	12	11	10	9	8
A15	A14	A13	A12	A11	A10	A9	A8
7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

#7 BCRTM HIGH-PRIORITYINTERRUPT ENABLE REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DATOVR
7	6	5	4	3	2	1	0
ILLCMD	DYNBUS	SSFAIL	ENDBIT	BITFAIL	EOL	MSGERR	STDINT

#8 BCRTM HIGH-PRIORITYINTERRUPT STATUS/RESET REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DATOVR
7	6	5	4	3	2	1	0
ILLCMD	DYNBUS	SSFAIL	ENDBIT	BITFAIL	EOL	MSGERR	STDINT

#9 STANDARD INTERRUPT ENABLE REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
7	6	5	4	3	2	1	0
UNUSED	UNUSED	ILLBCMD	ILLCMD	POLMTCH	RTYFAIL	MSGERR	CMDBLK

#10 REMOTE TERMINAL ADDRESS REGISTER

15	14	13	12	11	10	9	8
INSTR	BUSY2	SS FLAG	DBC	RT FLAG	SRQ	BUSY1	BC/RT
7	6	5	4	3	2	1	0
LOCK	PARERR	RTAPAR	RTA4	RTA3	RTA2	RTA1	RTA0

Table 1. BCRTM Registers (continued from page 19)

#11 BUILT-IN-TEST START REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#12 PROGRAMMED RESET REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#13 REMOTE TERMINAL TIMER RESET REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#14 BUS MONITOR CONTROL REGISTER

15	14	13	12	11	10	9	8
BMS	MAT	MDT	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#16 MONITOR SELECTED REMOTE TERMINAL ADDRESES 0-15

15	14	13	12	11	10	9	8
TA15	TA14	TA13	TA12	TA11	TA10	TA9	TA8
7	6	5	4	3	2	1	0
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0

#17 MONITOR SELECTED REMOTE TERMINAL ADDRESES 16-31

15	14	13	12	11	10	9	8
TA31	TA30	TA29	TA28	TA27	TA26	TA25	TA24
7	6	5	4	3	2	1	0
T23	T22	T21	T20	T19	TA18	TA17	TA16

X = DON'T CARE

4.0 SYSTEM OVERVIEW

The BCRTM can be configured for a variety of processor and memory environments. The host processor and the BCRTM communicate via a flexible, programmable interrupt structure, internal registers, and a user-definable shared memory area. The shared memory area (up to 64K) is completely user-programmable and communicates BCRTM control information -- message data, and status/ error information.

Built-in memory management functions designed specifically for MIL-STD-1553 applications aid processor off-loading. The host needs only to establish the parameters within memory so the BCRTM can access this information as required. For example, in the RT mode, the BCRTM can store data associated with individual subaddresses anywhere within its 64K address space. The BCRTM then can automatically buffer up to 128 incoming messages of the same subaddress, thus preventing the previous messages from being overwritten by subsequent messages. This buffering also extends the intervals required by the host processor to service the data. Selecting an appropriate MCLK frequency to meet system memory access time requirements controls the memory access rate. The completion of a user-defined task or the occurrence of a user-selected event is indicated by using the extensive set of interrupts provided.

In the BC mode, the BCRTM can process multiple messages, assist in scheduling message lists, and provide host-programmable functions such as auto retry. The BCRTM is incorporated in systems with a variety of interrupt latencies by using the Interrupt History List feature (see Exception Handling and Interrupt Logging, page 38). The Interrupt History List sequentially stores the events that caused the interrupt in memory without losing information if a host processor does not respond immediately to an interrupt.

In the Monitor (M) mode, the BCRTM's powerful linked list command block structure allows it to process a series of monitored 1553 messages without the intervention of the host. The BCRTM can store as much bus traffic as can be contained in its 64K memory space. In addition, the host has the capability of instructing the BCRTM to monitor and store data for only selected remote terminals. The host system is responsible for initializing an area in memory that tells the BCRTM where to store command word information and data for each command that the BCRTM receives on the 1553 bus. This area of memory consists of "Bus Monitor Command Blocks". An M Command Block is very similar to the BC Command Block in the BCRTM. The only real differences are the direction of information flow, and that there is no Head Pointer in the M Command Block.

5.0 SYSTEM INTERFACE

5.1 DMA Transfers

The BCRTM initiates DMA transfers whenever it executes command blocks (BC mode) or services commands (RT mode). DMAR initiates the transfer and is terminated by the inactive edge of DMACK. The Address Enable (AEN) input enables the BCRTM to output an address onto the Address bus.

The BCRTM requests transfer cycles by asserting the DMAR output, and initiates them when a DMAG input is received. A DMACK output indicates that the BCRTM has control of the Data and Address buses. The TSCTL output is asserted when the BCRTM is actually asserting the Address and Data buses.

To support using multiple bus masters in a system, the BCRTM outputs the DMAGO signal that results from the DMAG signal passing through the chip when a BCRTM bus request was not generated (DMAR inactive). You can use DMAGO in daisy-chained multimaster systems.

5.2 Hardware Interface

The BCRTM provides a simple subsystem interface and facilitates DMA arbitration. The user can configure the BCRTM to operate in a variety of memory-processor environments including pseudo-dual-port RAM and standard DMA configurations.

For complete circuit description, such as arbitration logic and I/O, please refer to the appropriate application note.

5.3 CPU Interconnection

Pseudo-Dual-Port RAM Configuration

The BCRTM's Address and Data buses connect directly to RAM, with buffers isolating the BCRTM's buses from those of the host CPU (figures 3a and 3b). The CPU's memory control signals (RD, WR, and MEMCSI) pass through the BCRTM and connect to memory as RRD, RWR, and MEMCSO.

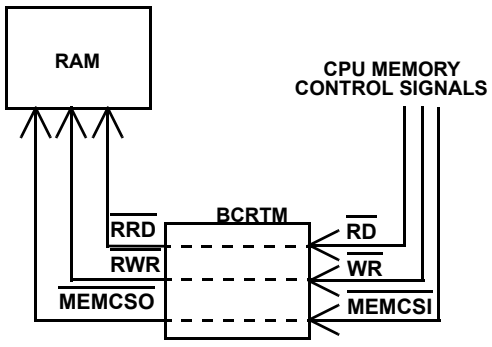


Figure 3a. Pseudo Dual-Port RAM Control Signals

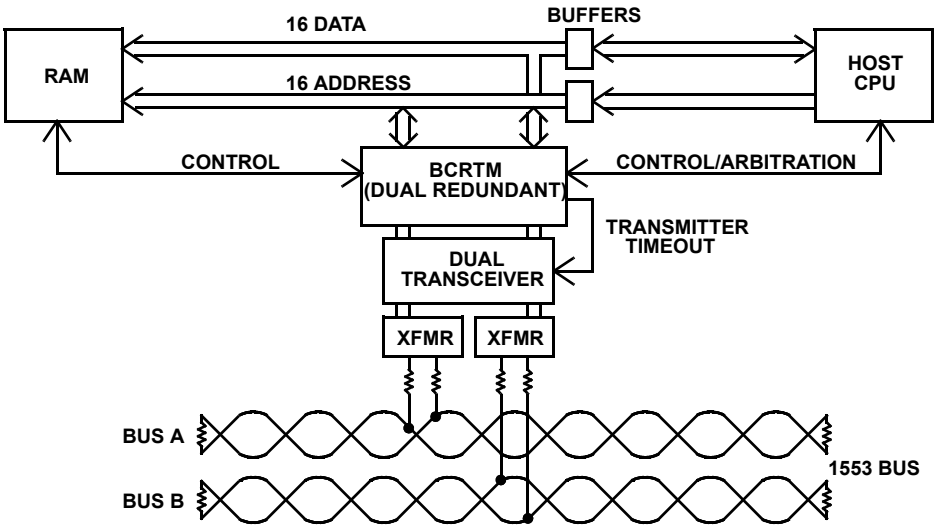


Figure 3b. CPU/BCRTM Interface -- Pseudo-Dual-Port RAM Configuration

Standard DMA Configuration

The BCRTM's and CPU's data, address, and control signals are connected to each other as shown in figures 3c and 3d. The RWR, RRD, and MEMCSO are activated after DMAG is asserted.

In either case, the BCRTM's Address and Data buses remain in a high-impedance state unless the CS and RD signals are active, indicating a host register access; or TSCTL is asserted, indicating a memory access by the BCRTM. CPU attempts to access BCRTM registers are ignored during BCRTM memory access. Inhibit DMA transfers by using the Busy function in the Remote Terminal Address Register while operating in the Remote Terminal mode.

The designer can use TSCTL to indicate when the BCRTM is accessing memory or when the CPU can access memory. AEN is also available (use is optional), giving the CPU control over the BCRTM's Address bus. A DMA Burst (BURST) signal indicates multiple DMA accesses.

Register Access

Registers 0 through 13 are accessed with the decode of the four LSBs of the Address bus (A0-A3) and asserting CS. Pulse either RD or WR for multiple register accesses.

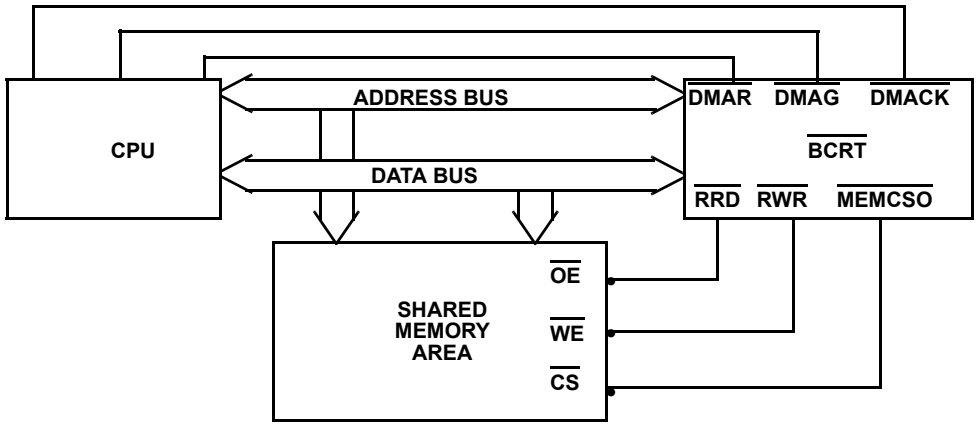


Figure 3c. DMA Signals

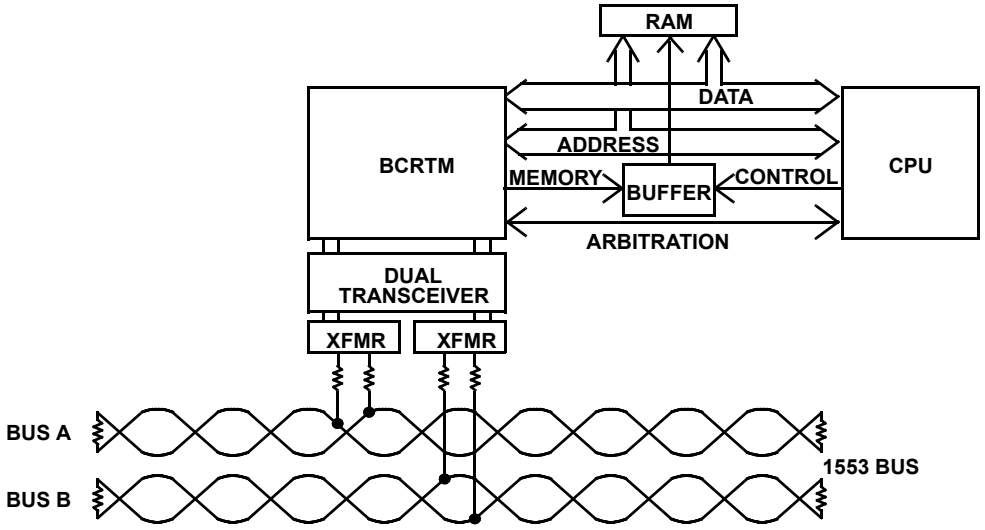


Figure 3d. CPU/BCRTM Interface -- DMA Configuration

5.4 RAM Interface

The BCRTM's RRD, RWR, and MEMCSO signals serve as read and write controls during BCRTM memory accesses. The host subsystem signals RD, WR, and MEMCSI propagate through the BCRTM to become RRD, RWR, and MEMCSO outputs to support a pseudo-dual-port. During BCRTM-RAM data transfers, the host subsystem's memory signals are ignored until the BCRTM access is complete.

5.5 Transmitter/Receiver Interface

The BCRTM's Manchester II encoder/decoder interfaces directly with the1553 bus transceiver, using the TAO-TAZ and RAZ-RAO signals for Channel A, and TBO-TBZ and RBZ-RBO signals for Channel B.

The BCRTM also provides a TIMERON signal output and an active channel output indicator (CHA/B) to assist in meeting the MIL-STD-1553B fail-safe timer requirements.

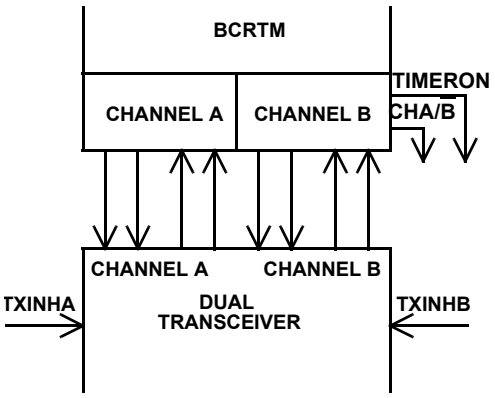


Figure 4. Dual-Channel Transceiver

6.0 REMOTE TERMINAL ARCHITECTURE

The Remote Terminal architecture is a descriptor-based configuration of relevant parameters. It is composed of an RT Descriptor Space (see figure 5) and internal, host-programmable registers. The Descriptor Space contains only descriptors. Descriptors contain programmable subaddress parameters relating to handling message transfers. Each descriptor consists of four words: (1) a Control Word, (2) a Message Status List Pointer, (3) a Data List Pointer, and (4) an unused fourth word (see figure 6.) These words indicate how to perform the data transfers associated with the designated subaddress.

A receive descriptor and a transmit descriptor are associated with each subaddress. The descriptors reside in memory and are listed sequentially by subaddress. By using the index within the descriptor, the BCRTM can buffer incoming and outgoing messages, which reduces host CPU overhead. This message buffering also reduces the risk of incoming messages being overwritten by subsequent incoming messages.

Each descriptor contains a programmable interrupt structure for subsystem notification of user-selected message transfers and indicates when the message buffers are full. Illegalizing subaddresses, in normal and broadcast modes, is accomplished by using programmable bits within the descriptor (see the RT Functional Operation section on page 24).

Message Status information -- including word count, an internally generated time tag, and broadcast and message validity information -- is provided for each message. The Message Status Words are stored in a separate Message Status Word list according to subaddress. The list's starting locations are programmable within the descriptor.

Message data, received or transmitted, is also stored in lists. The message capacity of the lists and the lists' locations are user selectable within the descriptor.

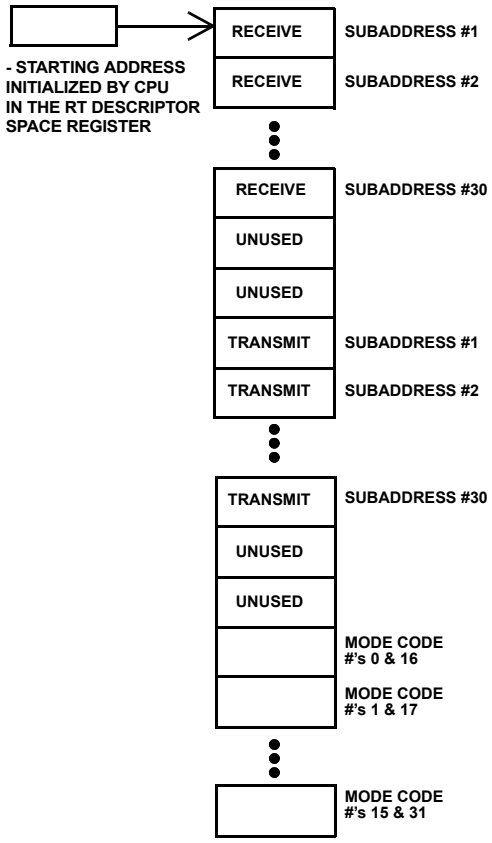


Figure 5. Descriptor Space

6.1 RT Functional Operation

The RT off-loads the host computer of all routine data transfers involved with message transfers over the 1553B bus by providing a wide range of user-programmable functions. These functions make the BCRTM's operation flexible for a variety of applications. The following paragraphs give each function's operational descriptions.

6.1.1 RT Subaddress Descriptor Definition

The host sets words within the descriptor (see figure 6). The BCRTM then reads the descriptor words when servicing a command corresponding to the specified descriptor. All bit-selectable functions are active high and inhibited when low.

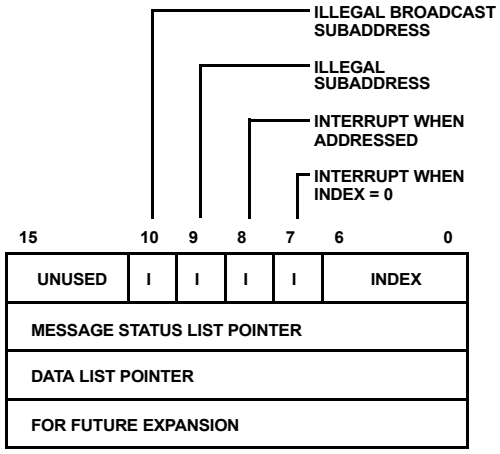


Figure 6. Remote Terminal Subaddress Descriptor

A.Control Word. The first word in the descriptor, Control Word, selects or disables message transfers andthe selects an index.

Bit Number	Description
BITs 15-11	Reserved.
BIT 10	Illegal Broadcast Subaddress. Indicates to the BCRTM not to access this subaddress using broadcast commands. The Message Error bit in the status word is set if the illegal broadcast subaddress is addressed. Since transmit commands do not apply to broadcast, this bit applies only to receive commands.
BIT 9	Illegal Subaddress. Set by the host CPU, it indicates to the BCRTM that a command with this subaddress is illegal. If a command uses an illegal subaddress the Message Error bit in the 1553 status word is set. The Illegal Command Interrupt is also asserted if enabled.
BIT 8	Interrupt Upon Valid Command Received. Indicates that the BCRTM is to assert an interrupt every time a command addresses this descriptor. The interrupt occurs just prior to post-command descriptor updating.
BIT 7	Interrupt When Index = 0. Indicates that the BCRTM initiates an interrupt when the index is decremented to zero.
BITs 6-0	Index. These bits are for indexed message buffering. Indexing means transacting a pre-specified number of messages before notifying the host CPU. After each message transaction, the BCRTM decrements the index by one until index = 0. Note that the index is decremented for messages that contain message errors.

B. Message Status List Pointer. The host sets the Message Status List Pointer, the second word within the descriptor, and the BCRTM uses it as a starting address for the Message Status List. It is incremented by one with each Message status word write. If the Control Word Index is already equal to zero, the Message Status List Pointer is not incremented and the previous Message status word is overwritten.

Note: A Message Status Word is also written and the pointer is incremented when the BCRTM detects a message error.

C. Data List Pointer. The Data List Pointer is the third word within the descriptor. The BCRTM stores data in RAM beginning at the address indicated by the Data List Pointer. The Data List Pointer is updated at the end of each successful message with the next message's starting address with the following exceptions:

- If the message is erroneous, the Data List Pointer is not updated. The next message overwrites any data corresponding to the erroneous message.
- Upon receiving a message, if the index is already equal to zero, the Data List Pointer is not incremented and data from the previous message is overwritten.

D. Reserved. The fourth descriptor word is reserved for future use.

6.1.2 Message Status Word

Each message the BCRTM transacts has a corresponding Message Status Word, which is pointed to by the Message Status List Pointer of the Descriptor. This word allows the host CPU to evaluate the message's validity, determine the word count, and calculate the approximate time frame in which the message was transacted (figures 7 and 8).

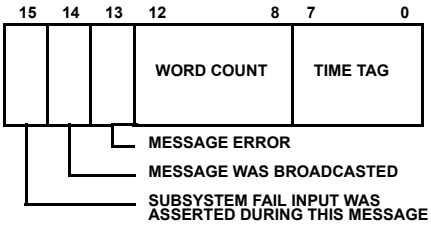


Figure 7. Message Status Word

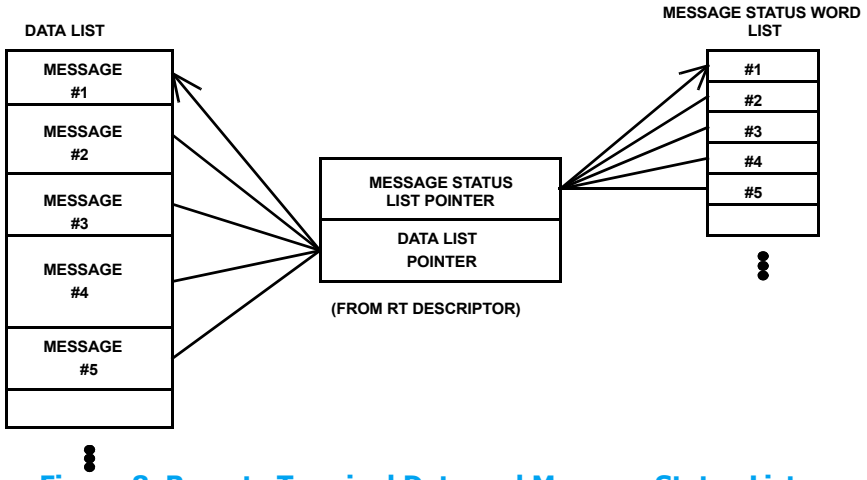


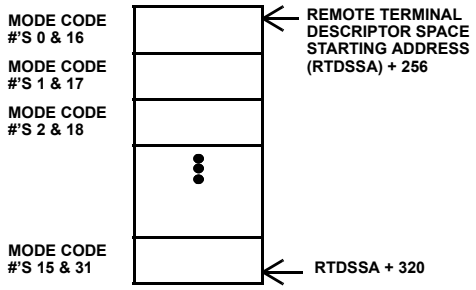
Figure 8. Remote Terminal Data and Message Status List

Message Status Word Definition

Bit Number	Description
BIT 15	Subsystem Failed. Indicates SSYSF was asserted before the Message Status Word transfer to memory. This bit is also set when the user sets bit 13 of Register 10.
BIT 14	Broadcast Message. Indicates that the corresponding message was received in the broadcast mode.
BIT 13	Message Error. Indicates a message is invalid due to improper synchronization, bit count, word count, Manchester error.
BITs 12-8	Word Count. Indicates the number of words in the message and reflects the Word Count field in the command word. Should the message contain a different number of words than the Word Count field, the Message Error flag is triggered. If there are too many words, they are withheld from RAM. If the actual word count is less than or greater than it should be, the Message Error bit in the 1553 status word is set.
BITs 7-0	Time Tag. The BCRTM writes the internally generated Time Tag to this location after message completion. The resolution is 64 microseconds. (See Register 13). If the timer reads 2, it indicates the message was completed 128 to 191μs after the timer started.

6.1.3 Mode Code Descriptor Definition

Mode codes are handled similarly to subaddress transactions. Both use the four-word descriptors residing in the RT descriptor space to allow the host to program their operational mode. Corresponding to each mode code is a descriptor (see figure 9a). Of the 32 address combinations for mode codes in MIL-STD-1553B, some are clearly defined functions while others are reserved for future use. Sixteen descriptors are used for mode code operations with each descriptor handling two mode codes: one mode code with an associated data word and one mode code without an associated data word. All mode codes are handled in accordance with MIL-STD-1553B. The function of the first word of the Mode Code Descriptor is similar to that of the Subaddress Descriptor and is defined below. The remaining three words serve the same purpose as in the Subaddress Descriptor.



Note:
Mode code descriptor blocks are also provided for reserved mode codes but have no associated predefined BCRTM operation.

Figure 9a. (RT) Mode Code Descriptor Space

Control Word

Bit Number	Description
BIT 15	Interrupt on Reception of Mode Code (without Data Word).
BIT 14	Illegalize Broadcast Mode Code (without Data Word).
BIT 13	Illegalize Mode Code (without Data Word).
BIT 12	Reserved.
BIT 11	Illegalize Broadcast Mode Code (with Data Word).
BIT 10	Illegalize Transmit Mode Code (with Data Word).
BIT 9	Illegalize Receive Mode Code (with Data Word).
BIT 8	Interrupt on Reception of Mode Code (with Data Word).
BIT 7	Interrupt if Index = 0.
BITs 6-0	Index. Functionally equivalent to the index described in the Subaddress Descriptor. It applies to mode codes with data words only.

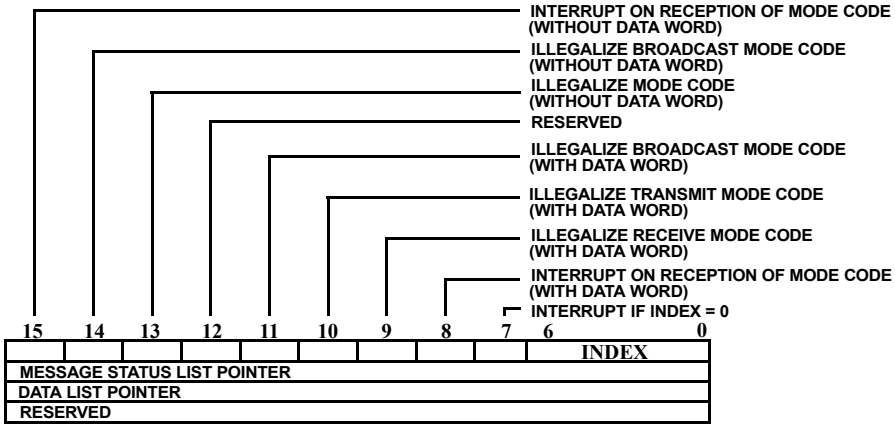


Figure 9b. (RT) Mode Code Descriptor

The descriptors, numbered sequentially from 0 to 15, correspond to mode codes 0 to 15 without data words and mode codes 16 to 31 with data words. For example, mode codes 0 and 16 correspond to descriptor 0 and mode codes 1 and 17 correspond to descriptor 1. The Mode Code Descriptor Space is appended to the Subaddress Descriptor Space starting at 0100H (256D) of the 320-word RT Descriptor Space (see figure 5).

The BCRTM autonomously supports all mode codes without data words by executing the specific function and transmitting the 1553 status word. The subsystem provides the data word for mode codes with data words (see the Data List Pointer section). For all mode codes, an interrupt can be asserted upon successful completion of the mode command by setting the appropriate bit in the control word (see figure 9b).

Dynamic Bus Control #00000
This mode code is accepted automatically if the Dynamic Bus Control Enable bit in the Remote Terminal Address Register is set. Setting the Dynamic
Bus Control Acceptance bit in the 1553 status word and BCRTM Status Register confirms the mode code acceptance. A High-Priority Interrupt is also asserted if enabled. If the Dynamic Bus Control Enable bit is not set, the BCRTM does not accept Dynamic Bus Control.

Synchronize (Without Data Word) #00001
If enabled in the Mode Code #00001 Descriptor Control Word, the BCRTM asserts an interrupt when this mode code is received.

Transmit Status Word #00010
The BCRTM automatically transmits the 1553 status word corresponding to the last message transacted.

Initiate Self-Test #00011
The BCRTM automatically starts its BIT routine. An interrupt, if enabled, is asserted when the test is completed. The BIT Word Register and external pin BCRTF are updated when the test is completed. A failure in BIT will also set the TF status word bit.

Transmitter Shutdown #00100
The BCRTM disables the channel opposite the channel on which the command was received.

Override Transmitter Shutdown #00101
The BCRTM enables the channel previously disabled.

Inhibit Terminal Flag Bit #00110
The BCRTM inhibits the Terminal Flag from being set in the status word.

Override Inhibit Terminal Flag Bit #00111
The BCRTM disables the Terminal Flag inhibit.

Reset Remote Terminal #01000
The BCRTM automatically resets the encoder, decoders, and protocol logic.

Transmit Vector Word #10000
The BCRTM transmits the vector word from the location addressed by the Data List Pointer in the Mode Code Descriptor Block.

Synchronize (with Data Word) #10001
On receiving this mode code, the BCRTM simply stores the associated data word.

Transmit Last Command #10010
The BCRTM transmits the last command executed and the corresponding 1553 status word.

Transmit BIT Word #10011
The BCRTM transmits BIT information from the BIT Register.

Selected Transmitter Shutdown #10100
On receiving this mode code, the BCRTM simply stores the associated data word.

Override Selected Transmitter Shutdown #10101
On receiving this mode code, the BCRTM simply stores the associated data word.

Mode codes 9-15 and 22-31 are reserved for future expansion of MIL-STD-1553B.

6.2 RT Error Detection

In accordance with MIL-STD-1553B, the remote terminal handles superseding commands on the same or opposite bus. When receiving, the remote terminal performs a response time-out function of 56 microseconds for RT-RT transfers. If the response time-out condition occurs, a Message Error bit is set in the 1553 status word and in the Message Status Word. Error checking occurs on both of the Manchester logic and the word formats. Detectable errors include word count errors, long words, short words, Manchester errors (including zero crossing deviation), parity errors, and data discontiguity.

6.3 RT Operational Sequence

The following is a general description of the typical behavior of the BCRTM as it processes a message in the RT mode. It is assumed that the user has already written a "1" to Register 0, bit 0, enabling RT operation.

Valid Command Received.

$\overline{\text{COMSTR}}$ goes active

- DMA Descriptor Read. After receiving a valid command, the BCRTM initiates a burst DMA:

  DMA arbitration (BURST)
  Control Word read
  Message Status List Pointer read
  Data List Pointer read

Data Transmitted/Received.

- Data Word DMA.

  If the BCRTM needs to transmit data from memory, it initiates a DMA cycle for each Data Word shortly before the Data Word is needed on the 1553B bus:

  DMA arbitration
  Data Word read (starting at Data List Pointer address, incremented for each successive word)

  If the BCRTM receives data, it writes each Data Word to memory after the Data Word is received:

  DMA arbitration
  Data Word write (starting at Data List Pointer address, incremented for each successive word)

Status Word Transmission.

The BCRTM automatically transmits the Status Word as defined in MIL-STD-1553B. The Message Error and Broadcast Command Received bits are generated internally. Writing to Register 10 enables the other predefined bits. For illegalized commands, the BCRTM sets the Message Error Bit in the 1553 Status Word.

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRTM is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

DMA arbitration (BURST)
Interrupt Status Word write
RT Descriptor Block Pointer write
Tail Pointer read (into Register 6)
$\overline{\text{STDINTP}}$ pulses low
STDINTL asserted (if enabled)
Processing continues

- Descriptor Write.

After the BCRTM processes the message, a final DMA burst occurs to update the descriptor block, if necessary:

DMA arbitration (BURST)
Message Status Word write
Data List Pointer write(incremented by word count)
Message Status List Pointer write (incremented by 1)
Control Word write(index decremented)

Note the following exceptions:

Mode codes without data require no descriptor update.

Predefined mode codes (18 and 19) which do not require access to memory for the data word, do not involve updating the Data List Pointer.

Messages with errors prevent updates to the Data List Pointer.

If the message index was zero, neither the Message Status List Pointer nor the Data
List Pointer is updated.

7.0 BUS CONTROLLER ARCHITECTURE

The BCRTM 's bus controller architecture is based on a Command Block structure and internal, host-programmable registers. Each message transacted over the MIL-STD-1553B bus has an associated Command Block, which the CPU sets up (see figures 10 and 11). The Command Block contains all the relevant message and RT status information as well as programmable function bits that allow the user to select functions and interrupts. This memory interface system is flexible due to a doubly-linked list data structure.

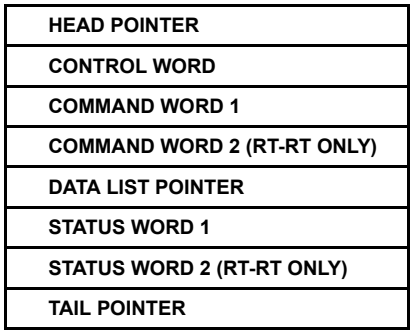


Figure 10. Command Block

In a doubly-linked Command Block structure, pointers delimit each Command Block to the previous and successive blocks (see figure 12). The linking feature eases multiple message processing tasks and supports message scheduling because of its ability to loop through a series of transfers at a predetermined cycle time. A data pointer in the command allows efficient space allocation because data blocks only have to be configured to the exact word count used in the message. Data pointers also provide flexibility in data-bank switching.

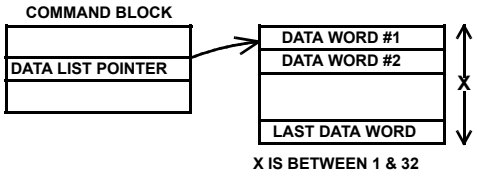


Figure 11. Data Placement

A control word with bit-programmable functions and a Message Error bit are in each Command Block. This allows selecting individual functions for each message and provides message validity information. The BCRTM 's register set provides additional global parameters and address pointers.

A programmable auto retry function is selectable from the control word and Control Register.

The auto retry can be activated when any of the following occurs:

- Busy bit set in the status word
- Message Error (indicated by the RT status response)
- Response Time-Out
- Message Error detected by the Bus Controller

One to four retries are programmable on the same or opposite bus.

The Bus Controller also has a programmable intermessage delay timer that facilitates message transfer scheduling (see figures 13 and 14). This timer, programmed in the control word, automatically delays between the start of two successive commands.

A polling function is also provided. The Bus Controller, when programmed, compares incoming status words to a host-specified status word and generates an interrupt if the comparison indicates any matching bits. An Interrupt and Continue function facilitates the host subsystem's synchronization by generating an interrupt when the specified Command Block's message is executed.

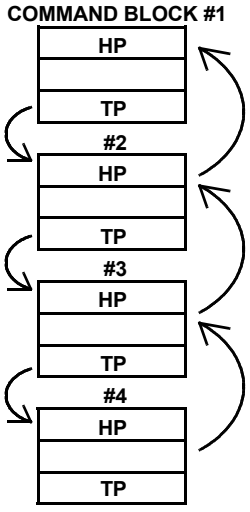


Figure 12. Command Block Chaining

7.1 BC Functional Operation

The Bus Controller off-loads the host computer of many functions needed to coordinate 1553B bus data transfers. Special architectural features provide message-by-message flexibility. In addition, a programmable interrupt scheme, programmable intermessage timing delays, and internal registers enhance the BCRTM 's operation.

The host determines the first Command Block by setting the initial starting address in the current Command Block Register. Once set, the BCRTM updates the current Command Block register with the next Command Block Address. The BCRTM then executes the sequential

Command Blocks and counts out message delays (where programmed) until it encounters the last Command Block listed (indicated by the End of List bit in the control word). Interrupts are asserted when enabled events occur (see the Exception Handling and Interrupt Logging section, page 38).

The functions and their programming instructions are described below. The registers also contain many programmable functions and function parameters.

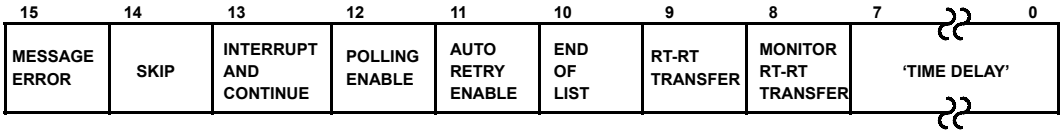


Figure 13. Control Word

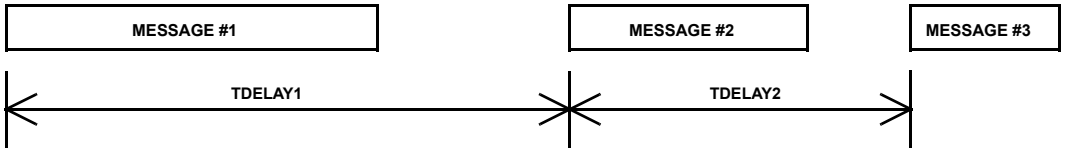


Figure 14. BC Timing Delays

BC Command Block Definition
Each Command Block contains (see figure 10):

A. **Head Pointer.** Host-written, this location can contain the address of the previous Command Block's Head Pointer. The BCRTM does not access this location.

B. **Control Word.** Host-written, the Control Word contains bit-selectable options and a Message Error bit the BCRTM provides (see figure 13). The bit definitions follow.

Bit Number **Description**

BIT 15 Message Error. The BCRTM sets this bit when it detects an invalid RT response as defined in MIL-STD-1553B.

BIT 14 Skip. When set, this bit instructs the BCRTM to skip this Command Block and execute the next.

BIT 13 Interrupt and Continue. If set, a Standard Interrupt is asserted when this block is addressed; operation, however, continues. Note that this interrupt must also be enabled by setting bit 0 of Register 9.

BIT 12 Polling Enable. Enables the BCRTM 's polling operation.

BIT 11 Auto Retry Enable. When set, the Auto Retry function, governed by the global parameters in the Control Register, is enabled for this message.

BIT 10 End of List. Set by the CPU, this bit indicates that the BCRTM , upon completion of the current message, will halt and assert a High-Priority Interrupt. The interrupt must also be enabled in the High-Priority Interrupt Enable Register.

BIT 9 RT-RT. Set by the CPU, this indicates that this Command Block transacts an RT-RT transfer.

BIT 8 Monitor RT-RT Transfer. Set by the CPU, this function indicates that the BCRTM should receive and store the message beginning at the location indicated by the data pointer.

BITs 7-0 Time Delay. The CPU sets this field, which causes the BCRTM to delay the specified time between sequential message starts (see figures 13 and 14). Regardless of the value in the Time Delay field (including zero), the BCRTM will at least meet the minimum 4ms intermessage gap time as specified in MIL-STD-1553B.
The timer is enabled by having a non-zero value in this bit field. When using this function, please note:

- Timer resolution is16 microseconds. As an example, if a given message requires 116μs tocomplete (including the minimum 4μs intermessage gap time) the value in the Time Delay field must be at least 00001000 (8 x 16μs = 128μs) to provide an intermessage gap greater than the4μs minimum requirement.
- If the timer is enabled and the Skip bit is set, the timer provides the programmed delay before proceeding.
- If the message duration exceeds the timer delay, the message is completed just as if the timer were not enabled.
- If SKIP = 1 and EOL = 1, the HPINT is generated if enabled.
- If SKIP = 1 and Interrupt and Continue = 1, the STDINT is generated if enabled.

C. **Command Word One.** Initialized by the CPU, this location contains the first command word corresponding to the Command Block's message transfer.

D. **Command Word Two.** Initialized by the CPU, this location is for the second (transmit) command word in RT-RT transfers. In messages involving only one RT, the location is unused.

E. **Data Pointer.** Initialized by the CPU, this location contains the starting location in RAM for the Command Block's message (see figure 15).

F. **Status Word One.** Stored by the BCRTM , this location contains the entire Remote Terminal status response.

G. **Status Word Two.** Stored by the BCRTM , this location contains the receiving Remote Terminal status word. For transfers involving one Remote Terminal, the location is unused.

H. **Tail Pointer.** Initialized by the host CPU, the Tail Pointer contains the next Command Block's starting address.

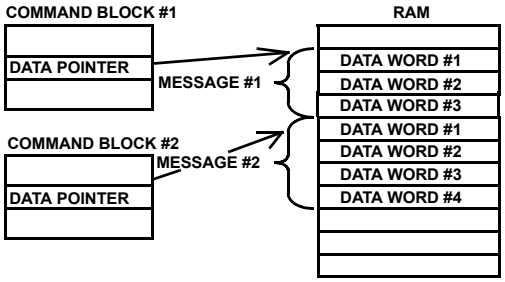


Figure 15. Continuous Data Storage

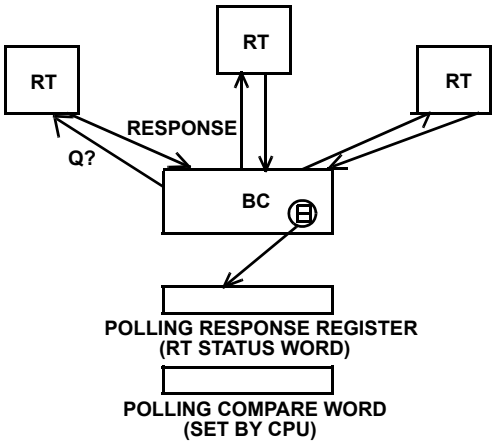


Figure 16. Polling Operation

7.2 Polling

During a typical polling scenario (see figure 16) the Bus Controller interrogates remote terminals by requesting them to transmit their status words. This feature can also alert the host if a bit is set in any RT status word response during normal message transactions. The BCRTM enables the host to initialize a chain of Command Blocks with the command word's Polling Enable bit. A programmable Polling Compare Register (PCR) is provided. In the polling mode, the Remote Terminal response is compared to the Polling Compare Register contents. Program the PCR by setting the PCR bits corresponding to the RT's 1553 status word bits to be compared. If they match (i.e., two 1's in the same bit position) then, if enabled in both the BC Command Block Control Word and in the Standard Interrupt Enable Register (Register 9), a polling comparison interrupt is generated.

Example 1. No bit match is present

PCR	00000000001
RT's 1553 Status Word response	00000100010
Result	No Polling Comparison Interrupt

Example 2. Bit match is present

PCR	00100100000
RT's 1553 Status Word response	00000100000
Result	Polling Comparison Interrupt

7.3 BC Error Detection

The Bus Controller checks for errors (see the Exception Handling and Interrupt Logging and the RT Error Detection sections, pages 38 and 27) on each message transaction. In addition, the BC compares the RT command word addresses to the incoming status word addresses. The BC monitors for response time-out and checks data and control words for proper format according to MIL-STD-1553B. Illogical commands include incorrectly formatted RT-RT Command Blocks.

7.4 Bus Controller Operational Sequence

The following is a general description of the typical behavior of the BCRTM as it processes a message in the BC mode.

The user starts BC operation by writing a "1" to Register 0, Bit 0.

- Command Block DMA - the following occurs immediately after Bus Controller startup:

  DMA arbitration (BURST)
  Control Word read
  Command Word 1 read (from third location of Command Block)
  Data List Pointer read

A. For BC-to-RT Command Blocks:

The BCRTM transmits the Command Word.

- Data Word DMA

  DMA arbitration
  Data Word read (starting at Data List Pointer address, incremented for each successive word)

The BCRTM transmits the Data Word. Data Word DMAs and transmissions continue until all Data Words are transmitted.

- Status Word DMA

The BCRTM receives the RT Status Word.

  DMA arbitration
  Status Word write (to sixth location of Command Block)

B. For RT-to-BC Command Blocks:

The BCRTM transmits the Command Word.

- Status Word DMA

The BCRTM receives the RT Status Word.

  DMA arbitration
  Status Word write (to sixth location of Command Block)

The BCRTM receives the first Data Word.

- Data Word DMA

  DMA arbitration
  Data Word write (starting at Data List Pointer address, incremented for each successive word)

Data Word receptions and DMAs continue until all Data Words are received.

C. For RT(B)-to-RT(A) Command Blocks:

The BCRTM transmits Command Word 1 to RT(B).

- Command Word 2 DMA

  DMA arbitration
  Command Word 2 read (from fourth location of Command Block)

The BCRTM transmits Command Word 2 to RT(A).

The BCRTM receives the RT Status Word from RT(A).

- Status Word DMA for RT(A) Status Word

  DMA arbitration
  Status Word write (to sixth location of Command Block)

The BCRTM receives the first Data Word

- Data Word DMA (only if the BCRTM is enabled to monitor the RT-to-RT message).

  DMA arbitration
  Data Word write (starting at Data List Pointer address, incremented for each successive word)

Data Word receptions and DMAs continue until all Data Words are received.

The BCRTM receives the RT Status Word from RT(B).

- Status Word DMA for RT(B) Status Word

  DMA arbitration
  Status Word write (to seventh location of Command Block)

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRTM is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

  DMA arbitration (BURST)
  Interrupt Status Word write
  Command Block Pointer write
  Tail Pointer read (into Register 6)
  $\overline{\text{STDINTP}}$ pulses low
  $\overline{\text{STDINTL}}$ asserted (if enabled)
  Processing continues

If Retries are enabled and a Retry condition occurs, the following DMA occurs:

  DMA arbitration (BURST)
  Control Word read
  Command Word 1 read (from third location of Command Block)
  Data List Pointer read

The BCRTM proceeds from the current Command Block to the next successive Command Block.

- If no Message Error has occurred during the current Command Block, the following occurs:

  DMA arbitration (BURST)
  Command Block Tail Pointer read (to determine location of next Command Block. Note that this occurs only if no Retry.)
  DMA hold cycle
  Control Word read (next Command Block)
  Command Word 1 read (next Command Block)
  Data List Pointer read

- If the BCRTM detects a Message Error while processing the current Command Block, the following occurs:

  DMA arbitration (BURST)
  Control Word write
  Command Block Tail Pointer read (to determine location of next Command Block. Note that this occurs only if no Retry.)
  DMA hold cycle
  Control Word read (next Command Block)
  Command Word 1 read (next Command Block)
  Data List Pointer read

The BCRTM proceeds again from point A, B, or C as shown above.

7.5 BC Operational Example
(see figure 18 on page 35)

The BCRTM is programmed initially to accomplish the following:

The first Command Block is for a four-word RT-RT transfer with the BCRTM monitoring the transfer and storing the data.

- Auto-retry is enabled on the opposite bus using only one retry attempt, if the incoming Status Word is received with the Message Error bit set.
- Wait for a time delay of 400ms before proceeding to the next Command Block.
- The Data List Pointer contains the address 0400H.

The second Command Block is for a BC-RT transfer of two words.

- The End of List bit is set in its Control Word.
- The Data List Pointer contains the address 0404H.
- The Polling Enable bit is set and the Polling Compare Register contains a one in the Subsystem Fail position (bit 2).

Then:

A. The CPU initializes all the appropriate registers and Command Blocks, and issues a Start Enable by writing a "1" to Register 0, bit 0.

B. The BCRTM , through executing a DMA cycle, reads the control word, command words, and the Data List Pointer. The delay timer starts and message execution begins by transmitting the receive and transmit commands stored in the Command Blocks. The BCRTM then waits to receive the status word back from the transmitting RT.

C. The BCRTM receives the RT status word with all status bits low from the transmitting RT and stores the status word in Command Block 1. The incoming data words from the transmitting RT follow. The BCRTM stores them in memory locations 0400H - 0403H.

   If the status word indicates that the message cannot be transmitted (Message Error), the response time-out clock counts to zero and the allotted message time runs out. An auto-retry can be initiated if programmed to do so. Nevertheless, the ME bit in the control word is set.

D. The BCRTM receives the status word response from the receiving RT. The ME bit in the status word is set, indicating the message is invalid. The BCRTM initiates the auto retry function, (as programmed) on the alternate bus, re-transmits the command words, receives the correct status word, and stores the data again in locations 0400H - 0403H. This time the status word response from the receiving RT indicates the message transfer is successful.

E. The timer delay between the two successive transactions counts down another 135 microseconds before proceeding. This is determined as follows:

   The message transaction time is approximately 130 microseconds (the only approximation is due to the range in status response and intermessage gap times specified by MIL-STD-1553B). Approximating that with the retry, the total duration for the two attempts
   is 265ms.

F. The BCRTM reads the Tail Pointer of Command Block 1 and places it in the Current Command Register. It also reads the control word, command word, and Data List Pointer, and the first data word in the second Command Block.

G. Since this is a BC-RT transfer, the BCRTM transmits the receive command followed by two data words from locations 0404H - 0405H in memory. The BCRTM reads the second data word from memory while transmitting the first.

H. The BCRTM receives the status response from the RT. In this case, the status word indicates, by the ME bit being low, that the message is valid. The status word also has the Subsystem Fail bit set.

I. The status word is stored in the Command Block. The BCRTM , having encountered the end of the list, halts message transactions and waits for another start signal.

J. The BCRTM asserts a High-Priority Interrupt indicating the end of the command list. Due to the polling comparison match, the BCRTM also asserts a Standard Priority Interrupt and logs the event in the Interrupt
   Log List.

8.0 BUS MONITOR ARCHITECTURE

The BCRTM's bus monitor architecture is based on a Command Block structure and internal, host-programmable registers. Each message transacted over the MIL-STD-1553B bus (for a monitored RT address) has an associated Command Block, which the CPU sets up (see figures 17 and 18). The Command Block contains all the relevant message and RT status information as well as programmable function bits that allow the user to select functions and interrupts.

MONITOR CINROL/STATUS
1553 COMMAND WORD 1
1553 COMMAND WORD
DATA LIST POINTER
1553 STATUS WORD 1
1553 STATUS WORD 2
TAIL POINTER

Figure 17. BCRTM Bus Monitor Command Block

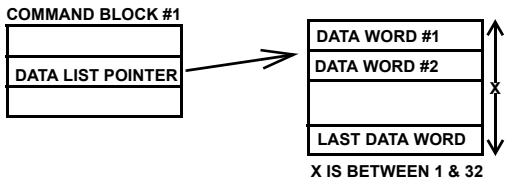


Figure 18. Data Placement

In a linked list Command Block structure, pointers delimit each Command Block to the successive block (see figure 19)

A data pointer 9 in the Command Block allows efficient space allocation because data blocks do not have to be placed contiguously in memory

A Monitor control/status word with an eight-bit Time Tag, an Interrupt When Addressed bit, a Message Error bit, and a Command Block Activated bit are in each Monitor Command Block. The user can access these control/status words to determine which Monitor Command Block, the host can determine when particular remote terminal has occurred.

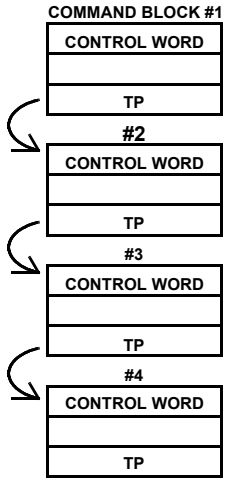
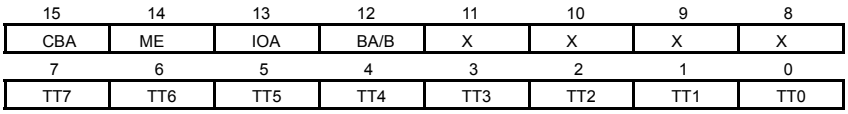


Figure 19. Monitor Command Block Tail Pointers



15	14	13	12	11	10	9	8
CBA	ME	IOA	BA/B	X	X	X	X
7	6	5	4	3	2	1	0
TT7	TT6	TT5	TT4	TT3	TT2	TT1	TT0

B0 - B7 **Time Tag** (64ms resolution)
B8 - B11 **Not Used**
B12 - **Bus A/B**: Defines which of the dual redundant 1553 buses on which the BCRTM received this message
B13 - **IWA**: Interrupt When Addressed. The BCRTM issues a standard priority interrupt when the monitor accesses this Bus Monitor Command block.
B14 - **ME**: Message Error. The BCRTM sets this bit if a 1553 message error occurred while receiving this message.
B15 - **CBA**: Command Block Activated. The BCRTM sets this bit when this Bus Monitor Command Block is accessed by the BCRTM.

Figure 20: Bus Monitor Control/Status Word

8.1 Monitor Functional Operation

The Bus Monitor function is a register-selectable mode of operation. The host uses registers 14, 16, and 17 in conjunction with Register 0 to program the BCRTM to monitor any combination of remote terminals or all of the remote terminals.

the BCRTM's memory mangement scheme gives the host a great deal of flexibility for processing 1553 bus data and is compatible with many bus monitoring applications. The host CPU is responsible for processing and initializing the Monitor Control Blocks. The Monitor structure is analogous to the Bus Controller Command Block scheme. The only real difference is the direction of information flow.

The number of Monitor Control Blocks that the host initializes depends on the data latency requirements for post-processing of 1553 commands. The linked list of Command Blocks could be connected in a loop fashion, with the BCRTM accessing the loop at one point and the host CPU processing the message behind that point. The bit positions of the BM control/status word are defined as shown in figure 20.

8.2 Monitor Error Detection

In the Monitor mode, the BCRTM checks all monitored messages for errors. Detectable errors include word count errors, long words, short words, Manchester errors (including zero crossing deviation), parity errors, and data contiguity.

Due to the nature of the 1553 protocol, it can be very difficult for any monitoring device to interpret some types of errors on the 1553 bus. For example, suppose an RT (whose RT Address the BCRTM is monitoring) incorrectly responds to a Broadcast command. The BCRTM, which is not receiving or transmitting the message, cannot distinguish between the erroneous status word and a new command sent from the Bus Controller, since the status sync is identified to the command sync. In this case, the BCRTM will put the extra status word in a new Monitor Command Block, and then report a message error due to the incorrect protocol on the erroneously interpreted status word from the RT transmitted.

8.3 Monitor Operational Sequence

The following is a general description of the operation of the BCRTM as it processes a monitored BC-to-RT message in the Monitor mode. DMA operations will vary slightly depending on the type of message (i.e., RT-to-BC, RT-toRT, etc.) It is assumed that the user has already written a "1" to Register 0, bit 0, and all other registers are in the appropriate state to enable Monitor operation.

Valid Command Received.

$\overline{\text{COMSTR}}$ goes active

- DMA Command Block Read. After receiving a valid command, the BCRTM initiates a burst DMA:

  DMA arbitration (BURST)
  Control Word read
  Command Word Write
  Data List Pointer read

Data Received.

- Data Word DMA.

  The BCRTM initiates a DMA cycle for each Data Word to store the data in memory, whether the command was a transmit or receive command to any valid monitored RT Address.

  DMA arbitration
  Data Word write (starting at Data List Pointer address, incremented for each successive word)

Status Word Received.

- Status Word DMA.

  DMA arbitration
  Status Word write.

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRTM is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

DMA arbitration (BURST)
Interrupt Status Word write
Command Block Pointer write
Tail Pointer read (into Register 6)
$\overline{\text{STDINTP}}$ pulses low
STDINTL asserted (if enabled)
Processing continues

Message Completion

Upon completion of the message, the BCRTM initiates a DMA cycle to update the status word and fetch the address of the next Monitor Command block:

DMA arbitration (BURST)
Control/ Status Word write
Tail Pointer write

9.0 EXCEPTION HANDLING AND INTERRUPT LOGGING

The exception handling scheme the BCRTM uses is based on an interrupt structure and provides a high degree of flexibility in:

- defining the events that cause an interrupt,
- selecting between High-Priority and Standard interrupts, and
- electing the amount of interrupt history retained.

The interrupt structure consists of internal registers that enable interrupt generation, control bits in the RT and BC data structures (see the Remote Terminal Descriptor Definition section, page 24, and the Bus Controller Command Block definition, page 30), and an Interrupt Log List that sequentially stores an interrupt events record in system memory.

The BCRTM generates the Interrupt Log List (see figure 17) to allow the host CPU to view the Standard Interrupt occurrences in chronological order. Each Interrupt Log List entry contains three words. The first, the Interrupt Status Word, indicates the type of interrupt (entries are only for interrupts enabled). In the BC mode, the second word is a Command Block Pointer that refers to the corresponding Command Block. In the RT mode, the second word is a Descriptor Pointer that refers to the corresponding subaddress descriptor. The CPU-initialized third word, a Tail Pointer, is read by the BCRTM to determine the next Interrupt Log List address. The list length can be as long or as short as required. The configuration of the Tail Pointers determines the list length.

The host CPU initializes the list by setting the tail pointers. This gives flexibility in the list capacity and the ability to link the list around noncontiguous blocks of memory. The host CPU sets the list's starting address using the Interrupt Log List Register. The BCRTM then updates this register with the address of the next list entry.

The internal High-Priority Interrupt Status/Reset Register indicates the cause of a High-Priority Interrupt. The High-Priority Interrupt signal is reset by writing a "1" to the set bits in this register.

The interrupt structure also uses three BCRTM -driven output signals to indicate when an interrupt event occurs:

$\overline{\text{STDINTL}}$ Standard Interrupt Level. This signal is asserted when one or moreof the events enabled in the Standard Interrupt Enable Register occurs. Clear the signal by resetting the Standard Interrupt bit in the High-Priority Interrupt Status/Reset Register.

$\overline{\text{STDINTP}}$ Standard Interrupt Pulse. This signal is pulsed for each occurrence of an event enabled in the Standard Interrupt Enable Register.

$\overline{\text{HPINT}}$ High-Priority Interrupt. This signal is asserted for each occurrence of an event enabled in the High-Priority Interrupt/Enable Register. Writing to the corresponding bit in the High-Priority Status/Reset Register resets it.

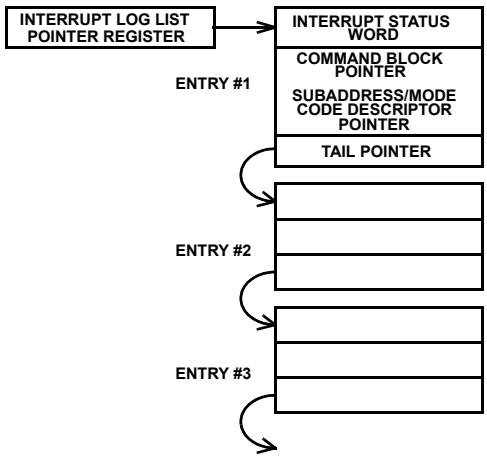


Figure 21. Interupt Log List

Interrupt Status Word Definition
All bits in the Interrupt Status Word are active high and have the following functions:

Bit Number	Description
BIT 15	Interrupt Status Word Accessed. The BCRTM always sets this bit during the DMA Write of the Interrupt Status Word. If the CPU resets this bit after reading the Interrupt Status Word, the bit can help the CPU determine which entries have been acknowledged.
BIT 14	No Response Time-Out (Message Error condition). Further defines the Message Error condition to indicate that a Response Time-Out condition has occurred.
BIT 13	(RT) Message Error (ME). Indicates the ME bit was set in the 1553 status word response.
BITs12-8	Reserved.
BIT 7	(RT) Subaddress Event or Mode Code with Data Word Interrupt. Indicates a descriptor control word has been accessed with either an Interrupt Upon Valid Command Received bit set or an Interrupt when Index=0 bit set (and the Index is decremented to 0).
BIT 6	(RT) Mode Code without Data Word Interrupt. Indicates a mode code has occurred with an Interrupt When Addressed interrupt enabled.
BIT 5	(RT) Illegal Broadcast Command. Applies to receive commands only. This bit indicates that a received command,due to an illegal mode code or subaddress field, has been received in the broadcast mode. This does not include invalid commands.
BIT 4	(RT) Illegal Command. This indicates that an illegal command has occurred due to an illegal mode code or subaddress and T/R field. This does not include invalid commands.
BIT 3	(BC) Polling Comparison Match. Indicates a polling comparison interrupt.
BIT 2	(BC) Retry Fail. Indicates all the programmed retries have failed.
BIT 1	(BC, RT) Message Error. Indicates a Message Error has occurred.
BIT 0	(BC) Interrupt and Continue. This corresponds to the interrupt and continue function described in the Command Block.

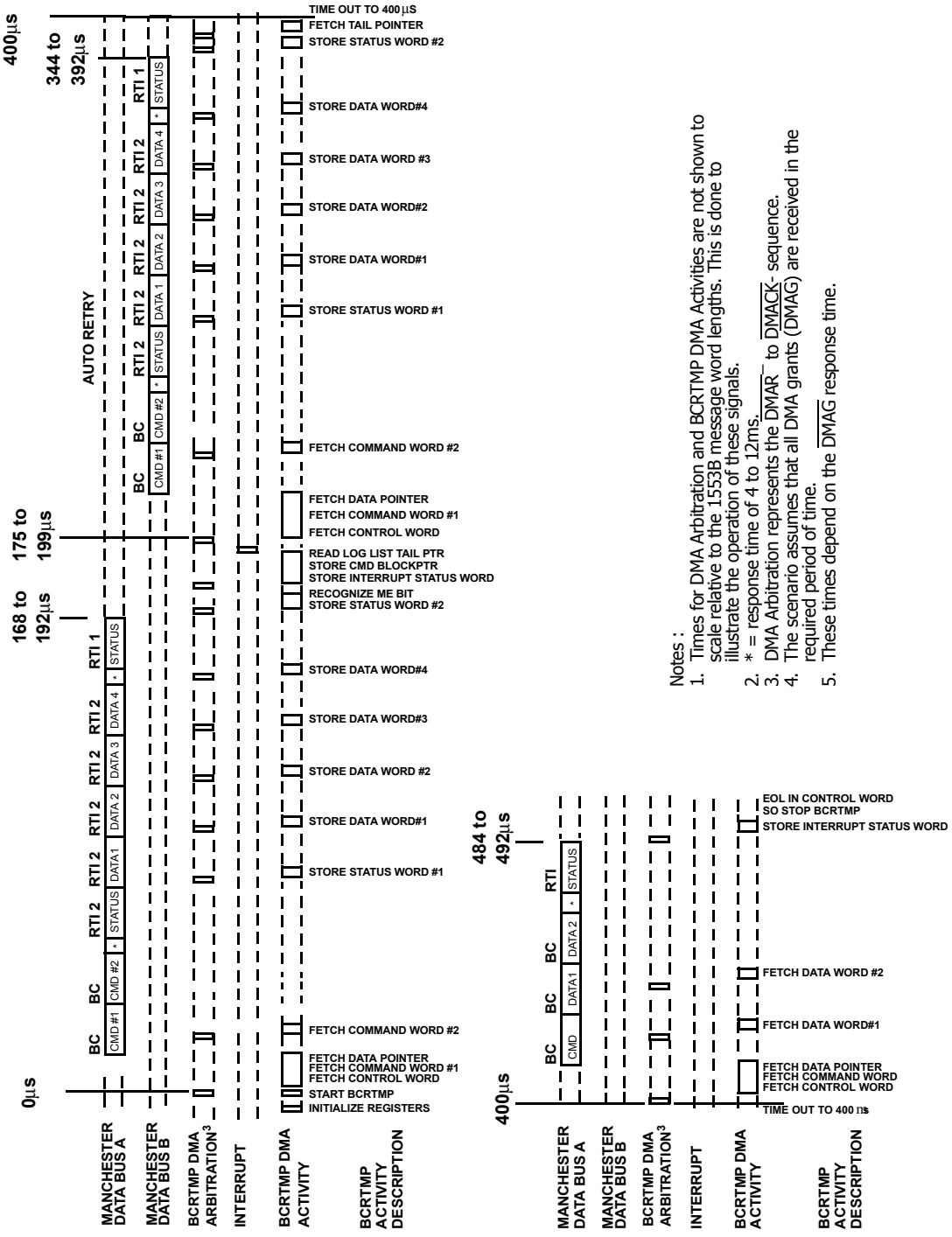


Figure 22. Bus Controller Scenario

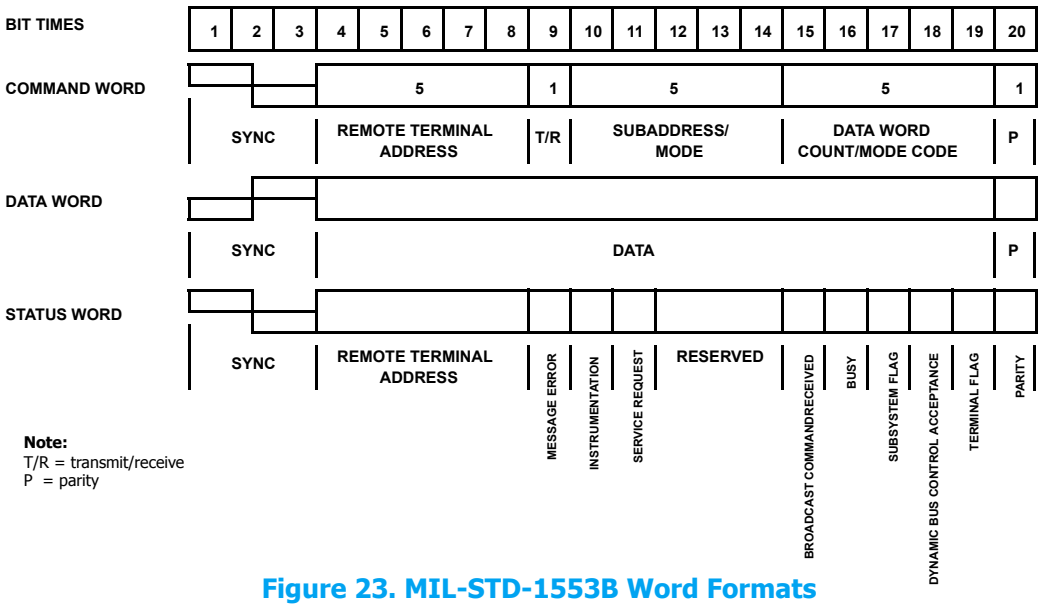


Figure 23. MIL-STD-1553B Word Formats

10.0 ABSOLUTE MAXIMUM RATINGS *

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	-0.3 to +7.0	V
$V_{I/O}$	Voltage on any pin	-0.3 to V_{DD} +0.3	V
I_I	DC input current	±10	mA
T_{STG}	Storage temperature	-65 to + 150	°C
T_{JMAX}	Maximum junction temperature	+175	°C
P_D	Average power dissipation [1]	300	mW
Θ_{JC}	Thermal resistance, junction to-case	12	°C/W

Notes:

1. Does not reflect the added PD due to an output short-circuited.

* Stresses outside the listedabsolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATION CONDITONS

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	4.5 to 5.5	V
T_C	Temperature range	-55 to +125	° C
F_O	Operating frequency	12 ±.01%	MHz

11.0 DC ELECTRICAL CHARACTERISTICS

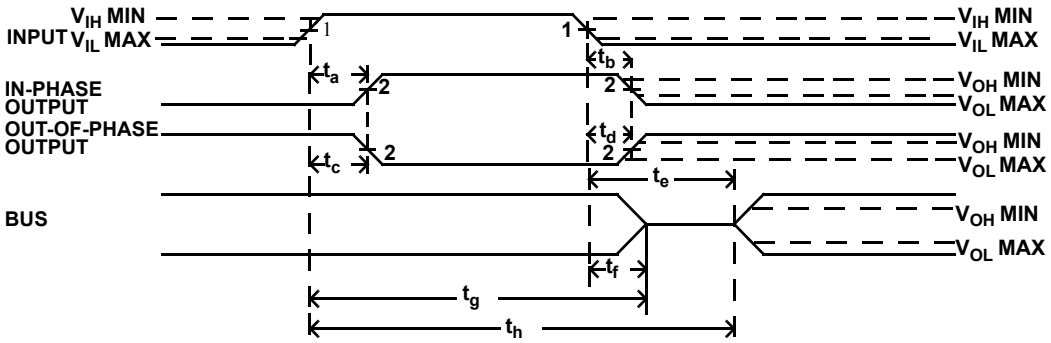
(V_{DD} = 5.0V ± 10%; -55°C <T_C <+125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage TTL inputs			0.8	V
V_{IH}	High-level input voltage TTL inputs		2.2		V
I_{IN}	Input leakage current TTL inputs Inputs w/ pull-up resistors Inputs w/ pull-up resistors	$V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	-1 -10 -900	-1 -10 -150	µA µA µA
V_{OL}	Low-level output voltage TTL outputs	I_{OL} = 3.2mA		0.4	V
V_{OH}	High-level output voltage TTL outputs	I_{OH} = -400mA	2.4		V
I_{OZ}	Three-state output leakage current TTL outputs	$V_{OUT} = V_{DD}$ or V_{SS}	-10	10	µA
I_{OS}	Short-circuit output current [1, 2]	V_{DD} = 5.5V, $V_{OUT} = V_{DD}$ V_{DD} = 5.5V, V_{OUT} = 0V	-100	100	mA mA
C_{IN}	Input capacitance [3]	f = 1MHz @ 0V		15	pF
C_{OUT}	Output capacitance [3]	f = 1MHz @ 0V		20	pF
C_{IO}	Bidirect I/O capacitance [3]	f = 1MHz @ 0V		25	pF
I_{DD}	Average operating current [1, 4]	f = 12MHz, C_L = 50pF		50	mA
Q_{IDD}	Quiescent current	See Note 5, Tc = +125°C Tc = 25°C, -55°C		1 35	mA µA

NOTES:
1. Supplied as a design limit. Tested only at initial qualification and after any design or proess changes which may affect this parameter.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Measured only for initial qualification, and after process or design changes which may affect input/output capacitance.
4. Includes current through input pull-up. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large current surge.
5. All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

12.0 AC ELECTRICAL CHARACTERISTICS

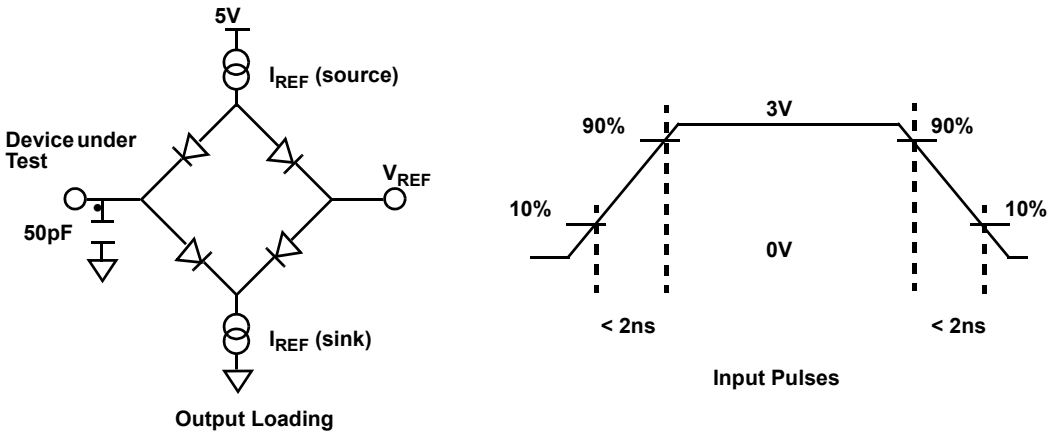
(OVER RECOMMENDED OPERATING CONDITIONS)



SYMBOL	PARAMETER
t_a	INPUT↑ to response↑
t_b	INPUT↑ to response↓
t_c	INPUT↑ to response↓
t_d	INPUT↓ to response↑
t_e	INPUT↓ to data valid
t_f	INPUT↓ to high Z
t_g	INPUT↑ to high Z
t_h	INPUT↑ to data valid

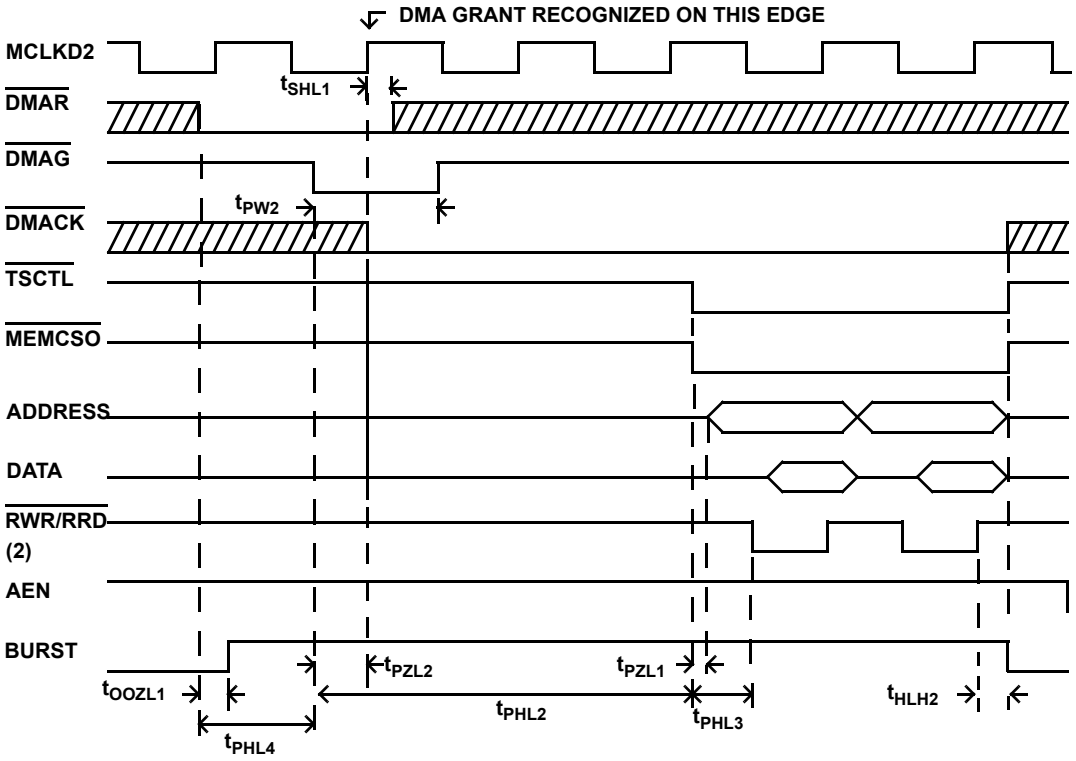
Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50pF load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 24. Typical Timing Measurements



Note:
50pF including scope probe and test socket

Figure 25. AC Test Loads and Input Waveforms

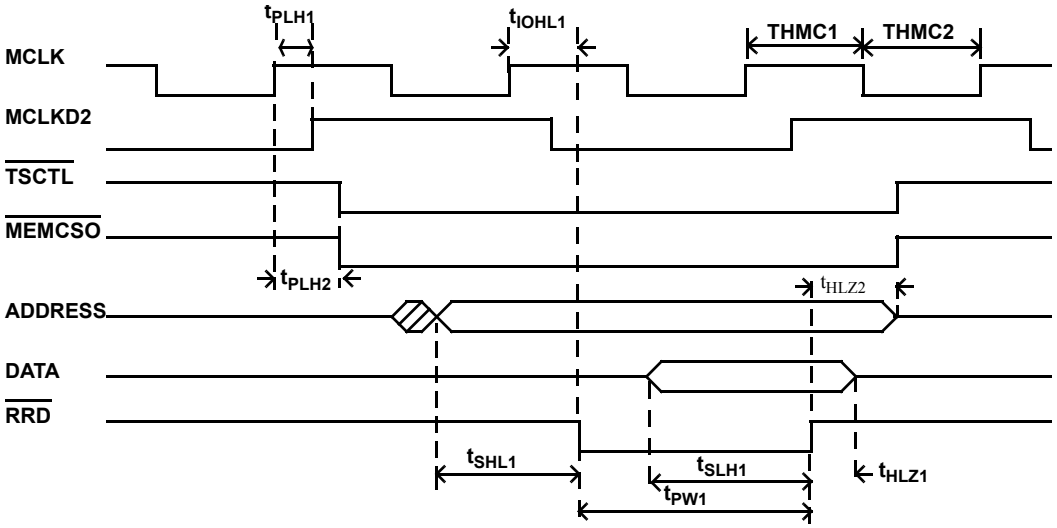


SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}[6]	DMACK↓ to DMAR High Impedance	-12	10	ns
t_{PZL2}	DMAG↓ to DMACK↓ [3]	-15	45	ns
t_{PHL2}[1]	DMAG↓ to TSCTL↓	2xMCLK	4xMCLK	ns
t_{PZL1}[6]	TSCTL↓ to ADDRESS valid	-15	40	ns
t_{HLH2}	RWR/RRD↑ to DMACK↑	THMC1-15	THMC1+20	ns
t_{PHL3}	TSCTL↓ to RWR/RRD↓	MCLK-20	MCLK+20	ns
t_{PW2}[1]	DMAG↓ to DMAG↑	MCLK	6xMCLK	ns
t_{OOZL1}	DMAR↓ to BURST↑	-10	10	ns
t_{PHL4}	DMAR↓ to DMAG↓ [5]	0	3.5 (1.9)	µs
t_{PHL4}	DMAR↓ to DMAG↓ [4]	0	1.9 (0.8)	µs

Notes:
1. Guaranteed by functional testing.
2. See figures 23 & 24 for detailed DMA read and write timing.
3. DMAG must be asserted at least 45ns prior to the rising edge of MCLKD2 in order to be recognized for the next MCLKD2 cycle. If DMAG is not asserted at least 45ns prior to the rising edge of MCLKD2, DMAG is not recognized until the following MCLKD2 cycle.
4. Provided MCLK = 12MHz. Number in parentheses indicates the longest DMAR to DMAG allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT Response Time. The number not in parentheses applies to all other circumstances.
5. Provided MCLK = 6MHz. Number in parentheses indicates the longest DMAR DMAG allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT Response Time. The number not in parentheses applies to all other circumstances
6. Tested only at initial qualification, and after any design or process changes which may affect this characteristic.

MCLK = period of the memory clock cycle.
BURST signal is for multiple-word DMA accesses.
THMC1 is equivalent to the positive phase of MCLK (see figure 23).

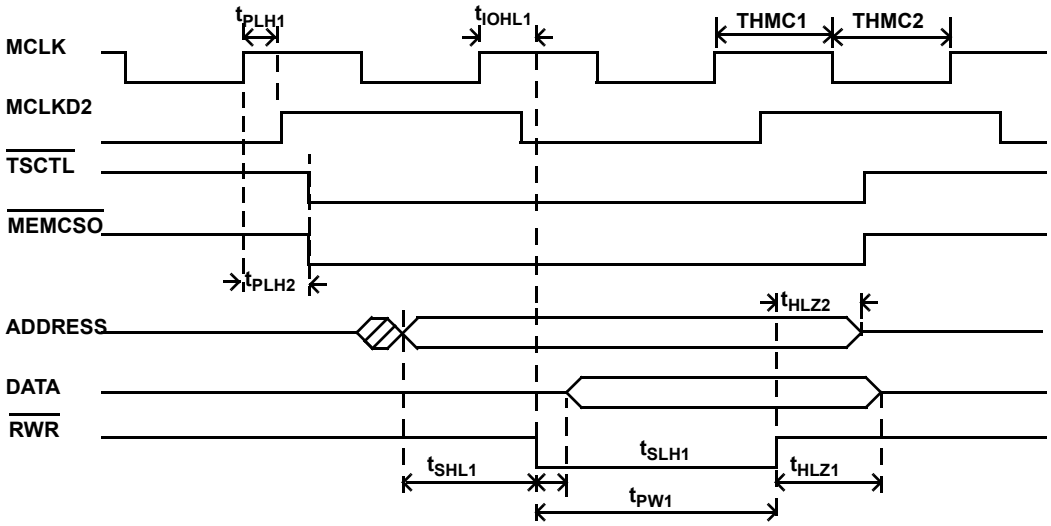
Figure 26. BURST DMA Timing



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to RRD↓	(ADDRESS setup)	THMC2-10	THMC2+10	ns
t_{PW1}	$\overline{RRD}$↓ to $\overline{RRD}$↑		MCLK-10	MCLK+5	ns
t_{HLZ2}	$\overline{RRD}$↑ to ADDRESS High Impedance	(ADDRESS hold)	THMC1-15	THMC1+20	ns
t_{HLZ1}	$\overline{RRD}$↑ to DATA High Impedance	(DATA hold)	5	-	ns
t_{SLH1}	DATA valid to $\overline{RRD}$↑	(DATA setup)	40	-	ns
t_{PLH1} [1]	MCLK↑ to MCLKD2↑		0	40	ns
t_{PLH2}	MCLK↑ to $\overline{TSCTL}$/$\overline{MEMCSO}$↓		0	40	ns
t_{IOHL1} [1]	MCLK↑ to $\overline{RRD}$↓		0	60	ns

Note:
1. Guaranteed by test.

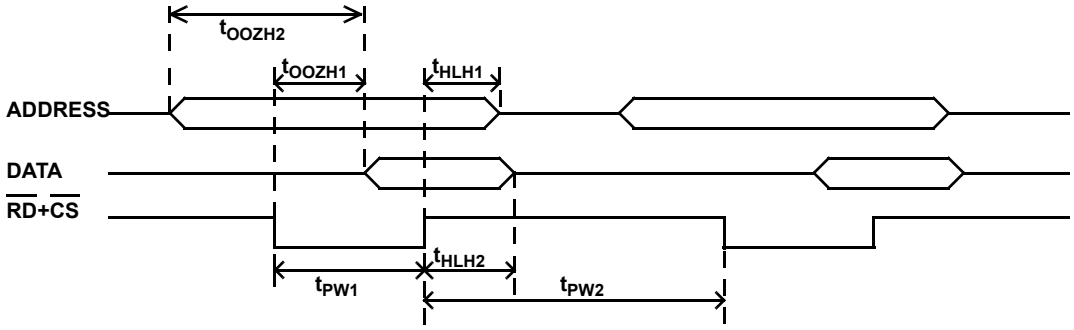
Figure 27. BCRTM DMA Read Timing (One-Word Read)



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to RWR↓	(ADDRESS setup)	THMC2-10	THMC2+15	ns
t_{OOZL1} 1	RWR↓ to DATA valid		-5	30	ns
t_{HLZ1}	RWR↑ to DATA High Impedance	(DATA hold)	THMC1-15	THMC1+25	ns
t_{HLZ2}	RWR↑ to ADDRESS High Impedance	(ADDRESS hold)	THMC1-15	THMC1+20	ns
t_{PW1}	RWR↓ to RWR↑		MCLK-10	MCLK+5	ns
t_{PLH1} 1	MCLK↑ to MCLKD2↑		0	40	ns
t_{PLH2}	MCLK↑ to TSCTL/MEMCSO↓		0	40	ns
t_{IOHL1} 1	MCLK↑ to RWR↓		0	60	ns

Note:
1. Guaranteed by test.

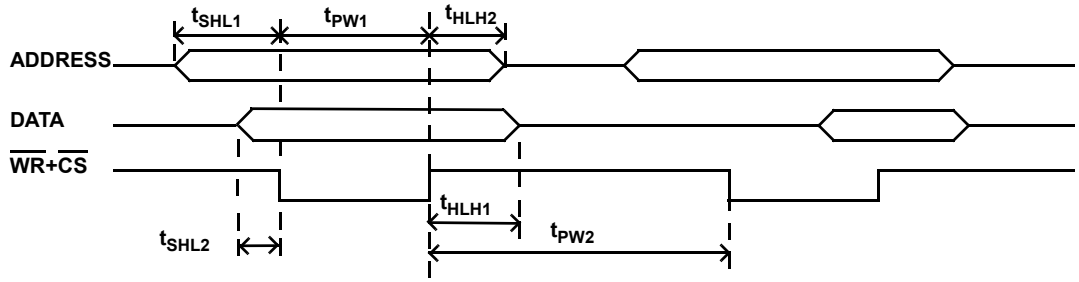
Figure 28. BCRTM DMA Write Timing (One-Word Write)



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{OOZH2}	ADDRESS valid to DATA valid		-	80	ns
t_{HLH2}	RD+CS↑ to DATA High Impedance	(DATA hold)	0	50	ns
t_{OOZH1} 2	RD+CS↓ to DATA valid	(DATA access)	-	60	ns
t_{HLH1}	RD+CS↑ to ADDRESS High Impedance	(ADDRESS hold)	5	-	ns
t_{PW1}	RD+CS↓ to RD+CS↑		60	-	ns
t_{PW2} 1	RD+CS↑ to RD+CS↓		80	-	ns

Notes:
1. Guaranteed by functional test.
2. User must adhere to both t_{OOZH1} and t_{OOZH2} timing constraints to ensure valid data.

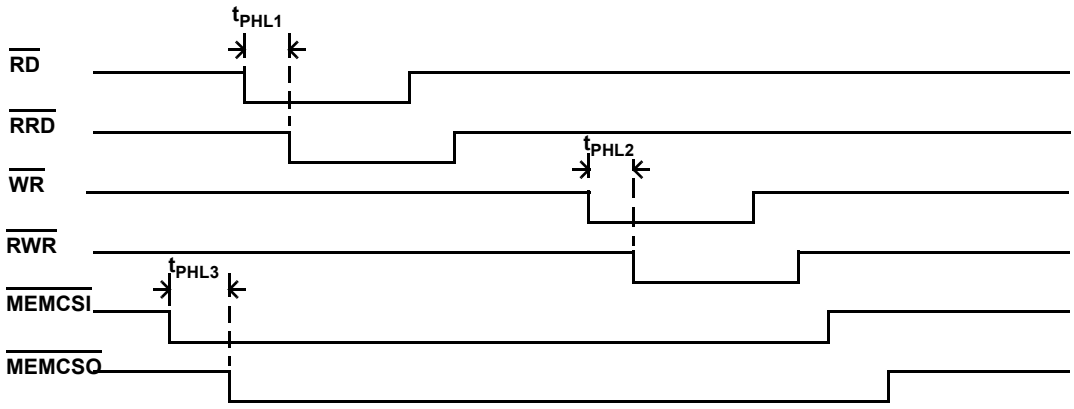
Figure 29. BCRTM Register Read Timing



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to WR+CS↓	(ADDRESS setup)	60	-	ns
t_{SHL2}	DATA valid to WR+CS↓	(DATA setup)	5	-	ns
t_{PW1}	WR+CSØ to WR+CS↑		60	-	ns
t_{HLH1}	WR+CS↑ to DATA High Impedance	(DATA hold)	10	-	ns
t_{HLH2}	WR+CS↑ to ADDRESS High Impedance	(ADDRESS hold)	10	-	ns
t_{PW2}	WR+CS↑ to WR+CS↓		80	-	ns

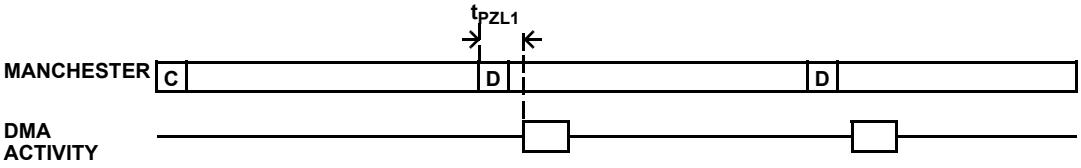
Notes:
1. Guaranteed by functional test.

Figure 30. BCRTM Register Write Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PHL1} [1]	$\overline{RD}\downarrow$ to $\overline{RRD}\downarrow$	0	30	ns
t_{PHL2} [1]	$\overline{WR}\downarrow$ to $\overline{RWR}\downarrow$	0	35	ns
t_{PHL3} [1]	MEMCSI↓ to MEMCSO↓	0	30	ns

Figure 31. BCRTM Dual-Port Interface Timing Delays

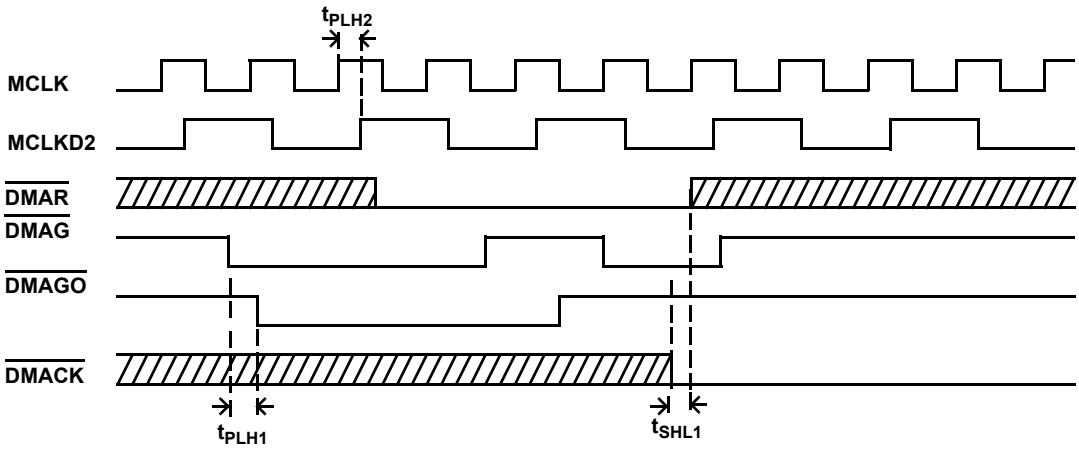


SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PZL1} [1, 2]	Data word to DMA activity	0	4	µs

This diagram indicates the relationship between the incoming Manchester code DMA activity (i.e., $\overline{DMAR}\downarrow$ to $\overline{DMACK}\uparrow$).

Note:
1. The pulsewidth = (11µs -t_{DMA} -t_{PZL1}) where t_{DMA} is the time to complete DMA activity (i.e., $\overline{DMAR}\downarrow$ to $\overline{DMACK}\uparrow$).
2. Guaranteed by functional test.

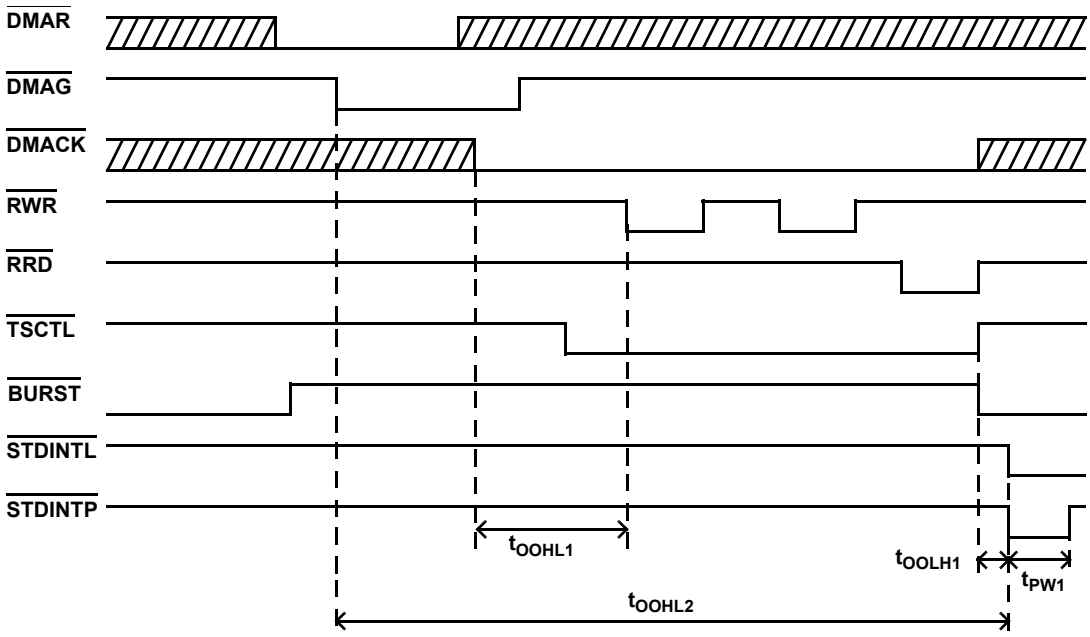
Figure 32. DMA Activity (RT Mode)



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PLH1}[1]	$\overline{DMAG}\downarrow$ to $\overline{DMAGO}\downarrow$	0	30	ns
t_{SHL1}	$\overline{DMACK}\downarrow$ to $\overline{DMAR}$ High Impedance	-12	10	ns
t_{PLH2}	MCLK$\uparrow$ to MCLKD2$\uparrow$	0	40	ns

Notes:
1. When $\overline{DMAG}$ is asserted before $\overline{DMAR}$, the $\overline{DMAG}$ signal passes through the BCRTM as $\overline{DMAGO}$.

Figure 33. BCRTM Arbitration when DMAG is Asserted before Arbitration



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{OOLH1}	TSCTL↑ to STDINTP/STDINTL↓	-	1	µs
t_{PW1}	STDINTP↓ to STDINTP↑	320	340	ns
t_{OOHL1}	DMACK↓ to RWR↓	3xMCLK-10	5xMCLK	ns
t_{OOHL2}	DMAG↓ to STDINTL↓	8xMCLK	12xMCLK	ns

Note:
Address and data bus relationships (not shown) are identical to figure 22.

Figure 34. BCRTM Interrupt Log List Entry Operation Timing

13.0 PACKAGE OUTLINE DRAWINGS

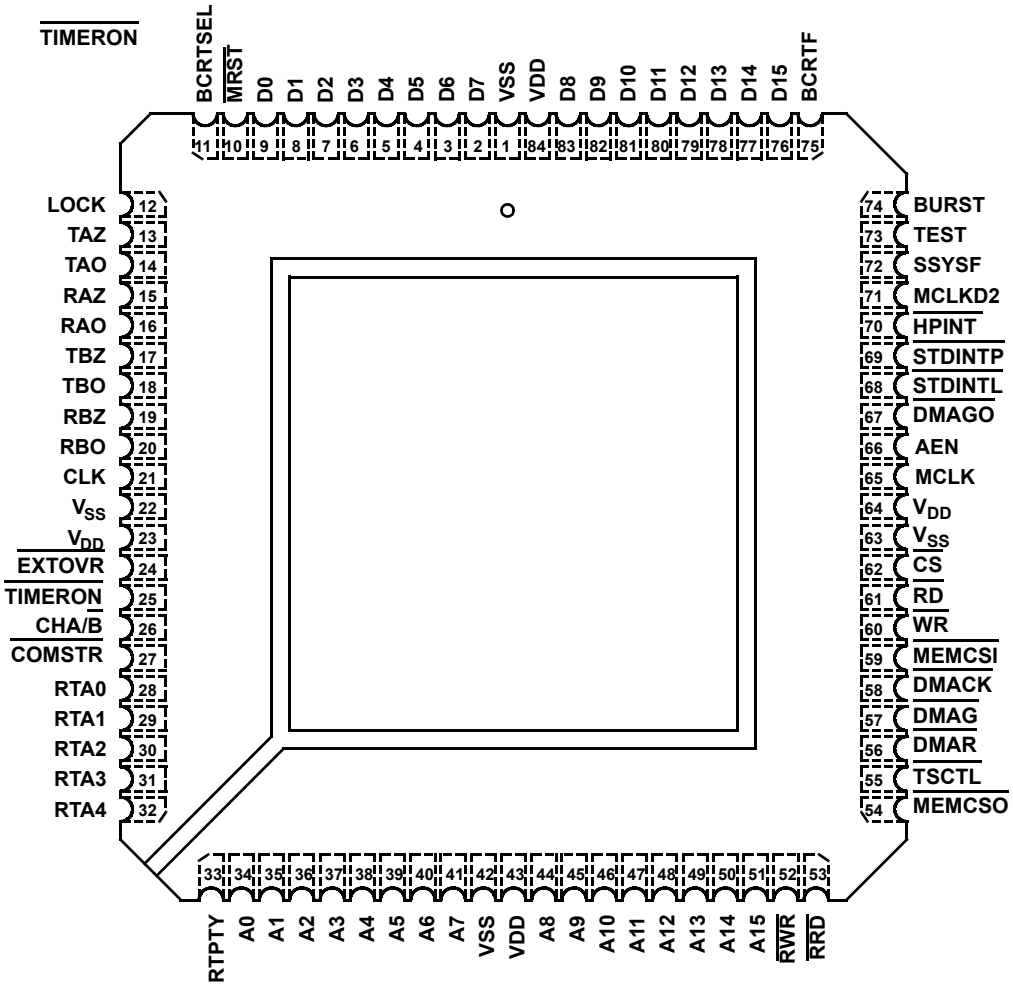


Figure 35a. BCRTM Flatpack Pin Identification (Top View)
(Flatpack Leads Omitted for Clarity)

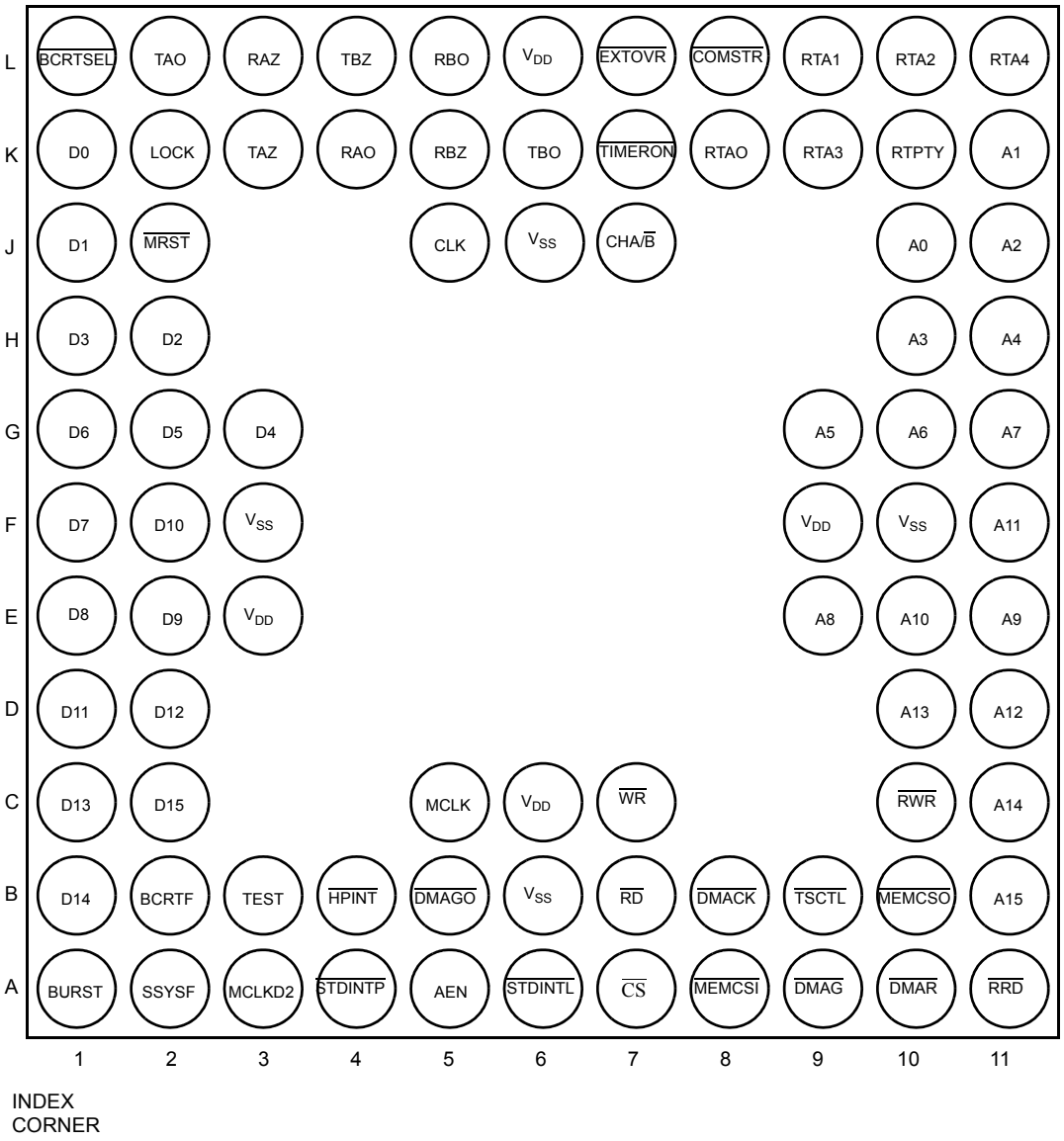
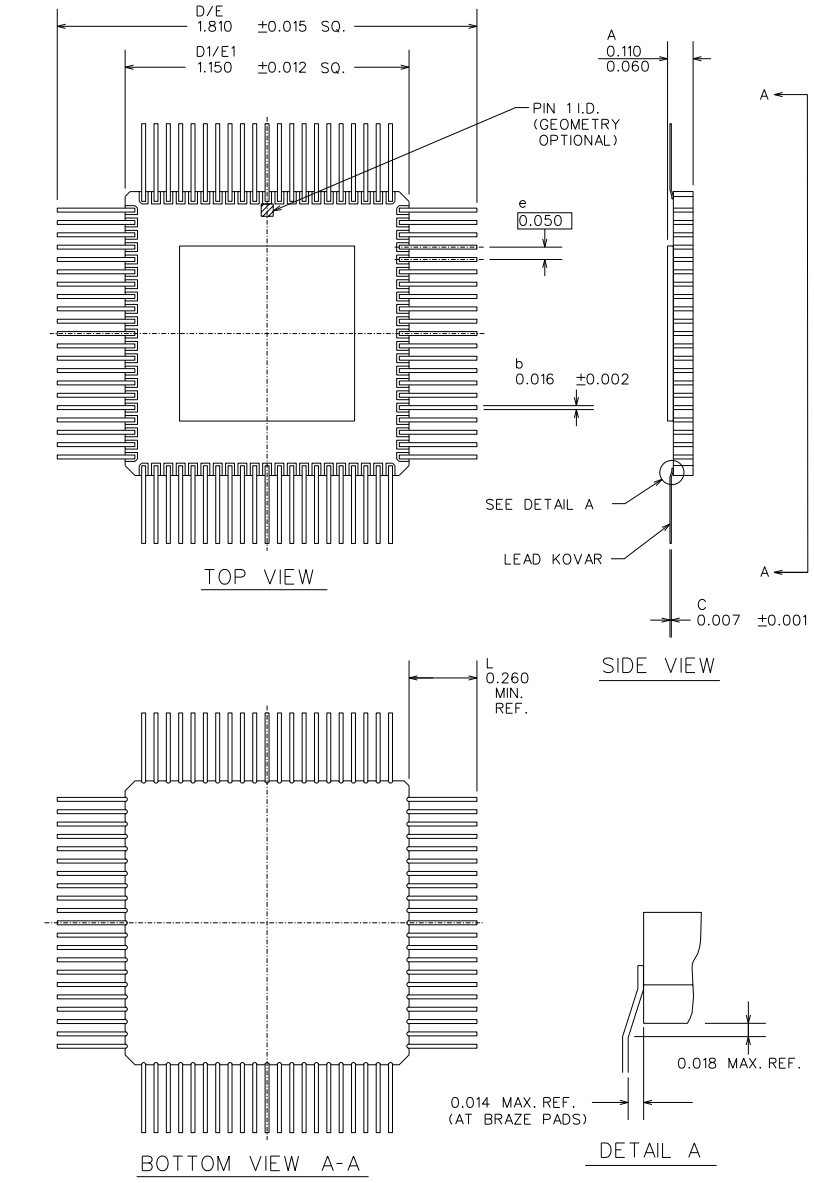


Figure 35b. BCRTM Pingrid Array Pin Indentification (Bottom View)



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-STD-1835

Figure 36a. 84-Lead Flatpack

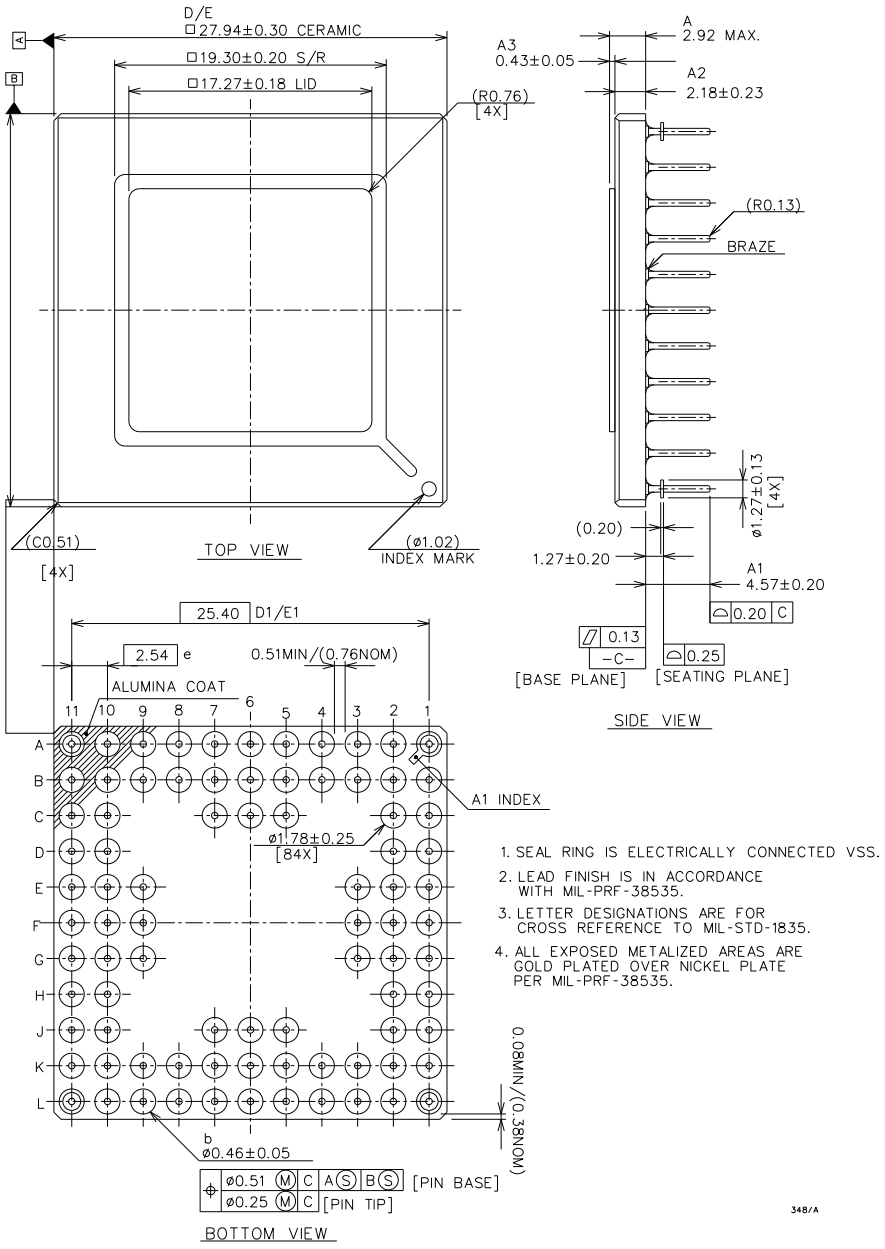
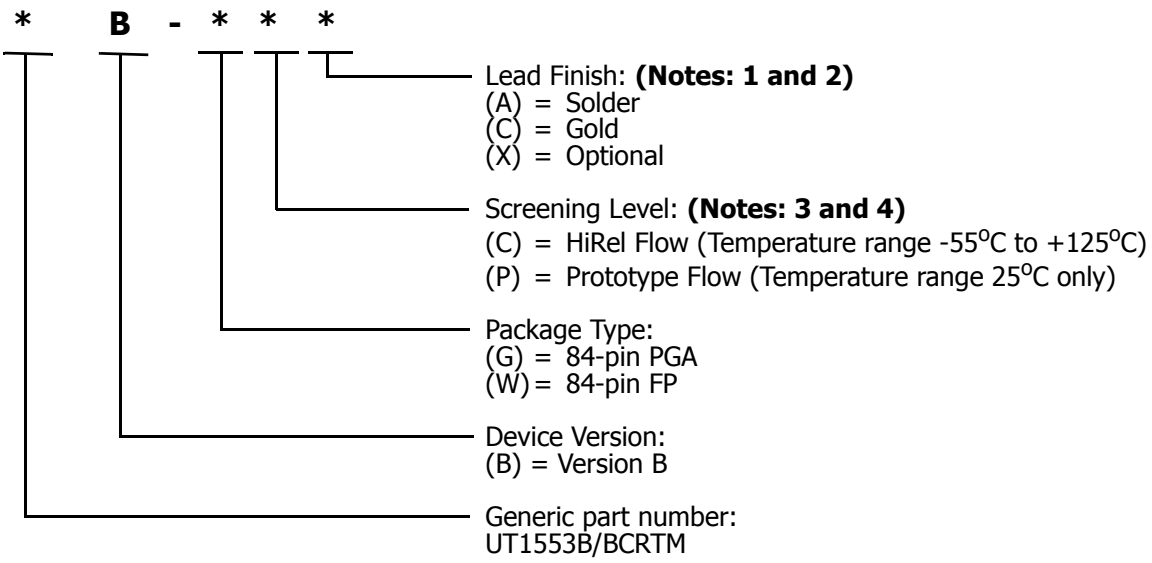


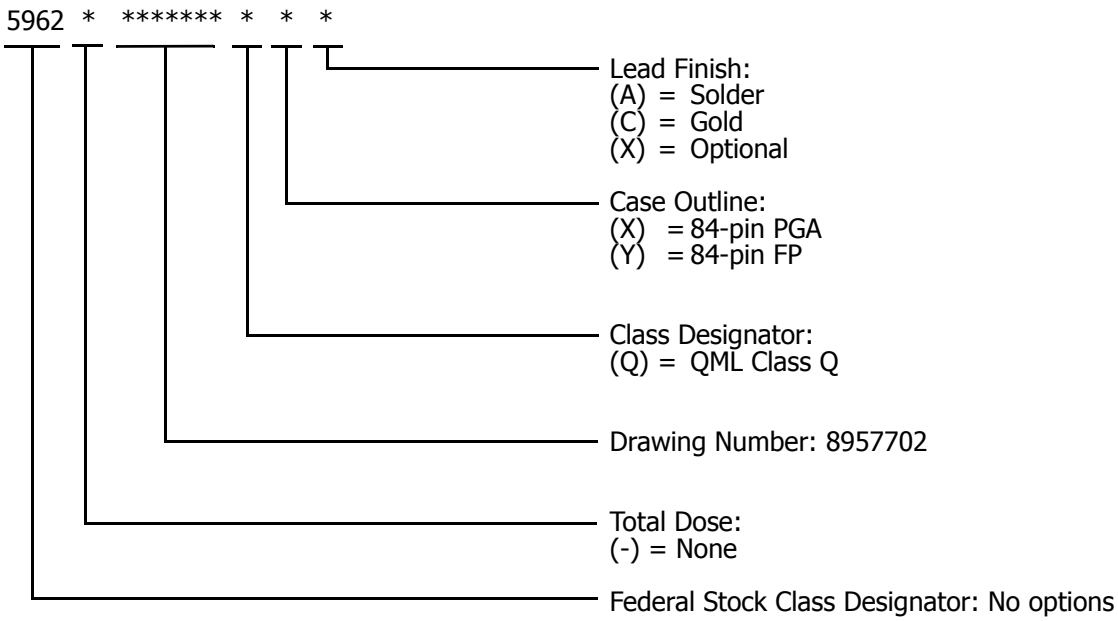
Figure 36b. 84-Lead PGA

14.0 ORDERING INFORMATION

UT1553B/BCRTM Version B Bus Controller/Remote Terminal



Notes:
1. Lead finish is "C" (Gold) only.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. HiRel flow per Aeroflex Manufacturing Flows Document.
4. Prototype Flow per Aeroflex Manufacturing Flows Document. Lead finish is GOLD only.



Notes:
1. Lead finish is "C" (Gold) only.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

REVISION HISTORY

Date	Rev. #	Change Description	Initials
05/27/2016	1.0.0	Released Datasheet	TM

Template Revision: A

Cobham Semiconductor Solutions – Datasheet Definitions

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Released Datasheet - Shipping QML & Reduced Hi – Rel

For Product Concept/Brief: Export classification information will be added at a later date.

(Search for ECCN (Classification) by part number or SMD HERE. Please pick one of the following statements. Delete the other statements and this note. Contact your export control officer with questions.)

The product or data that is the subject of this transaction, to be provided by Aeroflex, is subject to the International Traffic in Arms Regulations ("ITAR") (22 CFR 120-130) and may not be exported, reexported or otherwise transferred to a foreign person, or outside the United States without authorization from the U.S. Department of State. By accepting this product or data, the recipient acknowledges and accepts these controls and agrees to comply with all applicable U.S. laws and regulations, including the ITAR, in handling this product or data, including any export, reexport or transfer of the product or data to another person or entity.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.

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