Application Specific Integrated Circuit (ASIC)

UT1752FC FPGA-to-ASIC

Product Brief
Cobham.com/HiRel
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COBHAM

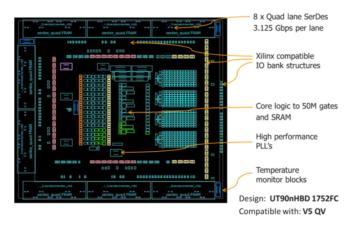**The most important thing we build is trust**

FEATURES

- ❑ Cobham UT90nHBD ASIC offering
- ❑ RHBD multi-Vt cell and IO library
- ❑ Compatible with Virtex-5QV 1752LGA CN/CF package
- ❑ Multiple pre-defined die frames and package substrates supporting up to 50 million equivalent 2-nand gates
- ❑ With AlSiC heat sink, Theta JC <0.15 C°/W
- ❑ Support for MIL-STD-123 screened 0402 decoupling capacitors
- ❑ Support for solder columns
- ❑ Proven development methodology using existing QML ceramic
- ❑ Daisy chain package available for board development
- ❑ SEU / Soft Error Immune 3.125Gbps SERDES IP, pin for pin, protocol compatible with Virtex-5QV, up to 32 SERDES RX/TX lanes
- ❑ Commercial and SEE hardened memory compilers

OPERATIONAL ENVIRONMENT

- ❑ Temperature Range: -55°C to +125°C
- ❑ Total Ionizing Dose: 100 krad(Si)
- ❑ SEL Immune: <110MeV-cm^2/mg
- ❑ SET Rate: 5.3×10^{-3} events/device-day

APPLICATIONS

- ❑ QML-Y FPGA to ASIC conversions
- ❑ QML-Y System on Chip (SoC) ASICs
- ❑ Commercial and Military Space products

INTRODUCTION

FPGA's allow for fast prototype time, but are expensive flight parts that have degraded speed performance over an ASIC solution. Cobham's ASIC solution allows you to port your FPGA design into an ASIC in record time using our pin-compatible package and FPGA conversion framework. Our ASIC's offer cost savings over your current FPGA, contain up to 5x the functionality of a single Virtex-5QV, with enhanced speed performance.

The UT1752FC FPGA-to-ASIC product provides a path to create a Virtex-5QV FPGA pin-for-pin and functionally equivalent QML Class-Y 90nm ASIC. The UT1752FC FPGA-to-ASIC product consists of five elements:
- Pre-defined set of Cobham UT90nHBD ASIC die frames with existing ceramic 1752 LGA substrates
- QML certified UT90nHBD ASIC development methodology
- QML Class Y certified flip-chip assembly flow with support for AlSiC heat sink, MIL-PRF-123 0402 capacitors, and solder column attach
- Pre-defined production test and burn-in hardware
- 1752 LGA daisy chain package with solder column option

8 x Quad lane SerDes
3.125 Gbps per lane

Xilinx compatible
IO bank structures

Core logic to 50M gates
and SRAM

High performance
PLL's

Temperature
monitor blocks

Design: **UT90nHBD 1752FC**
Compatible with: **V5 QV**