

The most important thing we build is trust

FEATURES

- ❑ Available in UT90nHBD ASIC library based upon an advanced 90nm silicon gate CMOS process in a commercial fab
- ❑ TID hardness > 1MRad (Si)
- ❑ SEU/Soft Error immune
- ❑ Quad channel transceiver with high speed CML outputs also available as Single and Dual channel transceivers in the UT90nHBD library
- ❑ 3.125Gbps maximum data rate per lane
- ❑ 10Gbps data throughput when 8b/10b encoding is used with this four lane macro
- ❑ Integrated low jitter PLL using external clock reference
- ❑ PLL reference: 156.25MHz or 312.5MHz
- ❑ Low 240mW per lane power consumption
- ❑ Dual supplies required: 1.8V and 1.0V
- ❑ On-chip 100Ω auto-adjustable, differential transmit terminations

- ❑ Adjustable transmit pre-emphasis with 2 tap transmit Feed Forward Equalization (FFE)
- ❑ Integrated 50Ω receiver termination resistors
- ❑ On chip receive equalization
- ❑ Testability (Scan, BIST, and loopback modes)
- ❑ Supports both backplanes and cables

APPLICATIONS

- ❑ 10G Base-X (XAUI)
- ❑ Proprietary lines and protocol
- ❑ Point-to-point data transmission

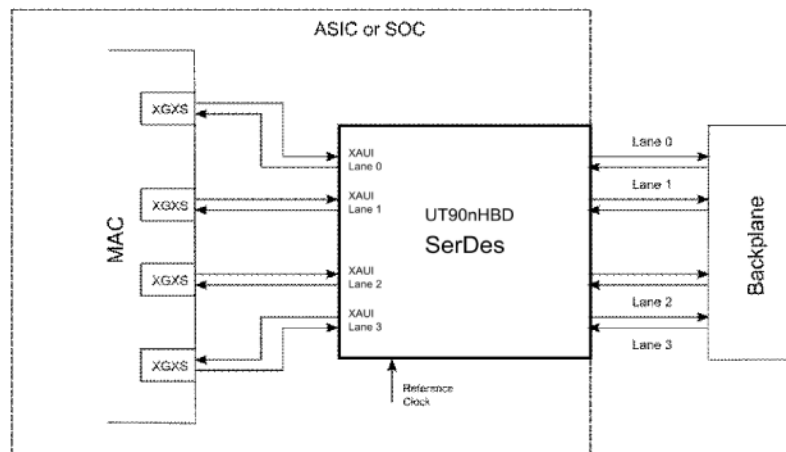


Figure 1: Quad Channel Functional Block Diagram

INTRODUCTION

The UT90nHBD SerDes is RadHard, quad channel, Serializer/Deserializer (SerDes) IP targeted for 10G XAUI applications in 90nm CMOS SoC ASIC designs. This SerDes macro block is a half-rate architecture providing a robust transmitter with 8/10/16/20:1 serialization, Feed Forward Equalization (FFE) and pre-emphasis, and a robust receiver with 1:8/10/16/20 deserialization. Included is a low jitter reference PLL which uses an external clock input to provide a common clock across 4 Tx/Rx lanes. With 8b/10b encoding, this UT90nHBD SerDes can also be used as a general purpose serializer/deserializer. Single and dual channel SerDes macro block are also available.

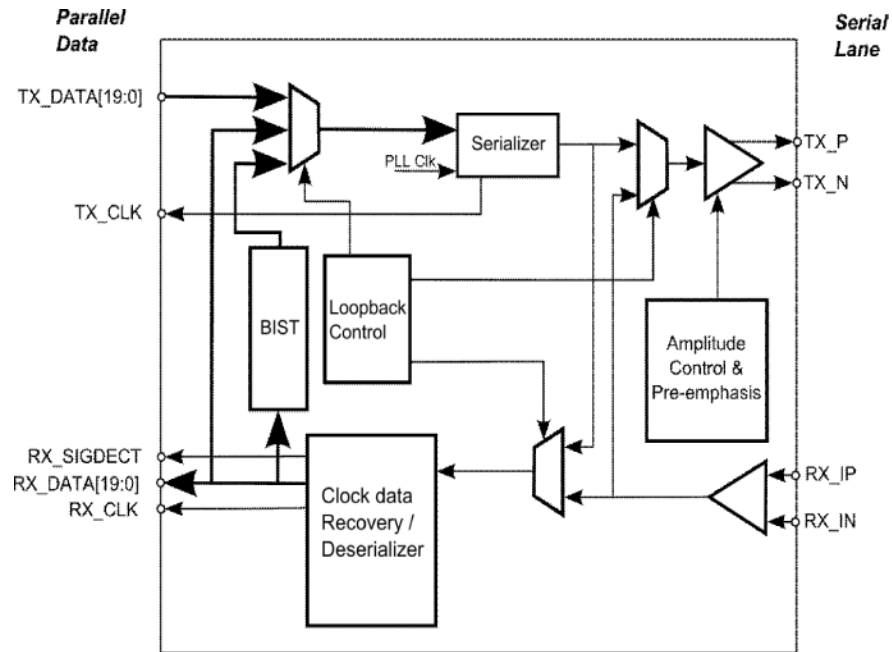


Figure 2: Single Channel Block Diagram

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