Thermal Model Generation and Analysis of the MDC22GCMG-67E0 Multiple Device Canopy

Baseline Results

Legacy Electronics
Project: TDSW130509-01
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Mentor Graphics®

Objectives

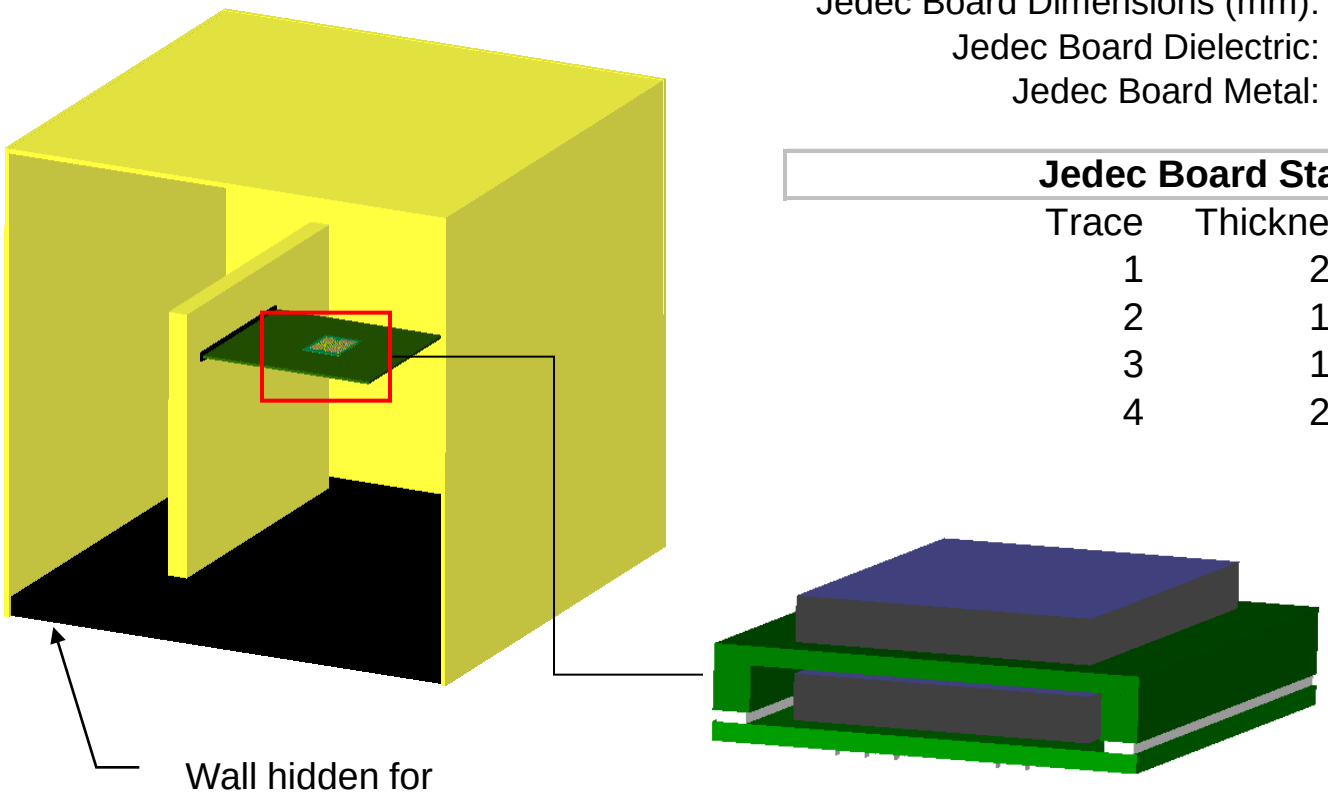
- **To build a Computational Fluid Dynamics FloTHERM® model of Legacy Electronics' MDC22GCMG-67E0 multiple device canopy, and simulate the package when mounted in a JEDEC Still-Air test environment.**
  - Power Dissipation
    - Total Power: 0.36 Watts/device x 2 = 0.72 W
  - Air-Flow Environment
    - Free Convection

JEDEC Still-Air Test Environment

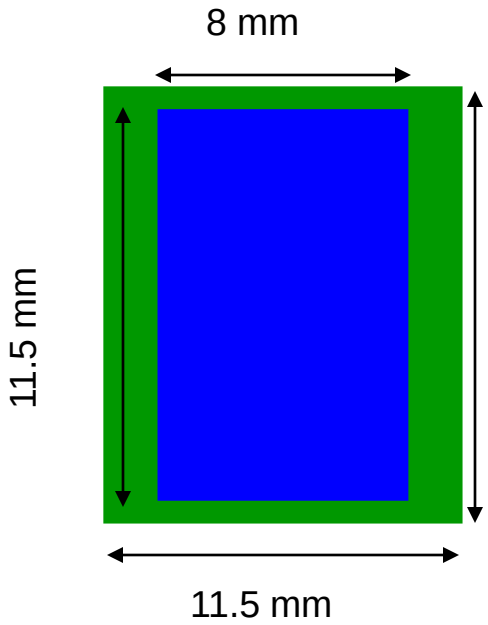
Ambient Temperature:	20 °C
Elevation:	Sea Level
Enclosure Dimensions (in):	12 X 12 X 12
Jedec Board Dimensions (mm):	114.5 X 101.6 X 1.6
Jedec Board Dielectric:	FR4
Jedec Board Metal:	Cu

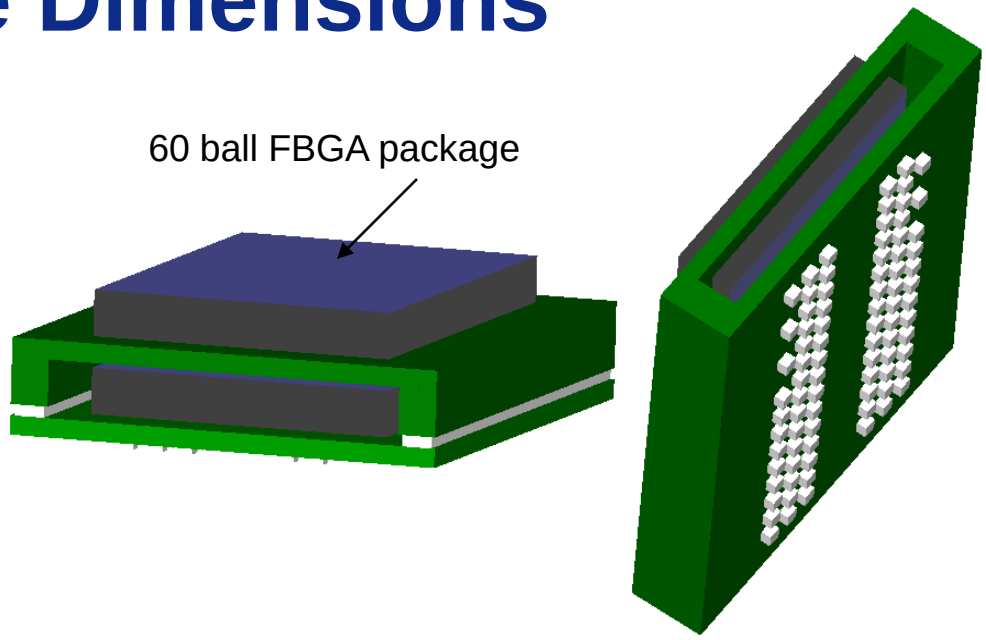
Jedec Board Stackup

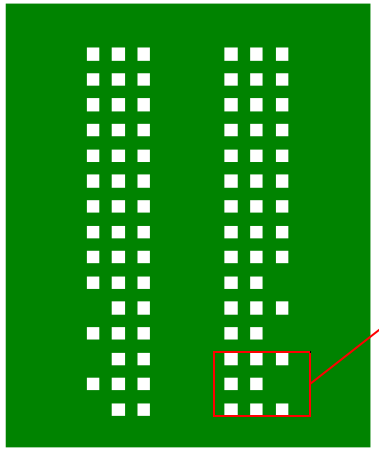
Trace	Thickness (oz)	% Cu
1	2	20
2	1	90
3	1	90
4	2	20

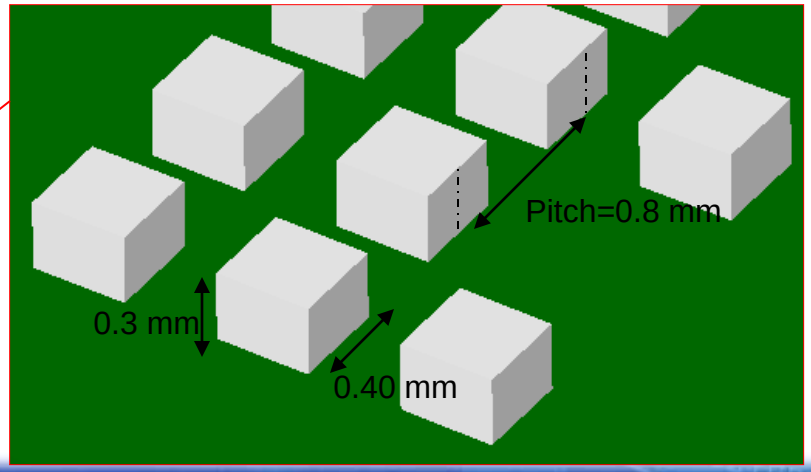


Package Dimensions

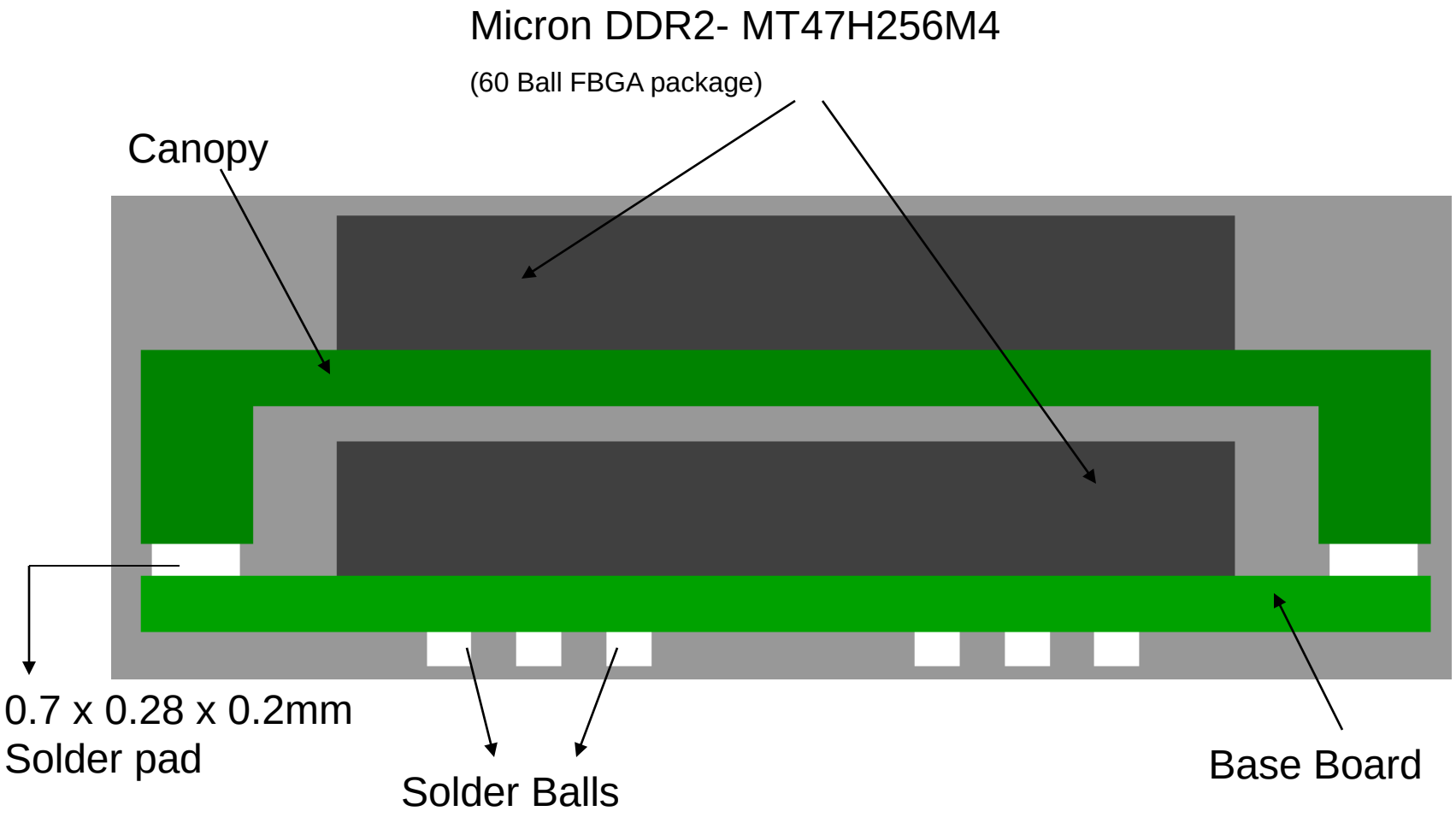






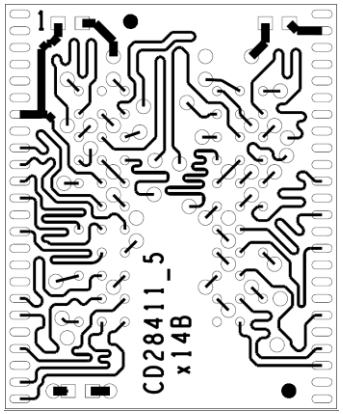


MDC22GCMG-67E0 Stackup

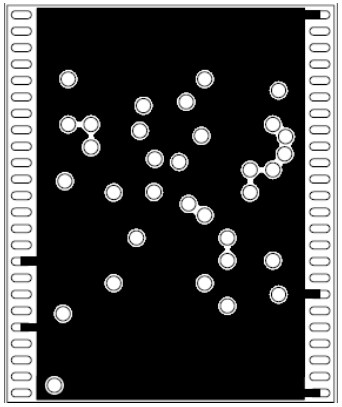


Base Board Layer Detail

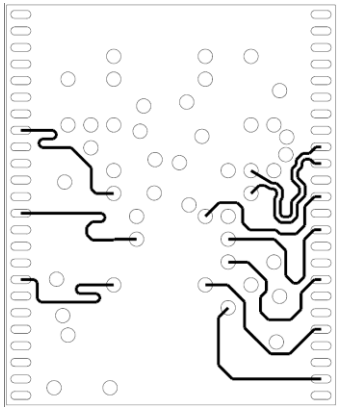
Layer	Type	Thickness (Oz)	Coverage (%)
1	Signal	1	17%
2	Ground	1	74%
3	Signal	1	6%
4	Signal	1	7%
5	Power	1	73%
6	Signal	1	16%



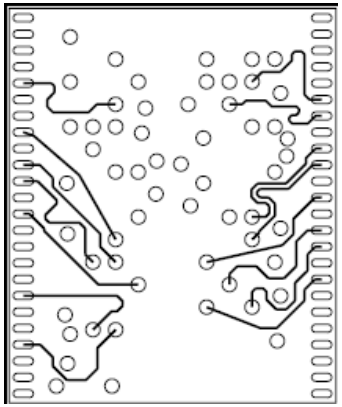
Layer 1



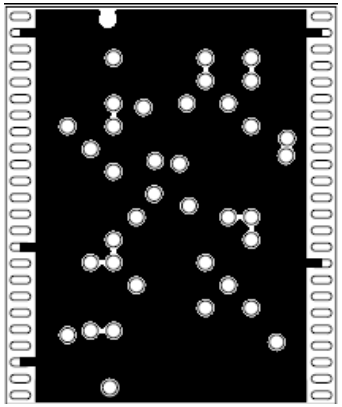
Layer 2



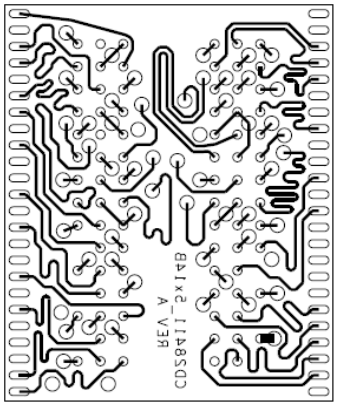
Layer 3



Layer 4



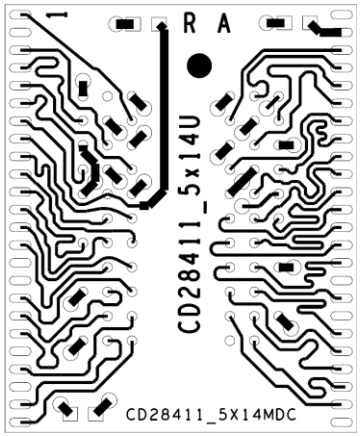
Layer 5



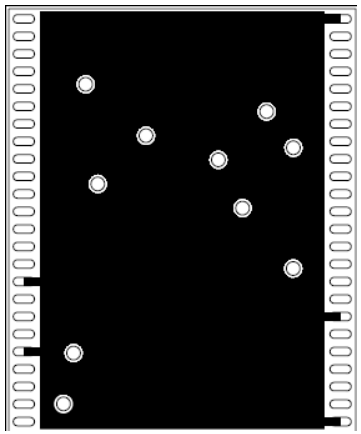
Layer 6

Canopy Layer Detail

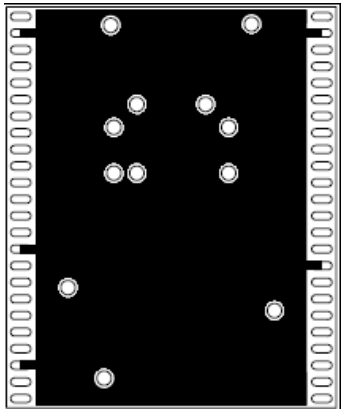
Layer	Type	Thickness (Oz)	Coverage (%)
1	Signal	1	20%
2	Ground	1	80%
3	Power	1	79%
4	Signal	1	1%



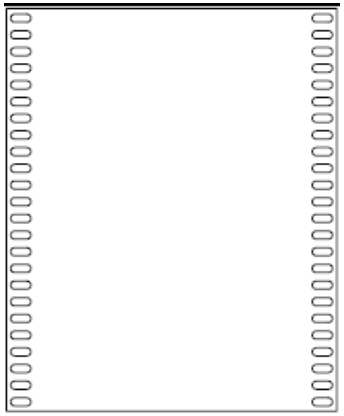
Layer 1



Layer 2



Layer 3



Layer 4

Material Properties

	Material	Conductivity (W/mK)
Prepreg	FR4	0.3
Traces	Cu	384
Solder	Solder (Sn96.5% and Ag3.5 %)	78.4

- The in-plane conductivities of layers are calculated as average of Cu and FR4 depending on % coverage.
- The Solder properties were obtained from FloTHERM Library with 96.5% Sn and 3.5% Ag.

Via and Solder Pad Details

- Similar to the layer definition seen in slides 6 and 7, the vias and canopy solder pads are modeled as rectangular blocks with volume weighted thermal conductivity.
- A summary of the thermal conductivities are seen below.
- Detailed calculations are available upon request

Rail Vias			
outline area	14	mm^2	
# of vias	24		
area of vias	0.75	mm^2	5%
area of FR4	13.25	mm^2	95%
k_effective	**7.76**	**W/mK**	

Lower Board Top-L3			
outline area	161	mm^2	
# of vias	48		
area of vias	1.51	mm^2	1%
area of FR4	159.49	mm^2	99%
k_effective	**1.60**	**W/mK**	

Lower Board L4-Bottom			
outline area	161	mm^2	
# of vias	58		
area of vias	1.82	mm^2	1%
area of FR4	159.18	mm^2	99%
k_effective	**1.97**	**W/mK**	

Solder Pads			
outline area	9.8	mm^2	
solderball area	0.18	mm^2	
# of solderballs	24		
total solder area	4.30	mm^2	44%
area of air	5.50	mm^2	56%
k_effective	**34.42**	**W/mK**	

Canopy L3-Bottom			
outline area	161	mm^2	
# of vias	58		
area of vias	1.82	mm^2	1%
area of FR4	159.18	mm^2	99%
k_effective	**1.87**	**W/mK**	

Canopy Top-L3			
outline area	161	mm^2	
# of vias	34		
area of vias	1.07	mm^2	1%
area of FR4	159.93	mm^2	99%
k_effective	**1.22**	**W/mK**	

DDR2: 2-Resistor model

- The DRAM's are modeled as a two resistor compact thermal models. The values for Junction-to-Board thermal resistance (Θ JB) and Junction-to-Case thermal resistance (Θ JC) were extracted from Micron Data Sheet.

Table 7: Thermal Impedance

Die Revision	Package	Substrate	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JC (°C/W)
E[1]	60-ball	2-layer	56.7	42.1	36.8	22.7	2.5
		4-layer	40.2	32.8	29.9	22.1	

Operating Temperature Limits

- According to the datasheet published by the DRAM manufacturer (Micron) the maximum DRAM operating temperatures are:
  - Commercial Temperature (IT):
    - 0°C <Tcase <85°C

Results

Component Temperature Summary

DRAM	Tcase_predicted (°C)	*Tcase_max (°C)	Margin (°C)
top	**51.4**	85	33.6
bottom	**46.5**	85	38.5

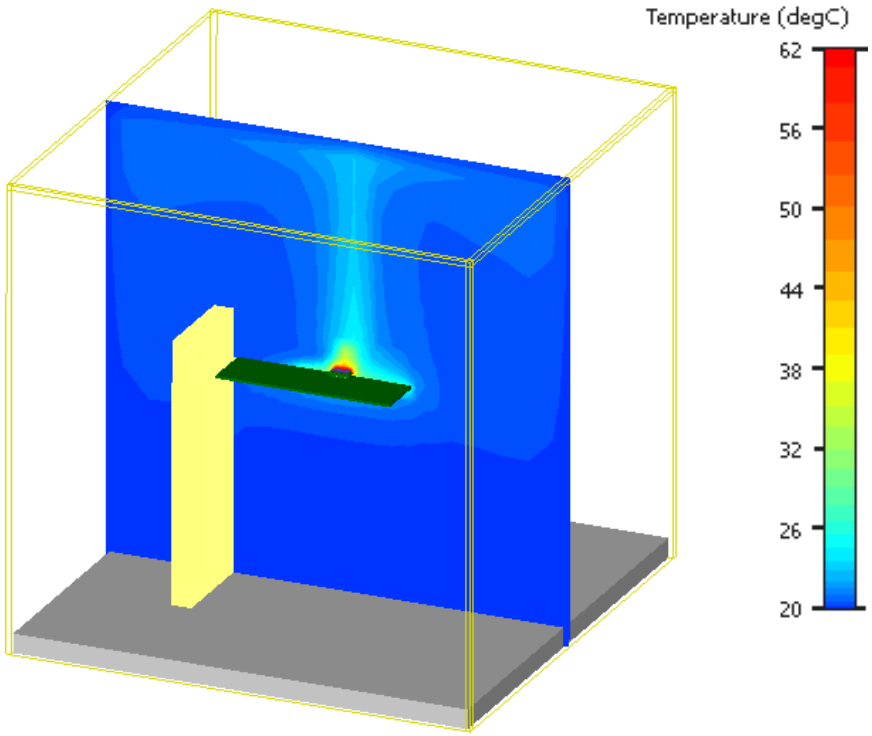
* max junction temperature from Micron datasheet

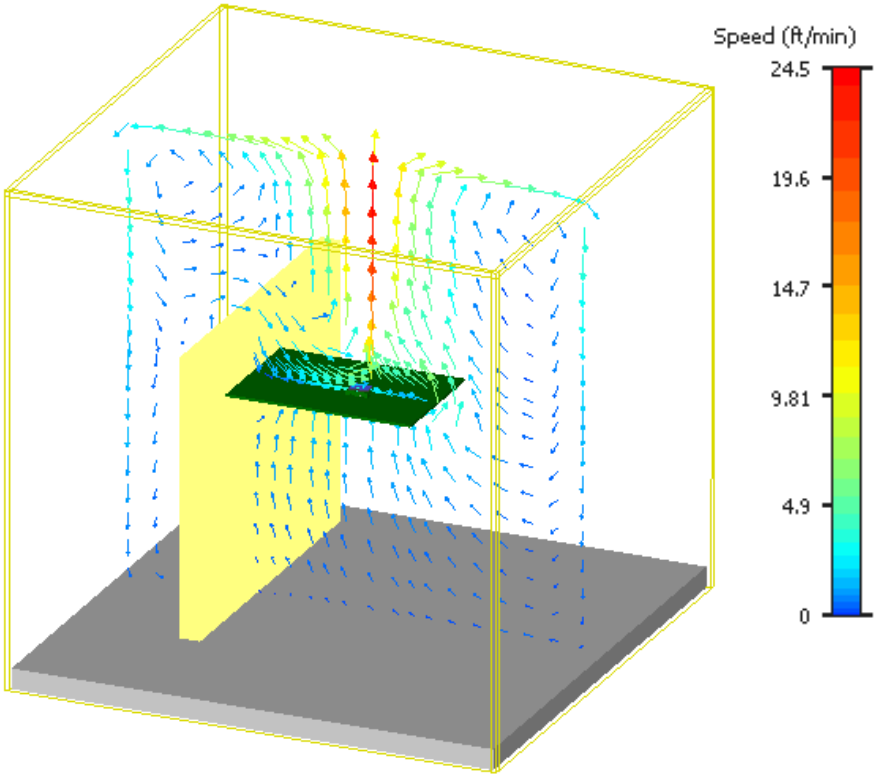
DRAM	Tj_predicted (°C)	Tamb (°C)	Heat Diss (W)	Θja* (°C/W)
top	51.4	20.0	0.36	87.3
bottom	46.5	20.0	0.36	73.7

* Junction-to-Ambient thermal resistance

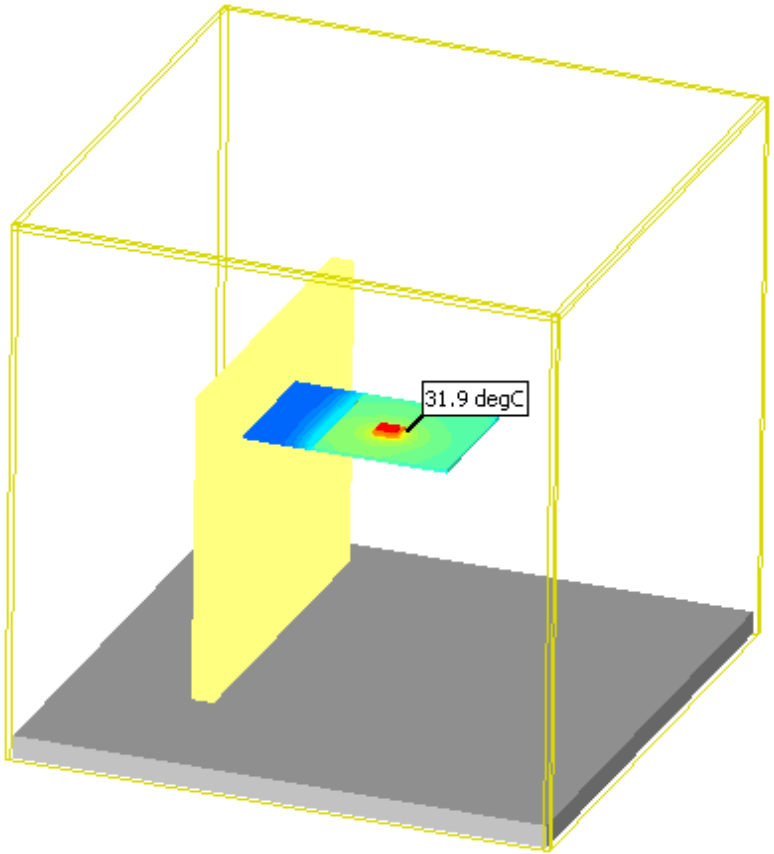
Air Temperature and Speed

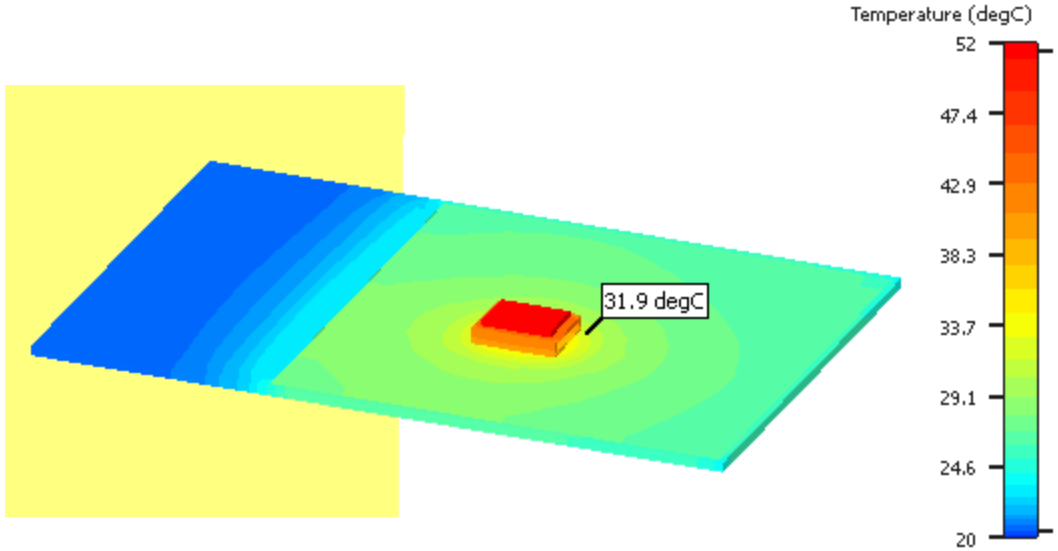
- Cutplane taken through centerline of the package



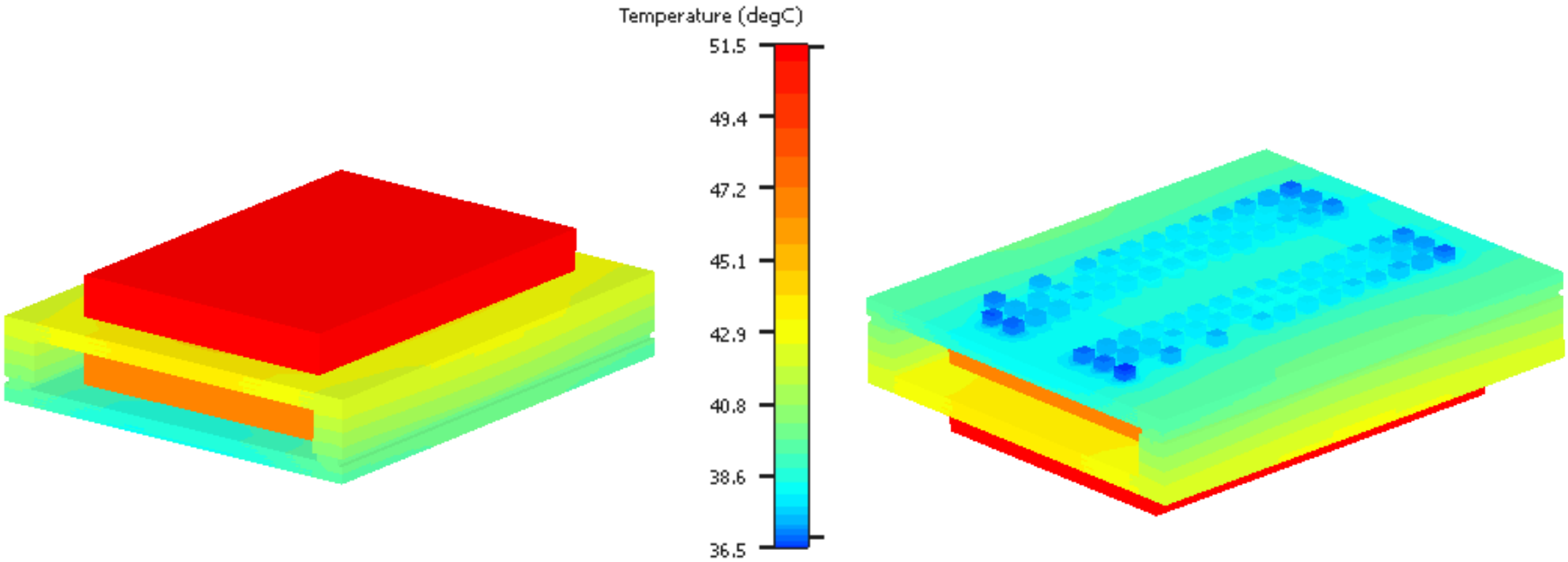


Host Board Surface Temperature





Component Surface Temperature



Summary

- A Computational Fluid Dynamics, FloTHERM® model of Legacy Electronics' **MDC22GCMG-67E0 multiple device canopy** has been created. The device has been equipped with 2 Micron DDR2-MT47H256M4 memory chips, and simulated in a JEDEC JESD51-2A Still-Air test environment.

- The predicted case temperature of the memory chips are:
  - Top DRAM – 51.4 °C; 33.6 °C below the maximum operating temperature
  - Bottom DRAM – 46.5 °C; 38.5 °C below the maximum operating temperature

- The junction-to-ambient thermal resistance of the hottest DRAM is predicted to be ~ 87.3 °C/W