APPLICATION NOTE

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Coordinated Circuit Protection for USB Applications

Introduction

The Universal Serial Bus (USB) protocol has evolved into the near de facto standard for all types of port-to-port connections, from personal computing devices to the newest generation of mobile devices, including ultra-thin smartphones and tablets. From its inception, the USB 1.1 interface replaced legacy port connectors and simplified the process of plug and play.

In 2000, USB 2.0 entered the market with a new High-Speed (HS) mode that served up to 480Mbit/sec, at the same time remaining backward-compatible with the Low-Speed (LS) and Full-Speed (FS) modes of USB 1.1. By 2008, three billion units of new electronic equipment with USB 2.0 interfaces had entered the market.

In 2008 the USB 3.0 specification was released. This version offered full USB 2.0 functionality (HS, FS, LS), plus a new and separate ultra-high-speed data link called SuperSpeed. It is estimated that in 2013 more than four billion pieces of new equipment offer a USB interface.

Although, the improved data rate, current and power delivery capability of USB 3.0 means faster system performance, it also intensifies the need for new and more robust circuit protection solutions for USB applications. This paper gives an overview of USB 3.0 requirements and presents typical circuit protection solutions for USB applications. This includes a coordinated circuit protection approach that can help protect USB 3.0 applications from potential damage caused by overcurrent, overvoltage and electrostatic discharge (ESD) transients. It also describes low-capacitance SESD (silicon ESD) protection devices, which can help minimize the impacts to system performance that can result from adding circuit protect devices to these high-speed data lines.

USB 3.0 vs. 2.0 Requirements

The USB 3.0 protocol provides data transfer rates almost ten times higher than the previous-generation USB 2.0 version (5Gb/s vs. 480Mb/s), as well as increases power delivery capabilities by 80% (from 500mA to 900mA). It also includes new power management features and new cables and connectors that are backward-compatible with USB 2.0 devices.

USB 3.0 provides power over two components: a standard host (A-type connector) and a new type of powering device (Powered-B connector). A Powered-B connector allows one USB device to charge another device by supplying current up to 1.0A. Since overcurrent conditions can affect the power bus, overcurrent protection is necessary on all power sources (i.e., hosts, hubs and Powered-B devices). Overcurrent protection is also required per UL60950.

Similar to USB 2.0, all types of USB 3.0 hosts must provide power. A single-unit load for USB 3.0 is redefined to be 150mA, an increase from 100mA in USB 2.0. A USB 3.0 host must be able to support up to six units (900mA) per port. In addition, USB 3.0 hubs may no longer be bus powered. All USB 3.0 hubs must be capable of supporting up to 900mA per port.

Additionally, higher-current-capable overcurrent protection devices are required for systems that support USB charging and USB 3.0. The USB charger specification utilizes the same pin-outs as USB 2.0, but allows for even higher current capability (up to 1.5A per port).

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Finally, USB 3.0 defines a Powered-B connector whose principal benefit is enhanced portability. The Powered-B connector allows for the elimination of USB cables and extra power supplies. Using a Powered-B connector, a USB device can now power another USB device. By providing two extra contacts, the new connector enables a power supplier (with a Powered-B receptacle) to provide up to 5V +/-10%, 1000mA of current to another device (with a Powered-B plug). For example, a printer can power up a wireless adapter, thus eliminating the need for a wired USB connection.

Overcurrent Protection

PolySwitch PPTC Devices

PolySwitch PPTC (polymeric positive temperature coefficient) devices provide a cost-effective solution for USB overcurrent protection in USB 3.0 applications. These devices can be used for current limiting in USB 3.0 host applications, USB 3.0 hub applications, USB charging applications and USB 3.0 Powered-B applications.

As shown in Figure 1, installing a PolySwitch PPTC device on the VBUS port of a USB power source limits the current in the event of a short circuit, prevents overcurrent damage caused by a sudden short circuit downstream, and helps achieve UL60950 compliance.

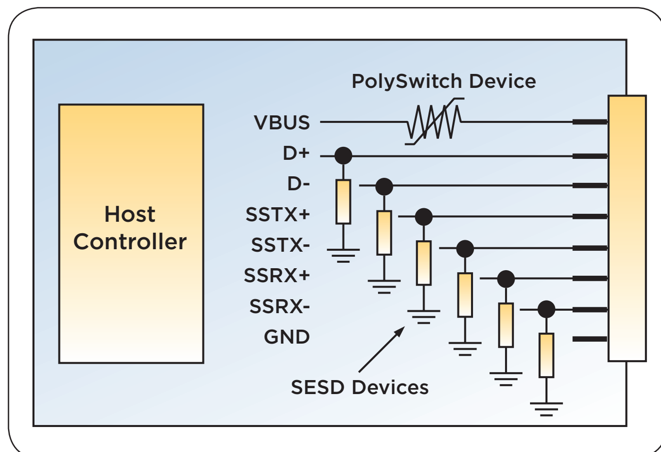

Figure 1. A PolySwitch PPTC device can be installed on the VBUS for host-side USB protection.

Overvoltage Protection

PolyZen Devices

Placing the PolyZen device on the power inputs of all USB-powered devices can help protect against damage caused by overvoltage events (Figure 2). PolyZen technology integrates into a single device a precision Zener diode and a PolySwitch PPTC device, which are thermally bonded. The PolyZen device can be installed on the VBUS of the USB input port, the DPWR port of Powered-B plugs and the barrel jack power port, and VBUS input of USB hub devices.

It should be noted that USB 3.0 will not support bus-powered hubs and will only support self-powered hubs. A power source is now needed to power-up all ports of the hub in USB 3.0 applications. If a DC power connector is used at the input to the hub, a circuit protection device may be warranted to help protect the hub electronics from damage caused by overvoltage events or from an unregulated or incorrect supply, reverse voltage or voltage transients.

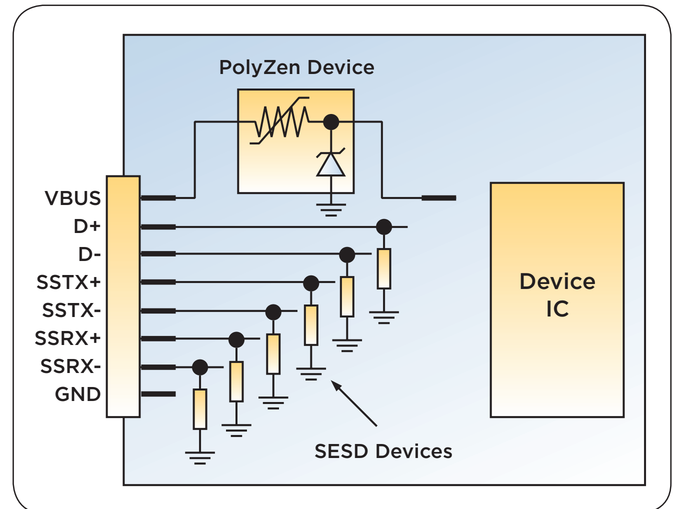

Figure 2. A PolyZen device can be installed on the VBUS for device-side USB protection.

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ESD Protection Requirements

The result of an imbalance of electrons between two objects separated by a dielectric is static electricity. This type of electrostatic discharge, or ESD, is a well-known phenomenon that can cause various types of failures in electronic systems. System failures can be generally classified into two categories: soft failures (i.e., system upsets) and hard failures (i.e., catastrophic damage to a component of the system). ESD design considerations include:

- Compliance with country-specific government regulations and to improve product reliability.
- Although modern integrated circuits (ICs) often have some degree of protection (typically between 500V and 2kV), ESD levels are based on the MIL-STD HBM model with 1500Ω of resistance. With the MIL-STD model, 2kV is more similar to the IEC model at 500V, which uses the 330-Ω resistor.
- USB 2.0 defines a transfer rate of 480Mb/sec and USB 3.0 defines a transfer rate of 5Gbit/sec, resulting in a fundamental frequency of up to 240MHz and 2.5GHz, respectively. For high signal integrity, rise and fall time of the data signal must be very fast. The 3rd, or even 5th, harmonic must be handled without significant attenuation. This can be achieved only by a state-of-the-art semiconductor process using the lowest possible parasitic effects and fastest semiconductor switching times. The drawback of miniaturized semiconductor structures is the weakness of overvoltage caused by an ESD strike. Adding internal ESD protection can cause parasitic effects (parasitic capacitance) and can result in space and cost issues.

SESD Devices

A very cost-effective solution for ESD protection in USB 2.0/3.0 applications is to combine an internal ESD protection structure (integrated in the USB transceiver) with a robust, high-current application circuit that is tailored for external ESD protection. This is implemented by the device/circuit designer on the PCB. The internal ESD protection structure is designed to provide device-level protection, according to the HBM JEDEC JESD 22-A115 specification only, which is important for device-handling during development, production and board assembly. More stringent system-level protection, according to the IEC61000-4-2 specification, can be achieved by an external diode tailored to the application.

To achieve a proper system-level ESD protection for USB applications, the ESD protection device must fulfill several different requirements. The ESD performance of a transient voltage suppression (TVS) diode can be ascertained first by the residual clamping voltage and then by the TVS diode response in the case of a dedicated ESD strike, according to IEC61000-4-2.

ESD-protection components are placed on lines that are connected to system I/O connectors, which are usually the ESD entry points. ESD protection components block and divert the ESD current and clamp the ESD voltage to protect the connected ICs.

Careful design and placement of ESD protection can not only prevent hard failures, but as a secondary effect they can also help limit the number of soft failures by reducing ESD field coupling as the current is diverted away from sensitive circuits.

SESD devices can be placed at the USB power source in USB designs (Figure 3). The SESD series includes 0402- and 0201- sized devices that have industry-leading, ultra-low capacitance of 0.10pF for bi-directional devices and 0.20pF for uni-directional devices. They also exhibit low insertion loss that helps provide signal integrity for ultra-high-speed data signals. The single-channel SESD devices provide robust ESD protection with industry-best 20kV contact and air discharge rating per the IEC61000-4-2 standard.

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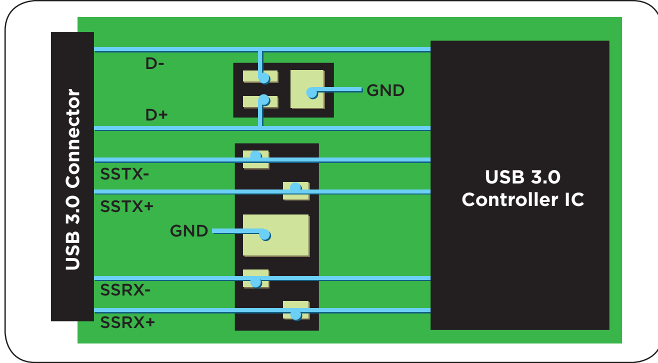

Figure 3. A 4- and 2-channel SESD array in a typical USB 3.0 circuit.

TVS Diodes

Transient Voltage Suppression, or TVS, components are often the preferred choice for ESD protection due to their current- and voltage-handling capabilities and their minimal loading on signals.

TVS diodes are used in parallel with the protected circuit. Under normal operating conditions, TVS diodes present high impedance to the protected circuit, but during an ESD event they can provide a low-impedance shunt path for the ESD current-to-ground. They can then return to their original high-impedance state as soon as the overvoltage condition is removed.

Figure 4 shows a typical ESD protection scheme in which a TVS device is used to protect an IC. When ESD reaches the protected line, the TVS diode triggers and clamps the voltage to its clamping voltage (V_{CL}) and diverts most of the internal ESD current (I_{ESD}) to ground. However, some portion of the current continues to flow into the protected IC. This is called the residual current (I_R). V_{CL} and I_R, as related to the input impedance of the IC, determine the stress seen by the IC.

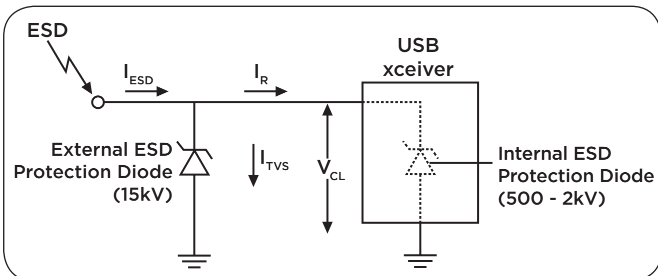

Figure 4. Typical ESD protection scheme.

ESD Protection Parameters

Figure 5 provides a characteristic waveform of a unidirectional ESD protection device.

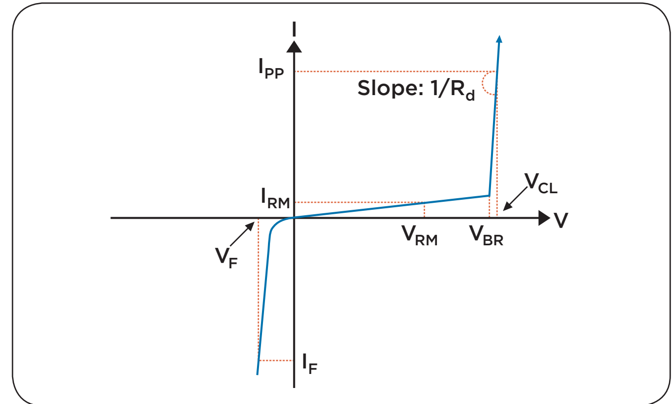

Figure 5. Voltage current characteristics of a TVS diode.

The following list provides details of ESD protection device parameters.

- V_F : Forward voltage drop across the ESD protection device
- V_{RM} : Maximum reverse working voltage of the diode
- V_{BR} : Breakdown voltage defined at I_R = -1mA
- V_{CL} : Clamping voltage
- I_{PP} : Maximum peak current
- R_{DYN} : Dynamic resistance

Important parameters to consider when designing ESD protection are covered in the following sections.

Clamping Voltage

When selecting an ESD protection device, designers should consider clamping voltage as one of the key parameters on the datasheet. During any ESD event, the protection device will clamp at its specified clamping voltage and shunt most of the peak pulse current (caused due to the event) to ground to protect the device IC from damage. Most of this clamping voltage is what the protected IC is exposed to. (Ideally this would be all of the voltage, considering there are no discrete elements or parasitic inductances or capacitances between the protection diode and the protected IC.)

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Even with most of the peak pulse current shunted to ground, residual current will still flow into the protected IC. Thus, the peak pulse during in an ESD event is a combination of the shunted current through the ESD protection device and the residual current flowing into the protected IC. As a result, more shunted current through the ESD device will mean less residual current in the protected IC. The power that the protected IC is exposed to during the ESD event depends upon the clamping voltage of the ESD protection device and the residual current.

Lower clamping voltage and lower residual current would therefore mean lower joule heating of the protected IC. Clamping voltage is usually determined by following equation:

$V_{CL} = V_{BR}$ + IResidual (Residual current through protected IC) * R_{DYN}

It is important for designers to note that every datasheet must be scrutinized thoroughly to understand the test methods used for determining the clamping voltage. It has become almost an industry standard to publish clamping voltage on the datasheet based on either an 8/20 microsecond surge or an 8kV ESD surge. The 8/20 microsecond surge has an 8 microsecond rise time (from 10% to 90% of its peak value), and a 20 microsecond decay time (to 50% of its peak value). An 8/20 microsecond surge current rating of 1A or higher is often published on datasheets.

An ESD pulse will have a rise time of less than 1nS and a duration of less than 100nS, with a peak current of 30A as designated in IEC 61000-4-2 level 4. The 8/20µS waveform is designated per IEC 61000-4-4 and is intended for high-power surge events such as inductive kick or lightning surges.

Therefore, an ESD protection diode that shows clamping a voltage of 9V at (8/20µS) may show a clamping voltage of more than 50V under ESD testing. With little knowledge of this fact a designer might end up selecting an ESD protection device by merely looking at the lowest clamping voltage value on the datasheet. So, when comparing different clamping voltages a designer must bear in mind which test setup was used to determine the value.

Signal Integrity

One of the biggest design challenges for ultra-high-speed data transmission systems is ensuring a certain level of signal integrity for a receiver. It is important to achieve a low bit error rate for high signal integrity (a bit error rate of 1E-12 is typical for USB 3.0 SuperSpeed). Signal integrity is characterized by the eye diagram.

In an ideal system without limitations in bandwidth the eye diagram would be completely open. In an actual system, the signal rise time/fall time is limited by the TX and the RX impedance (90Ω differential) in combination with all parasitic capacitance at TX side and RX side. These parasitic capacitances are inside the USB 3.0 transceiver and/or externally on the PCB.

External parasitics can be caused by unmatched PCB lines, the USB 3.0 connector or other shunt capacitors. Therefore it is mandatory to keep these additional shunt capacitors as small as possible. The low-pass frequency response of the USB 3.0 cable must be taken in to account as well. To compensate the attenuation of the high frequency content, the signal is tuned by a dedicated equalization on TX and on RX side.

Employing both of these measures can help speed up the signal at the rising and the falling edge, which results in a more open eye diagram (i.e., improved signal integrity).

For a proper signal integrity performance, the capacitance of the diodes must be very low and the diode must provide a high level of ESD protection.

Eye Diagrams

It is commonly understood when viewing eye diagrams that a great deal can be easily inferred about the degradation ESD protection devices are causing to the electrical quality of a high-speed digital signal. However, for a subset of a data channel, namely the contributions to degradation from a passive TVS device, this “great deal” of information may be helpful, meaningless or even misleading.

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An eye diagram is produced by repetitively sampling a digital signal on an oscilloscope's vertical axis while triggering the horizontal sweep with the data rate. The resulting pattern looks like an eye. The larger the eye the better the data signal integrity. The excellent eye diagram performance of the 0.2pF SESD array device operating at 2.5GHz is shown in Figure 6.

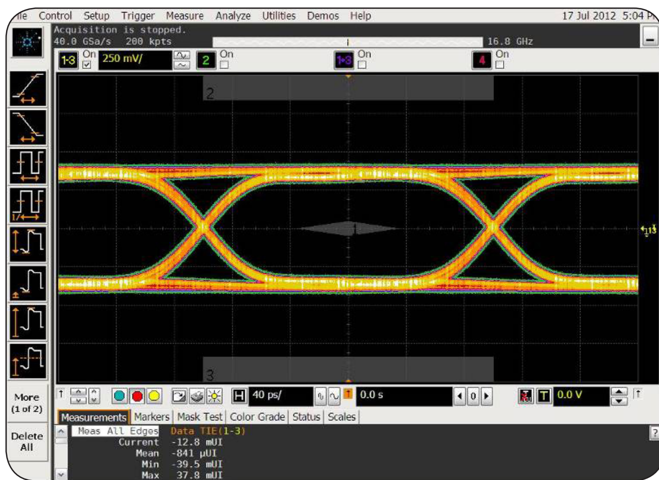

Figure 6. Eye pattern of TE's SESD10004Q4UG-0020-090 4-channel array for USB 3.0.

Insertion Loss

Unlike an eye diagram, the insertion loss plot is created by reference Network Analyzer test equipment rather than an arbitrary PHY (chipset). A reference test board must be used that has dedicated launches (such as coaxial RF SMA connectors) for input and output. It is extremely difficult to achieve this in an actual system board terminated by a PHY on one end and a USB connector on the other, so these measurements are done by TVS vendors on a reference fixture or evaluation PCB, resulting in the different perspective for eye diagrams and insertion loss plots.

The eye diagram is an extraordinary combination of active deviations, passive parasitics and dynamic effects for an entire data channel, end-to-end. For selection of a single passive component within that channel, insertion loss characterization reveals the primary relevant contributions of parasitic effects on the channel for that device.

For a first-pass evaluation of a TVS device, an insertion loss plot showing <0.5dB at 2.5GHz is an excellent indicator of suitability for use in a USB 3.0 system. Discerning designers will pursue this further with more details on differential insertion loss, crosstalk and other metrics specific to their particular implementation environment.

Insertion loss plots suggest at an instant the passive and reciprocal effect of the device on signals at all frequencies of interest. If an insertion loss plot shows -6dB at a given frequency, then any signal at that frequency sent through that channel will appear on the other end at about half its original level.

The graph in Figure 7 shows insertion loss for 0.2 pf SESD uni-directional and 0.1pF SESD bi-directional devices. As shown, the insertion loss is negligible at 2.5GHz.

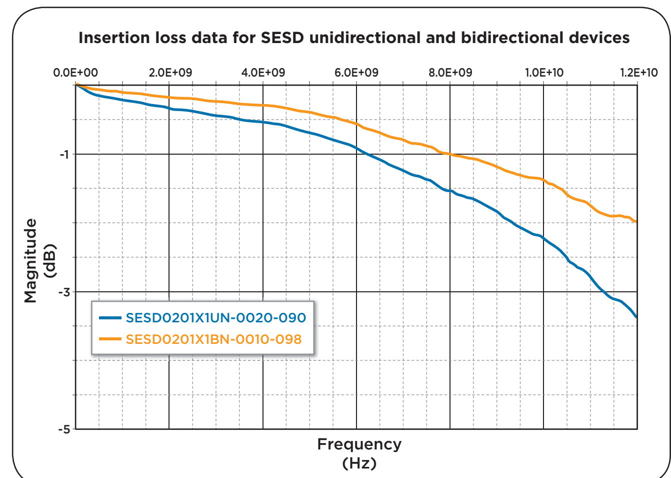

Figure 7. Insertion loss data for SESD unidirectional and bidirectional devices.

Coordinated Circuit Protection

A coordinated protection scheme can be used to help enhance protection against high-current, high-voltage and ESD transients in USB applications. Figures 8a and 8b illustrate the circuit protection devices that are suitable for USB 2.0 and USB 3.0 connector designs.

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In Littelfuse's approach to a coordinated design, PolySwitch PPTC overcurrent protection devices help designers meet the new high-current requirements of the USB 3.0 specification while offering a simple, space-saving solution. For overvoltage protection, PolyZen devices offer the simplicity of a traditional clamping diode while helping to eliminate the need for significant heat sinking. And for ESD protection, SESD devices help provide ultra-low capacitance (0.10pF and 0.20pF) required for high-speed data transmission applications and are available in the industry's smallest form factors.

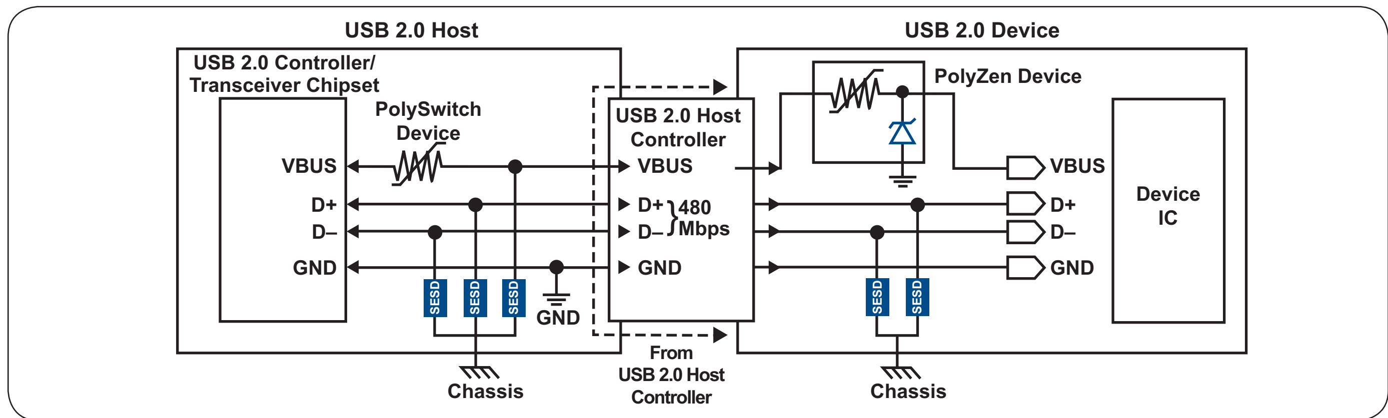

Figure 8a. Littelfuse's coordinated protection approach for USB 2.0.

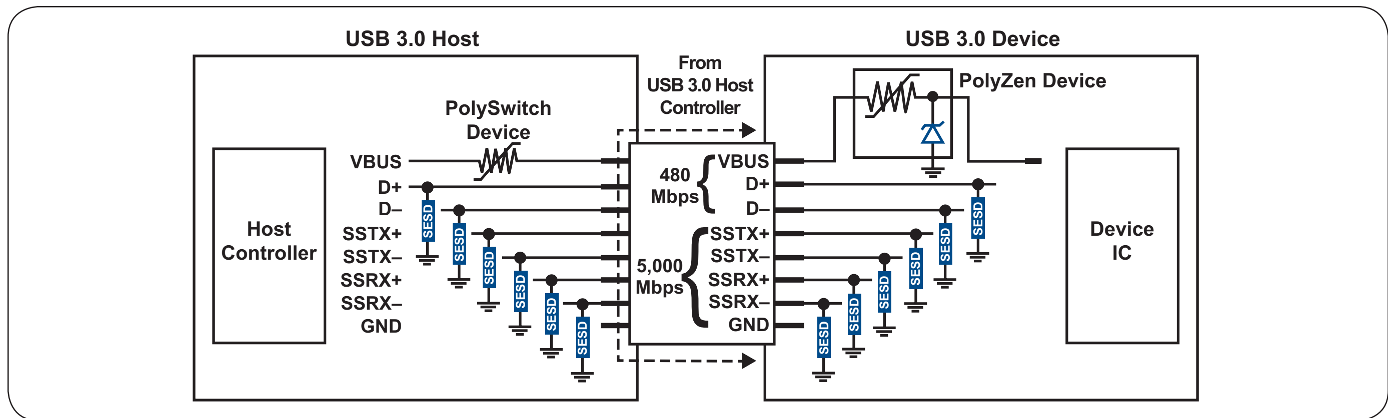

Figure 8b. Littelfuse's coordinated circuit protection approach for USB 3.0.

Summary

Littelfuse offers a coordinated circuit protection in USB applications that can help designers meet stringent protection requirements. In addition to offering PolySwitch overcurrent and PolyZen overvoltage protection devices, the company's SESD devices provide robust performance in USB designs by providing very low clamping voltage and lower dynamic resistance than similar solutions. The eye diagrams and insertion loss resulting from SESD device testing demonstrate their extremely low impact on logic levels and negligible signal-distortion impact, which is a major consideration in sensitive electronics. With industry-leading ultra-low capacitance, SESD devices can help design engineers optimize their design, board space while also helping to minimize design risks.

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Device Recommendations

Littelfuse recommends the following circuit protection devices for USB protection (Table 1 and Table 2).

		Recommended Parts Ganged Ports per PolySwitch Device			
USB Host Protocol	Max allowed current per port	1	2	3	4
USB 1.0 or 2.0	0.5A	nanoSMDC075F	miniSMDC160F	miniSMDC200F	miniSMDC260F
USB 3.0	0.9A	nanoSMDC150F	miniSMDC260F	N/A	N/A
USB Charging Enabled Port	1.5A	miniSMDC260F	N/A	N/A	N/A

Littelfuse recommends placing overvoltage protection devices on all USB-powered equipment, specifically on the VBUS port, as shown in the following table.

USB VBUS Overvoltage Protection Recommendations			
USB 2.0	USB 3.0	USB Charging	Notes
PolyZen Device ZEN056V130A24LS	PolyZen Device ZEN056V130A24LS	PolyZen Device ZEN056V230A24LS	Lower Voltage Clamping
PolyZen Device ZEN059V130A24LS	PolyZen Device ZEN059V130A24LS	NA	Lower Voltage and Low Power Consumption in Suspend Mode
PolyZen Device ZEN065V130A24LS	PolyZen Device ZEN065V130A24LS	PolyZen Device ZEN065V230A16LS	Lower Leakage Current

Table 1. Recommended PolySwitch and PolyZen devices for USB protection.

	Silicon ESD Packages							
	0402 1-Ch Bi-Di	0402 1-Ch Uni-Di	0201 1-Ch Bi-Di	0201 1-Ch Uni-Di	0402 2-Ch Flow-Through	2-Ch Flow-Through Array	4-Ch Flow-Through Mini-Array	6-Ch Flow-Through Array
Dimensions (mm)	1.0 x 0.6 x 0.38	1.0 x 0.6 x 0.38	0.6 x 0.3 x 0.31	0.6 x 0.3 x 0.31	1.0 x 0.6 x 0.38	2.5 x 1.0 x 0.38 (0.5mm pitch)	2.0 x 0.6 x 0.38 (0.4mm pitch)	2.8 x 0.8 x 0.38 (0.4mm pitch)
Technology	SESD (Bi-Di)	SESD (Uni-Di)	SESD (Bi-Di)	SESD (Uni-Di)				
pF / kV contact	0.10pF / 20kV	0.20pF / 20kV	0.10pF / 20kV	0.20pF / 20kV				
IEEE61000-4-5 8/20µS Lightning	2Amp							
Leakage Current	50 nanoAmp (Typ)							
Applications	Ultra-High-Speed Digital (HDMI 3.0, Thunderbolt, DisplayPort, V-by-One HS, LVDS)							
Production	Yes							
	Single-Channel Protection				2-Channel	4-Channel	6-Channel	

Table 2. Recommended SESD devices for USB protection.

Notice:

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