XYlon

logi3D Scalable 3D Graphics Accelerator

for

Xilinx Zynq-7000 EPP and FPGAs

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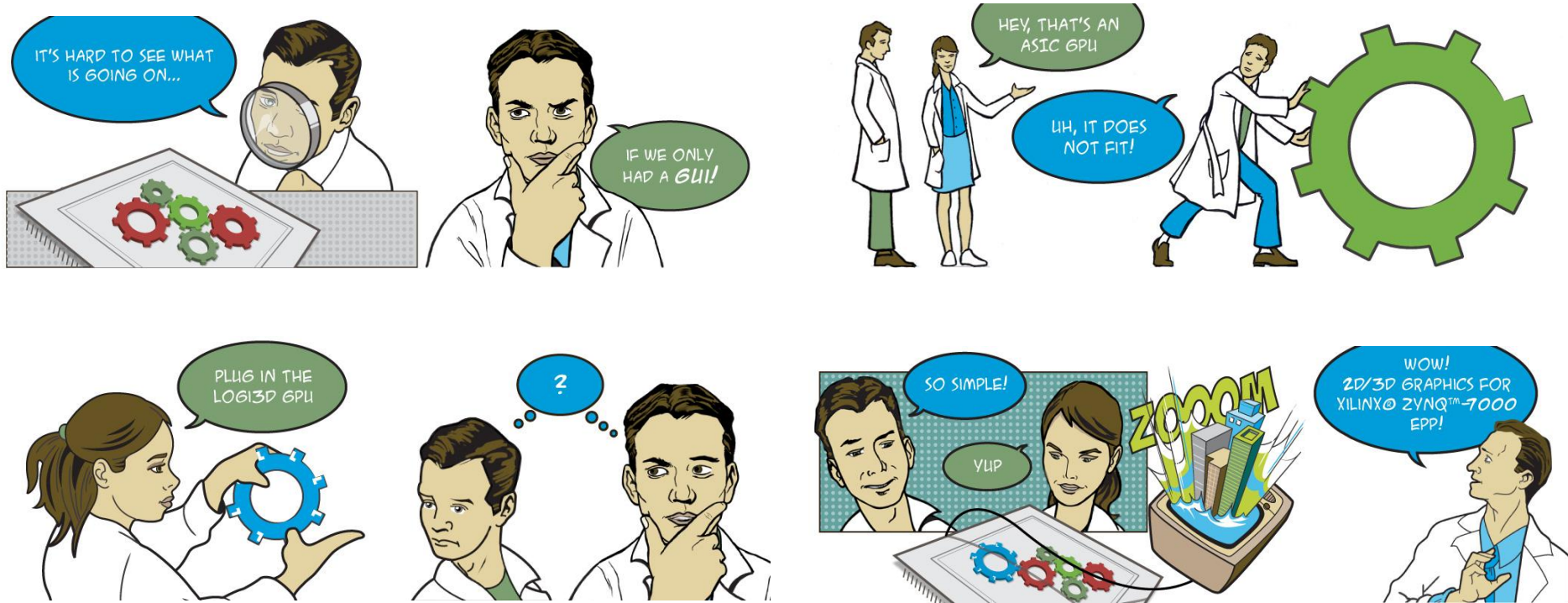
The logi3D Scalable 3D Graphics Accelerator is the World's first GPU IP core designed specifically for the Xilinx® ZynqTM-7000 EPP. It upgrades Xylon's product line of 2D graphics accelerator IP cores for Xilinx programmable devices.

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logi3D Scalable 3D Graphics Accelerator IP Core
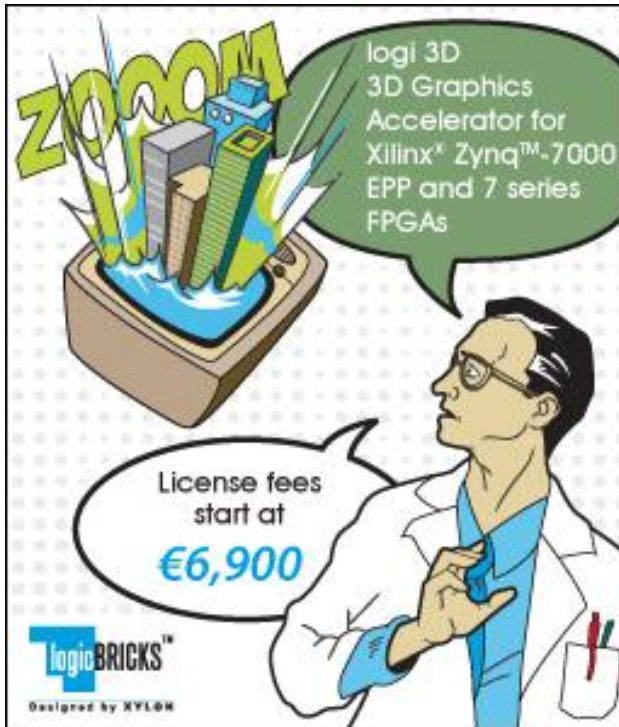
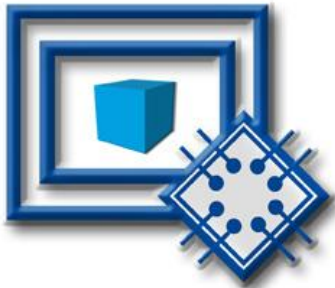

- ❑ 3D graphics accelerator designed from ground up for the Xilinx Zynq-7000 Extensible Processing Platform (EPP)

- ❑ Supports the OpenGL ES® 1.1 API*

- ❑ AMBA® AXI4 compliant plug-and-play IP core

- ❑ Currently supported OS is Linux, with support for other OSes planned for year 2012

- ❑ Can be used with different Xilinx FPGAs (7 Series, Spartan®-6, ...) in various ASSP+FPGA combinations

*Product is based on a published Khronos specification, and is expected to pass the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

Applications

- ❑ The logi3D IP core can be used as a Graphics Processing Unit (GPU) in major graphics applications, including scalable user interfaces, visualizations, navigation, automotive, defense systems, etc.

- ❑ It targets full System On Chip (SoC) Xilinx Zynq-7000 EPP based solutions which:

  - ❑ Leverage ARM® dual-core Cortex™-A9 MPCore™ processing system
  - ❑ Implement your own proprietary IP cores in the programmable logic, and
  - ❑ Use Graphics User Interface (GUI) controlled by Xylon logi3D based 3D GPU!

*Screenshots from Xylon's log3D demo system*

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logi3D IP Core – Key Features

❑ Graphics accelerator designed to support OpenGL ES 1.1 API

❑ Enables 3D graphics on Xilinx Zynq-7000 EPP, 7 series, Spartan-6 and Virtex®-6 FPGAs

❑ Conforms to the AMBA AXI4 interface protocol

❑ FPGA resource-effective 3D graphics acceleration

❑ Geometry engine implemented in software saves programmable logic resources

❑ Rasterizer and post-filtering fully implemented in programmable logic

❑ Assembly code acceleration of geometry engine available for ARM NEON™ coprocessor

❑ Currently supported OS is Linux, with support for other OSes planned for year 2012

❑ Compatible with Xilinx implementation tools – simple plug-and-play
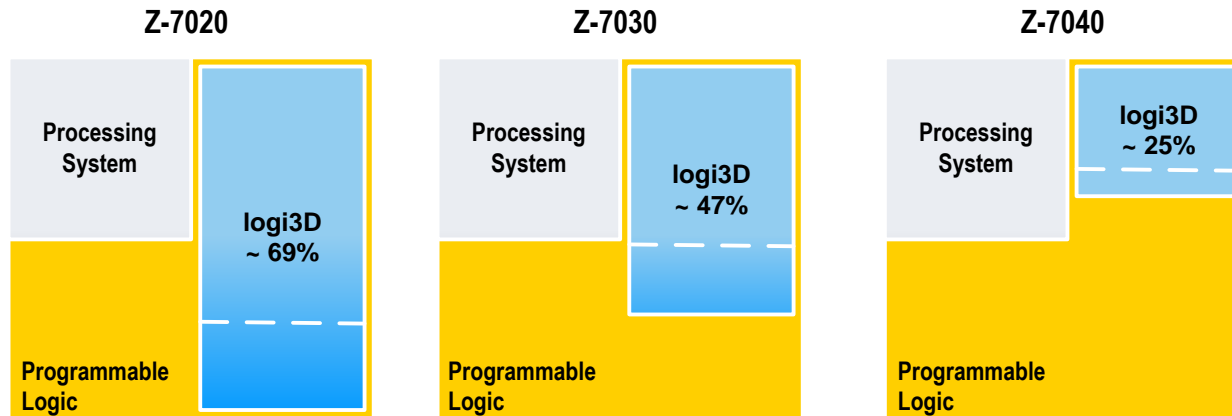
❑ Supported resolutions – up to 2048x2048 or higher

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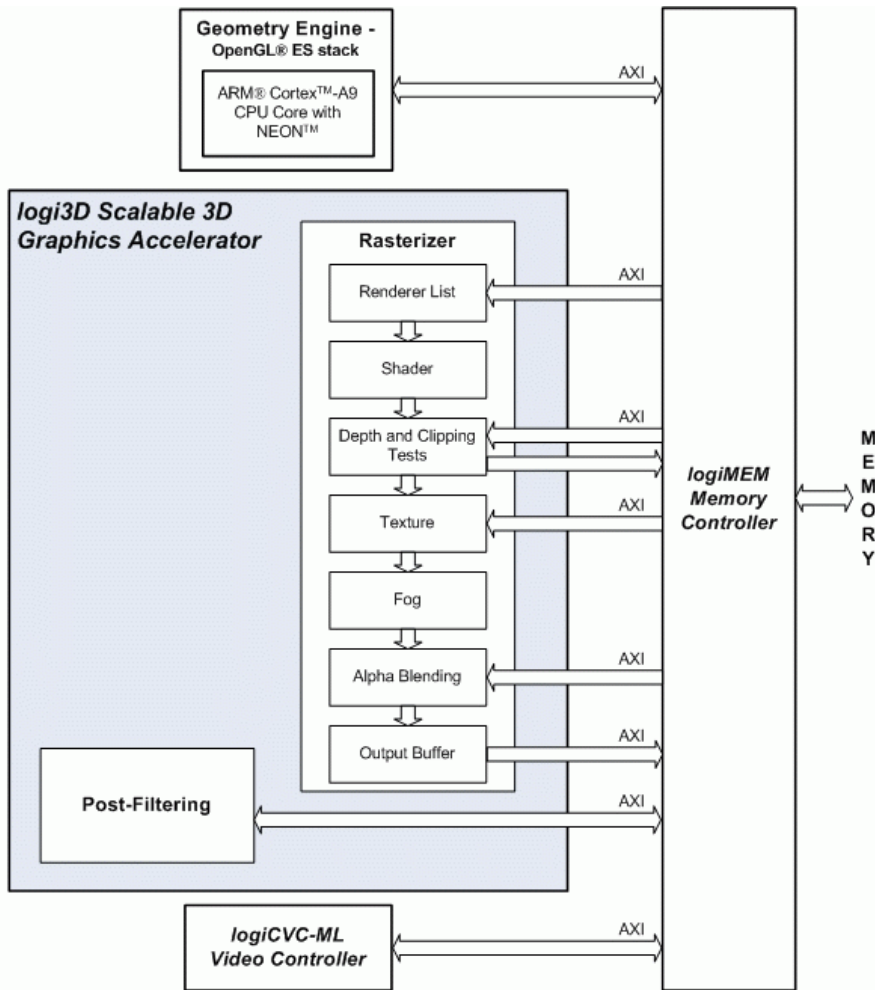
❑ The logi3D IP core is carefully hardware/software partitioned to assure high graphics performance and optimal utilization of programmable logic

❑ Complex Geometry Engine is implemented in software running on a single ARM Cortex-A9. It can use the NEON coprocessor for additional performance speed up.

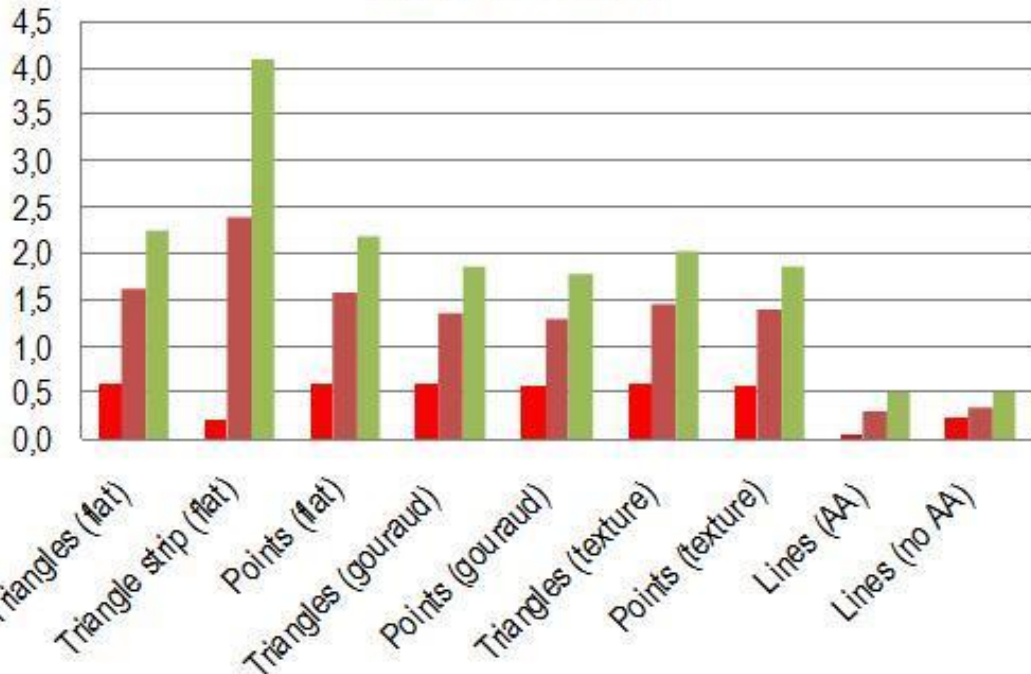❑ Rasterizer Engine works fully in the programmable logic

logi3D IP Core – Size

Z-7020

Processing System

logi3D ~ 69%

Programmable Logic

Z-7030

Processing System

logi3D ~ 47%

Programmable Logic

Z-7040

Processing System

logi3D ~ 25%

Programmable Logic

- ❑ The figure shows the estimated logi3D IP core's size in the Xilinx Zynq-7000 EPP programmable logic

- ❑ IP users can make further optimizations by switching off the unneeded IP core's functions

- ❑ The dotted line shows the logi3D IP core's size with the second Texture Unit switched off
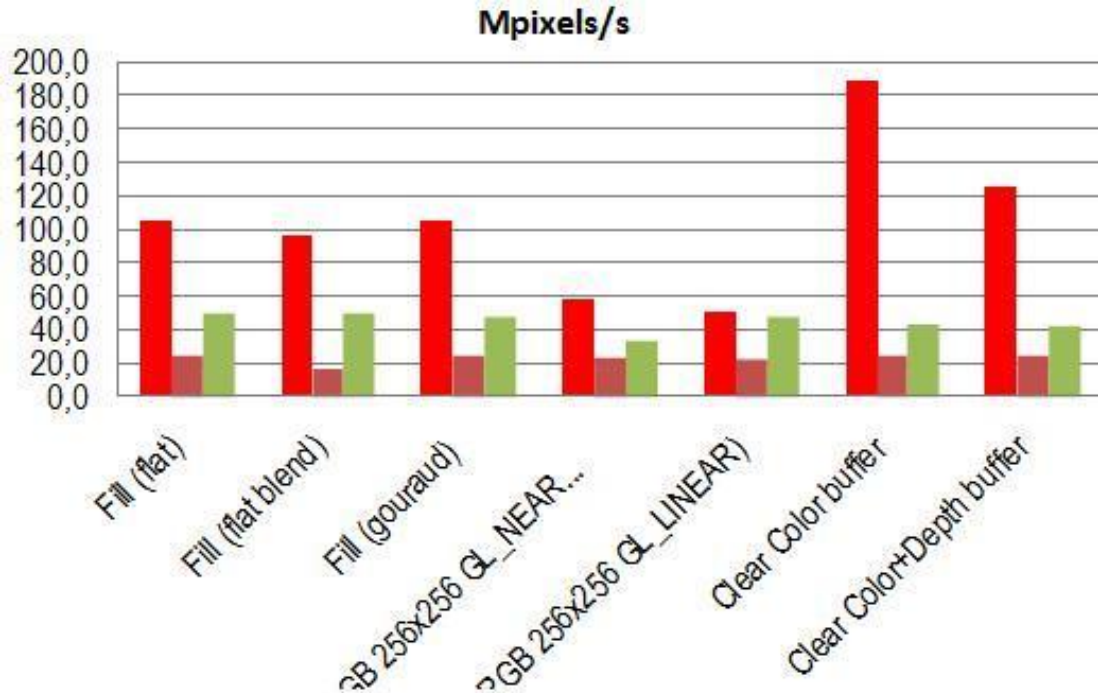
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MVertices-Lines/s

The estimate of logi3D Geometry Engine performance is based on measurements with Xylon logi3D development system: TI's OMAP3530 based kit + logiCRAFT-CC board with the Xilinx Spartan-6 FPGA

- Estimate for Xilinx® Zynq™-7000:
  ARM Cortex-A9 @667MHz, 2xDDR2@400MHz, logi3D @ 120MHz
- TI OMAP 3 : ARM Cortex-A8 @ 600MHz, PowerVR SGX530 @ 100MHz
- TI OMAP 3 : ARM Cortex-A8 @ 1GHz, PowerVR SGX530 @ 200MHz

❏ The chart shows that a software-based Geometry Engine cannot perform as well as full hardware implementations of graphics accelerators. However, it significantly saves the programmable logic resources and enable implementations of other IP cores alongside the logi3D in a single Zynq-7000 EPP device.

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logi3D IP Core – Rasterizer Engine Performance


Mpixels/s

The estimate of logi3D Rasterizer Engine performance is based on measurements with Xylon logi3D development system: TI's OMAP3530 based kit + logiCRAFT-CC board with the Xilinx Spartan-6 FPGA

Chart categories: Fill (flat), Fill (flat blend), Fill (gouraud), GB 256x256 GL_NEAR..., RGB 256x256 GL_LINEAR), Clear Color buffer, Clear Color+Depth buffer

Legend:
- **Estimate for Xilinx® Zynq™-7000:** ARM Cortex-A9 @667MHz, 2xDDR2@400MHz, logi3D @ 120MHz
- **TI OMAP 3 : ARM Cortex-A8 @ 600MHz, PowerVR SGX530 @ 100MHz**
- **TI OMAP 3 : ARM Cortex-A8 @ 1GHz, PowerVR SGX530 @ 200MHz**

❑ Xylon design team has had to design highly performing and hardware-based Rasterizer Engine in order to overcome the performance trade-off caused by decision to implement software-based Geometry Engine which saves the programmable logic resources

❑ The Rasterizer Engine performs very well and compensates for the lack of the Geometry Engine's performance

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logi3D IP Core – What's the Real Performance?
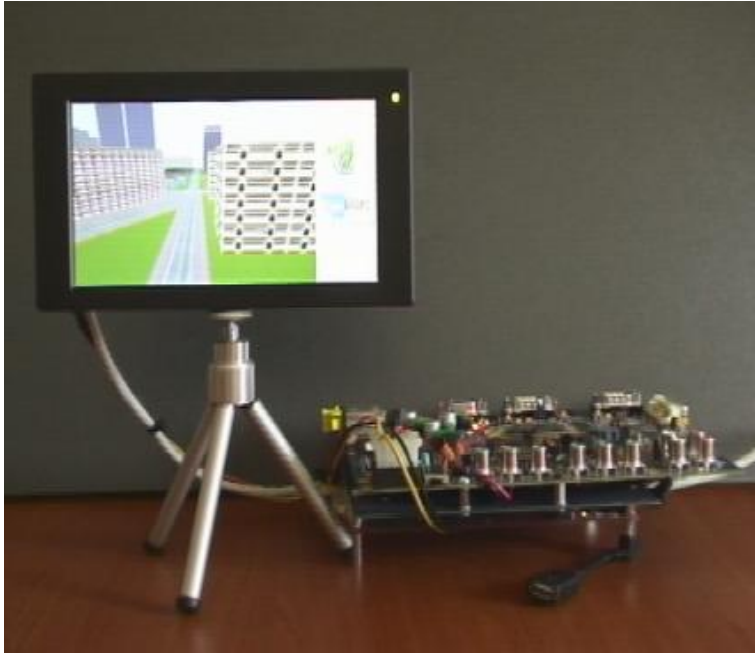
- ❏ The logi3D provides the 3D graphics performances previously unseen in the programmable logic

- ❏ The demo video clip presents the 3D graphics performance achievable by the logi3D running on the ARM Cortex-A8 + Xilinx Spartan-6 FPGA

- ❏ Newer and faster Xilinx Zynq-7000 EPP and 7 Series FPGA (Artix™, Kintex™ and Virtex-7) programmable logic enable higher 3D performances

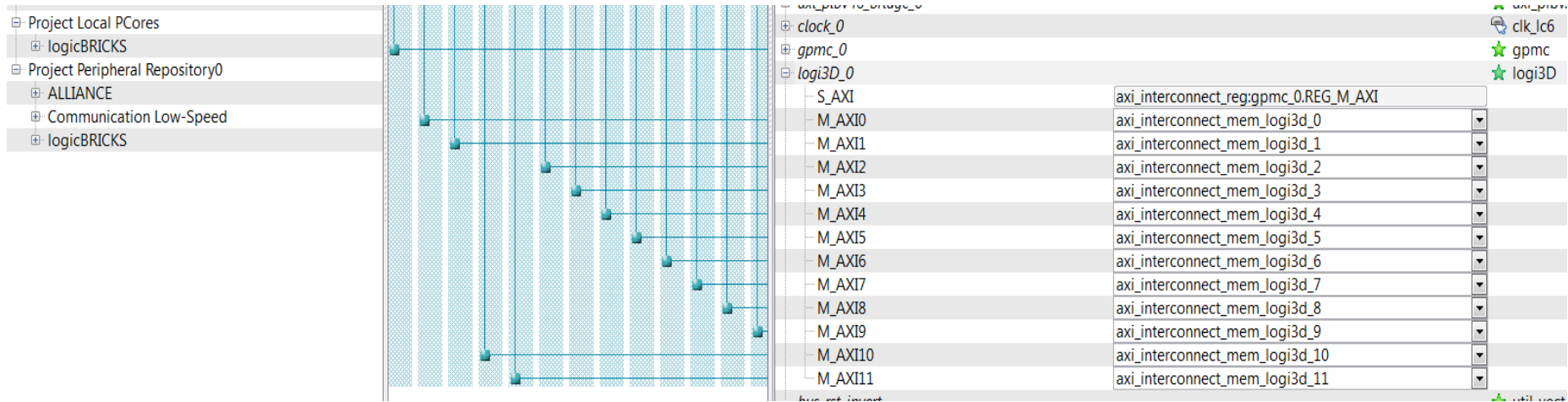- ❏ Zynq-7000 implementations will be faster!

Click Photo to watch Xylon's demo video clip, or visit:

http://www.logicbricks.com/Solutions/EPP-FPGA-logi3D-Graphics-Accelerator-Video-Clip.aspx

To learn more about the used demo hardware system, pleas visit:

http://www.logicbricks.com/Solutions/logiGPU-Graphics-Demonstration-Kit-Zynq-7000-Emulation.aspx

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How to Use the logi3D IP Core?

- Xylon delivers the logi3D as configurable IP core compatible with the Xilinx Platform Studio (XPS) and EDK implementation tools. Designers can use it in a same way as Xilinx IP cores which comes with the XPS.

- Designer can drag the logi3D IP core from the IP repository (left) into the XPS Assembly View (right)

- The AMBA AXI4 SoC bus can be connected by a single click

- Double-click on the logi3D instance in the XPS Assembly View opens the configuration dialog box and allows IP parametrization. It also enables access to IP core's documentation.

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logi3D IP Core – Software Deliverables
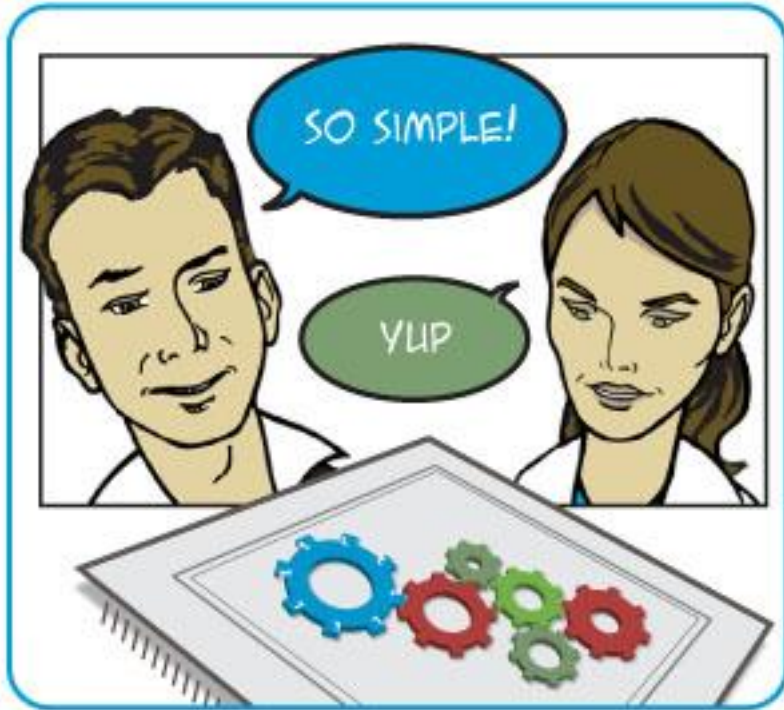

- ❑ The logi3D deliverables includes:

  - ❑ The EGL library for Linux:
    - ✓ Null Window (bin)
    - ✓ X Window System (bin)
  - ❑ GLES 1.1 library (bin)
  - ❑ logi3D driver (bin)
  - ❑ Simple 3D demo (source)

- ❑ Currently supported OS is Linux

- ❑ Support for Microsoft® Windows® Embedded Compact and Android™ is planned for year 2012

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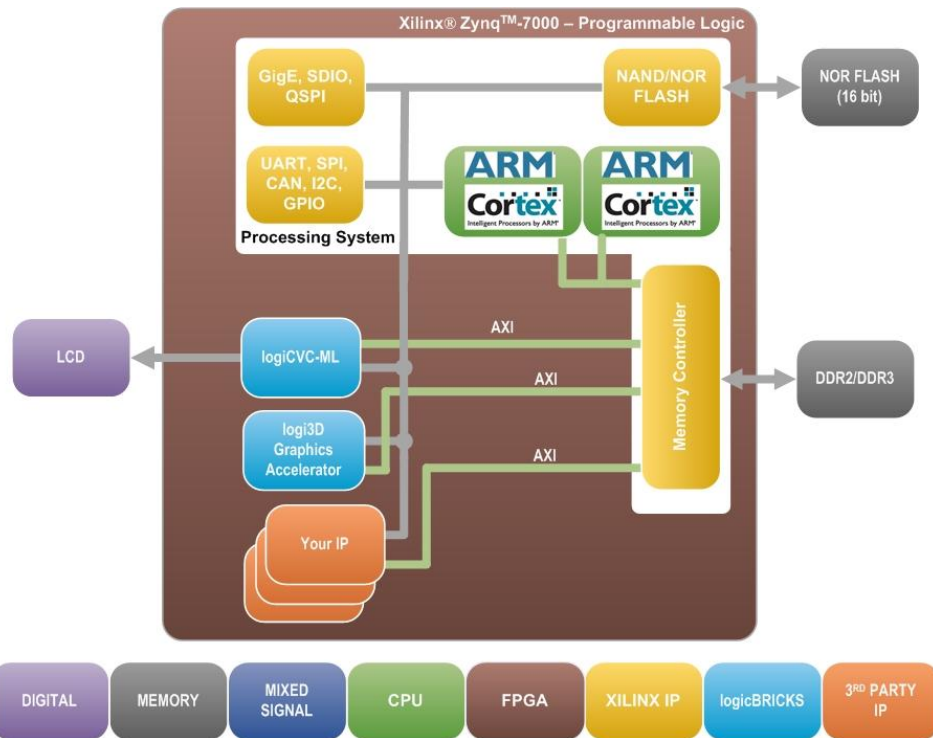
- logi3D is designed primarily for Xilinx Zynq-7000 EPP

- Can be simply interconnected with other IP cores due to its AMBA AXI4 Common Interconnect compliance

- One ARM Cortex-A9 may run the OS, OpenGL ES 1.1 library and graphics and other software application

- The logi3D can use the ARM NEON coprocessor for additional performance

- Xylon offers other logicBRICKS IP cores that complement the logi3D IP core's functionality, such as the logiCVC-ML Compact Multilay Video Controller for LCD displays

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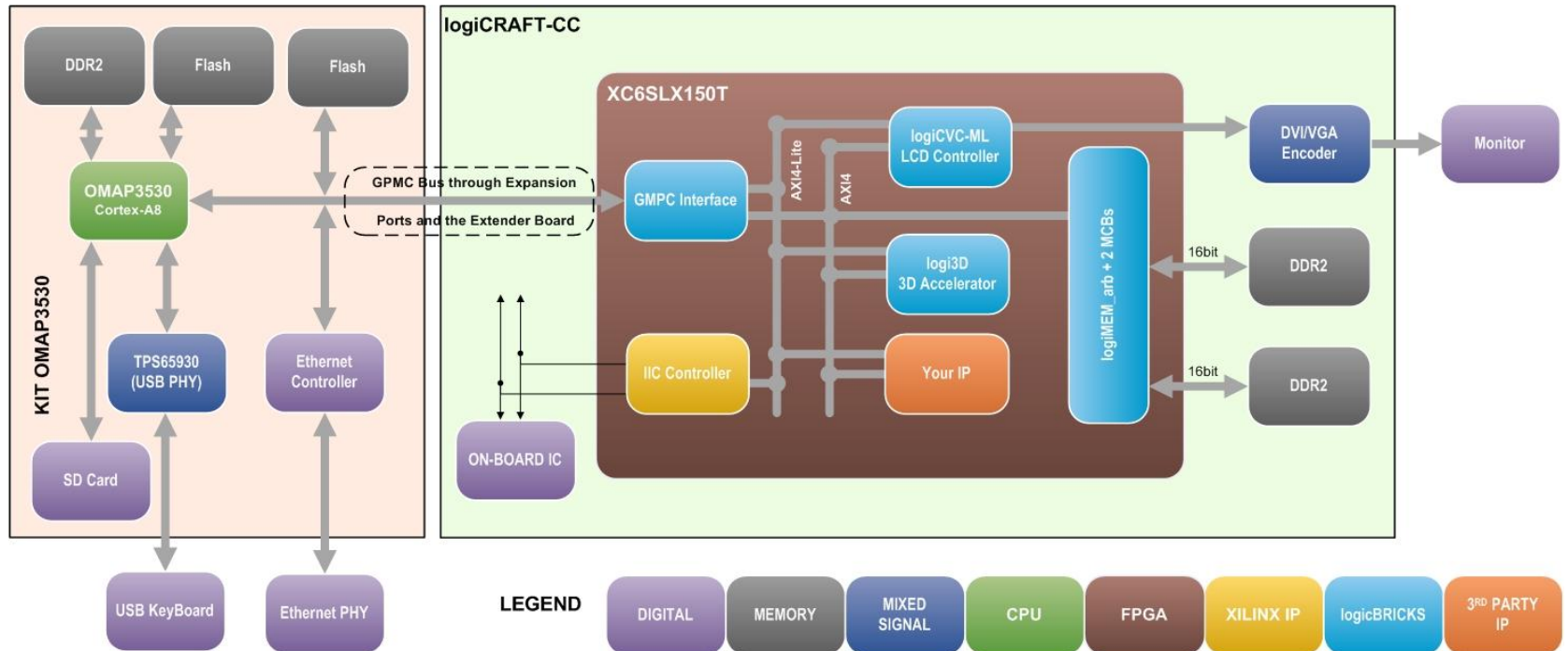
- The block diagram of Xylon's logiGPU demo kit is an example of ASSP+FPGA systems utilizing the logi3D IP Core

- logi3D can be implemented in several Xilinx FPGA families. The FPGA implementation requires an external processor for a full 3D graphics implementation. Xylon's logiGPU Graphics Demonstration Kit, which is used for in-house development, performance estimates and the demo video clip, is an example of such ASSP+FPGA systems.

- To enable early development and demonstrate the IP core before implementing in Xilinx Zynq-7000 EPP devices, Xylon has designed the logiGPU Graphics Demonstration Kit that combines the ARM development kit with the Cortex-A8 processor and the Xylon logiCRAFT-CC FPGA Companion Chip board with the Xilinx Spartan-6 FPGA.

- The logiGPU kit runs the Linux OS and OpenGL ES 1.1 API, and emulates future implementations of the logi3D Graphics Processing Units (GPU) on the Xilinx Zynq-7000 EPP. To learn more, please visit:

  http://www.logicbricks.com/Solutions/logiGPU-Graphics-Demonstration-Kit-Zynq-7000-Emulation.aspx

Expected Performance Improvements

Xilinx Zynq-7000 Features		Xylon logiGPU Kit
2X ARM Cortex-A9 800MHz max*	>	ARM Cortex-A8 600MHz
NEON SIMD	>=	NEON SIMD
DDR3 memory intf. speed	>	DDR2 400MHz max. memory intf. speed
Up to 3000 interconnections between the processing system and programmable logic. If AXI4 runs at 100MHz: 800 MB/sec * efficiency Read/Write	>	GPMC interface: >200 MB/sec Write 30-50 MB/sec Read
Zynq-7000 programmable logic speed	>	Spartan-6 programmable logic speed
Memory bandwidth for GPU[*2]	>=	Memory Bandwidth for GPU

* Xilinx automotive grade Zynq-7000 2x ARM Cortex-A9 targeted to 667MHz max

❑ The table summarizes Zynq-7000 EPP features which will enable better logi3D performance in comparison to performance demonstrated by Xylon's logiGPU demonstration kit

❑ The logi3D IP core is available directly from Xylon

❑ The IP deliverables include:
- ❑ Encrypted VHDL source code compatible with the Xilinx Platform Studio and EDK tools
- ❑ OpenGL ES 1.1 software library, Linux driver and simple C demo application
- ❑ Documentation

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Xylon's IP Cores and Hardware Platforms

logicBRICKS IP Cores

- logiCVC-ML Compact Multilayer Video Controller
- logiWIN Versatile Video Input
- logiBITBLT BitBlock Transfer 2D Graphics Accelerator
- logiBMP Bitmap 2.5D Graphics Accelerator
- logiBAYER Color Camera Sensor Bayer Decoder
- logiVIEW Perspective Transformation and Lens Correction Image Processor
- ... and more

Xylon HW Platforms

- logiCRAFT-CC Companion Chip Platform
- logiCRAFT6 Multimedia Evaluation/Development Platform
- logiTAP Platform for Embedded GUI System Developments
- logiHAC Automotive Hybrid Cluster Development Platform
- ... and more

choose & configure

implement your FPGA w/o coding

you have an amazing idea?
looking for a perfect graphics controller?

logicBRICKS™ make your ideas come true

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Xylon – Design House and IP Provider

Xylon is provider of proven FPGA application solutions and leading-edge IP cores optimized for Xilinx FPGAs in embedded graphics, video, image processing and networking.

CORE COMPETENCES

- ❑ FPGA IP cores development
- ❑ Turn-Key FPGA Solutions
- ❑ Embedded Graphics Solutions
- ❑ SW Drivers and Middleware

Visit offical Xylon web site:

www.logicbricks.com

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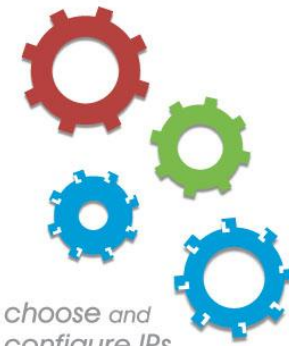260-0031 Japan
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Thank you! Vielen Dank! Arigato!
Hvala!