Xylon d.o.o.

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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Verification	Reference design simulation
Reference Designs & Application Notes	Vivado reference design
Additional Items	SW drivers, API and post-processing library logiADAK ADAS Development Kit
Simulation Tool Used	
Vivado Simulator	
Support	
Support provided by Xylon	

Features

- Advanced HOG/SVM object classification core for support of Object Detection in camera-based video systems
- Supports Xilinx® Zynq®-7000 AP SoC, 7 series and newer FPGAs
- Supports resolutions up to 4096x4096
- Run-time variable input image size
- Includes support for multiple scale detection (pyramid of images)
- User-defined classifier can be run-time loaded via software
- Up to 4 SVM classifiers in a parallel to perform simultaneous detections of different objects
- Switching among 4 pre-loaded object models per SVM on the basis of the scale index
- ARM® AMBA® AXI4 compliant Memory Mapped Register Interface
- AXI4 Slave Stream Video Input Interface
- Supports RGB(8:8:8) and YUV(4:2:2) video stream formats
- High Input Data rate (> 120 Mpixels per Second)
- High Throughput (> 7.6 GMAC/sec for the classification stage)
- Low Latency (< 8 lines)
- Simple programming due to a small number of control registers
- Pedestrian detection classifier trained on a wide range of automotive scenarios included
- C code API and post-processing library available
- Can be evaluated on Xylon logiADAK ADAS kit

Applications

- Driving Assistance Systems
- Video Surveillance
- Robot Navigation
- Assistive Technology for the Visually Impaired
- Content Based Indexing
- Advanced Human-Machine Interfaces

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) [1] sysgen_clk	LCs	Slices [2] (FFs/ LUTs)	IOB	CMT	BRAM [3]	DSP48A	DCM / CMT	GTx	Design Tools
Zynq®-7000 (XC7Z045-2)	240	~14,893	2,327 (7,797/5,480)	0	0	45	35	0	N/A	VIVADO® 2015.4

Notes:

1) The maximum pixel rate is a half of Fmax
2) Including AXI4-lite interface and assuming configuration with default IP parameters, max image size = 1024x1024, max template size = 128x64, 1 SVM. Each additional SVM requires 1913 FFs, 947 LUTs, 15 BRAMs and 32 DSP48s.
3) Number of RAMB18

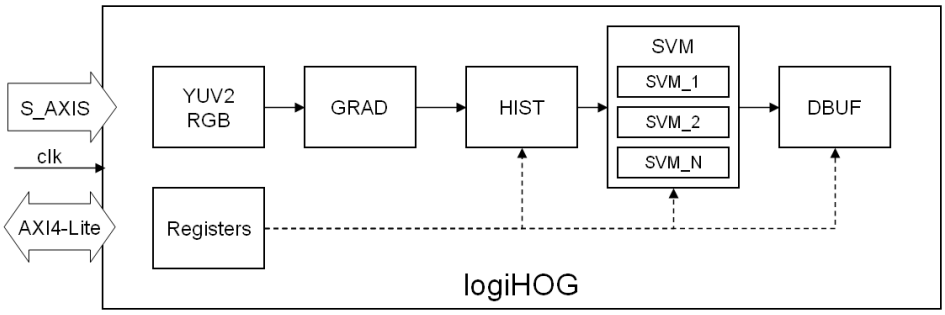

Figure 1 : logiHOG Architecture

General Description

The logiHOG is an HOG/SVM-based object detection logicBRICKS IP core for detection of multiple objects in vision-based embedded applications. It is a direct successor of the logiPDET Pedestrian Detector IP core. The algorithm follows a discriminative approach by combining the HOG-based descriptor and the SVM classifier.

HOG (Histogram of Oriented Gradients) is a descriptor designed to encode object structure. It is particularly suitable for pedestrian detection. SVM (Support Vector Machine) is a non probabilistic binary linear classifier. The core works at a single scale, i.e. the classifier is trained to recognize object at a fixed size. Extension to multiple scales is given by inserting the core in a framework that provides a sequence of re-scaled versions of the same input frame. This way it is possible to detect objects moving in an arbitrary range of distance.

The core is provided with a built-in pedestrian detection classifier, but users can load their own classifier via software API at the run-time. Multiple SVM blocks can be instantiated to simultaneously detect different objects.

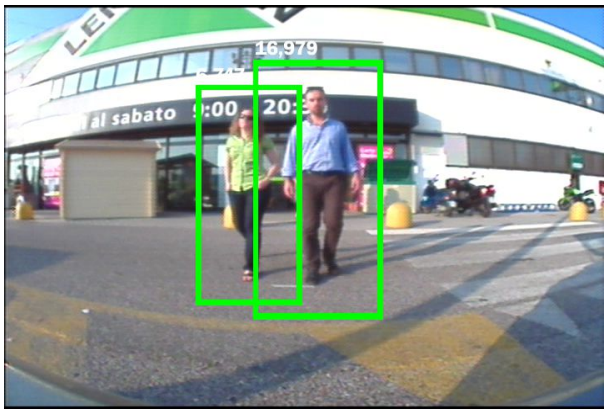

Figure 2: Pedestrian Detection – Screenshot

Object detectors based on HOG/SVM classifiers can be trained and tested with the logiSTK (Figure 3) software tool. The logiSTK tool enables even non-experts in computer vision to execute complex operations, such as the learning process for an automated classifier, in a simple and effective way. The tool can export object classifiers for the logiHOG IP core. By mean of the logiVCS (Figure 4) visual configuration system software tool, logiHOG users can calibrate the camera used on a specific vehicle and automatically compute ROIs (Region of interest) of camera frames where the tracked objects can be found. The logiVCS takes the trained classifiers from the logiSTK software training kit, enables user to tune object tracking parameters, and imports/exports object detectors configurations in the logiADAK kit

To learn more about the logiSTK and logiVCS software tools, please visit:
http://www.logicbricks.com/Solutions/Xylon-ADAS-Development-Kit/Software-Downloads.aspx

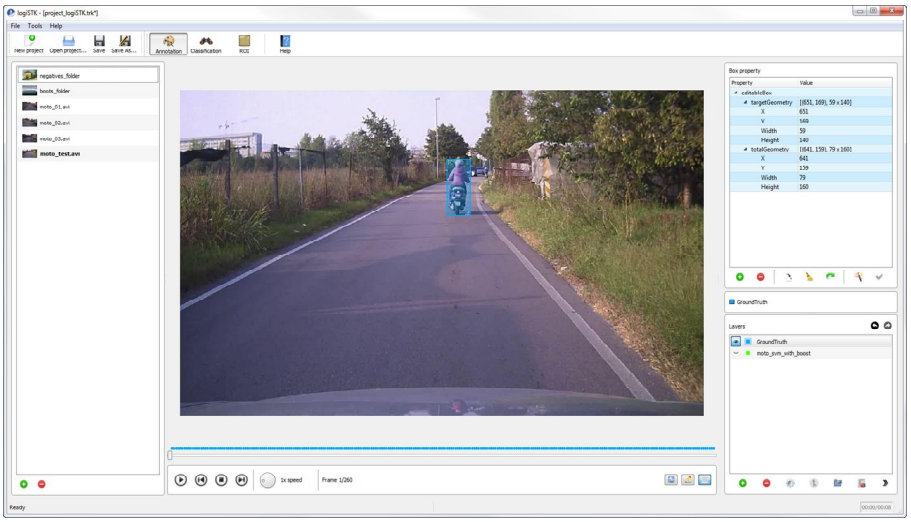

Figure 3: logiSTK Software Training Kit for object detection – Screenshot

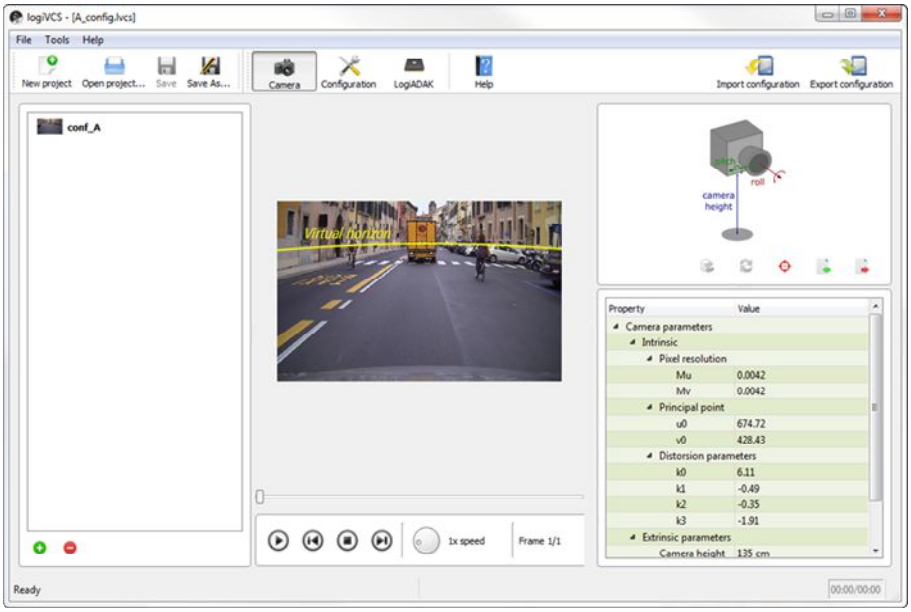

Figure 4: logiVCS Visual Configuration System – Screenshot

Functional Description

The Figure 1 presents internal logiHOG IP core's architecture. The logiHOG functional blocks are: YUV2RGB, GRAD block, HIST block, SVM block, DBUF block and Registers.

YUV2RGB

This is an optional block optionally used with the 16-bit YUV422 video input. It converts the video stream from the YUV422 to 24-bit RGB888 video format.

GRAD block

The GRAD block computes gradient of the input RGB image. The gradient orientation is quantized into 8 bins in 0°-180°. For each input pixel the GRAD block returns the index of the orientation bin (0..7), the fractional part of the quantization, and the gradient magnitude.

HIST block

The HIST block generates the 8-bins oriented gradient histograms (HOG) for each 8x8 cell of the input image. It returns the bins of the cell histograms corresponding to the current position of the detection sliding window.

SVM block

The SVM block is responsible of the histogram block normalization (a block is composed by 2x2 adjacent cells) and the estimation of the confidence (score) on the current detection window. It is possible to instantiate up to 4 SMV blocks to detect different objects in parallel. User-defined classifiers can be loaded run-time through the register interface. In addition, it is possible to run-time switch among different pre-loaded classifiers for each SVM block on the basis of the scale index.

DBUF block

The DBUF buffers the detected objects with a score greater than zero. For each of these objects, which are detected at a certain scale of the sequence, scale index, position, score and the index of the SVM detected the object (in case of multiple SVMs) are memorized in the output buffer.

logiHOG Registers

The logiHOG register interface can be configured as AXI4-Lite interface.

Core I/O Signals

Descriptions of all signals I/O are provided in Table 2.

Table 2: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
clk	Input	input processing clock
AXI4-Stream signals (slave bus)		
s_axis_tdata(23:0)	Input	Video Data: • for 24-bit RGB input (RED [23:16] ; GREEN [15:8] ; BLUE [7:0]) • for 16-bit YUV422 input type only 15:0 is in use (U/V [15:8] ;Y [7:0])
s_axis_tvalid	Input	Valid
s_axis_tuser	Input	Start Of Frame
s_axis_tlast	Input	End Of Line
s_axis_tready	Output	Ready
Register Interface		
AXI4-Lite Interface	BUS	Refer to AMBA AXI version 4 specification from ARM

Verification Methods

The logiHOG IP core is fully supported by Xilinx Vivado design tool. This tight integration tremendously shortens IP integration and verification. A full logiHOG implementation does not require any particular skills beyond general Xilinx tools knowledge. To learn more about this IP core, please visit:

http://www.logicbricks.com/Products/logiHOG.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Xilinx System Generator for DSP (MathWorks Matlab/Simulink) to source model access

Available Support Products

The logiHOG can be fully evaluated on the logiADAK programmable development platform for upcoming advanced driver assistance (ADAS) applications that require intensive real-time video processing, parallel execution of multiple advanced algorithms and versatile interfacing with sensors and vehicle's communication backbones. The abundant performance and reprogrammability of the Zynq-7000 AP SoC device enables ADAS designers to design SoCs that outperform competing solutions and achieve a new level of system differentiation through a combination of hardware-accelerated video inputs from multiple camera inputs and the ability to quickly adapt to ever changing sensor setups and interfacing. To learn more about this product, please contact Xylon or visit our website:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiADAK.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.0.1	29.06.2015	Initial datasheet release

The logiHOG IP core, logiSTK and logiVCS software tools are sourced from Technology Partner
eVS embedded Vision Systems Srl.