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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference designs .xdc examples
Reference Designs & Application Notes	Reference design included with the Xylon logiADAK Development Kit For other evaluation options, please contact Xylon
Additional Items	Bare-metal software driver
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Designed and optimized for Xilinx® Zynq®-7000 All Programmable SoC
- Real-time driver drowsiness detection based on the video input from optical camera
- Detection rate set to 10 fps
- Inputs are 3D points from the face detector and tracker: eyes, gaze, eyebrows, lips and head
- Drowsiness states estimated via face behavioral features: PERCLOS, microsleep, eye closure duration, blink frequency, fixed gaze, yawn, yawning frequency, head angle and eyebrow raise
- Classified drowsiness states: not sleepy, slightly sleepy, sleepy, rather sleepy, very sleepy, extremely sleepy and sleeping
- Configurable behavioral features tracking periods and drowsiness state thresholds
- Can be used while wearing sunglasses and during the night driving (with the proper optical system)
- Road verified on the fleet of test vehicles and under different road and weather conditions
- Xylon has developed measurement optical camera system (meets the standard IEC 62471 for LED lighting products - eye safety) for driver fatigue monitoring while wearing sunglasses and during the night driving
- ARM® AMBA® AXI4-Lite bus compliant registers interface
- Controlled by a single ARM Cortex™-A9 CPU core with a lightweight software library
- Required resources utilization and achievable performance allow for parallel execution of other real-time vision applications on the same Xilinx Zynq-7000 All Programmable SoC
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepackaged for Xilinx Vivado® Design Suite and fully controllable through the IP Integrator GUI interface
- IP deliverables include the software driver, documentation and technical support

Table 1: Example of Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) aclk	Slices[1] (FFs/LUTs)	IOB[2]	BRAM	MULT/ DSP48/E	CMT (PLLs/DCMs)	GTx	Design Tools
Zynq®-7000 (XC7Z020)	120	1192 (3607/3510)	0	0	7	0	N/A	Vivado 2014.4

Notes:
1) Assuming the following configuration: 32-bit AXI4-Lite register interface with readable registers.
2) Assuming register and memory interfaces, as well status signals are connected internally.

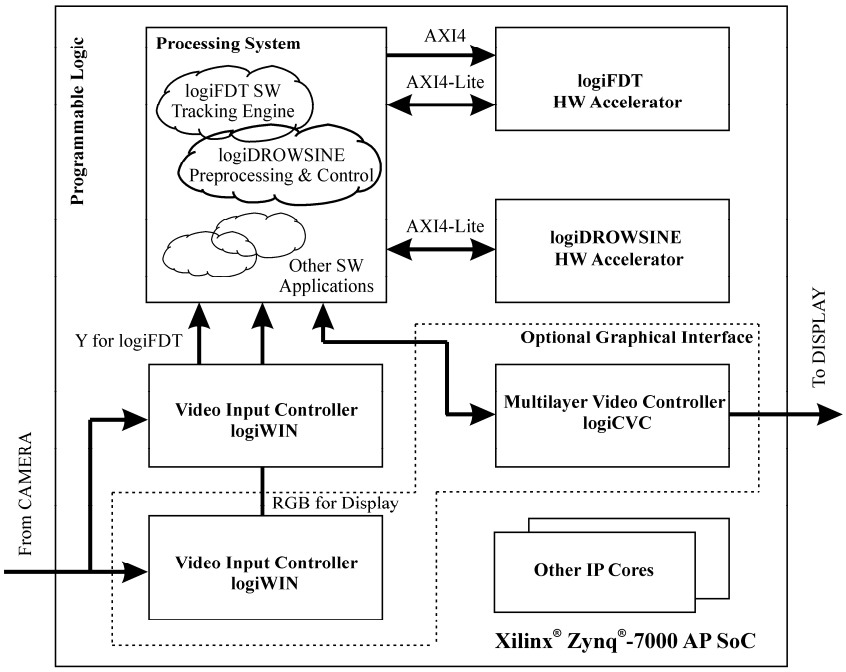

Figure 1: Example SoC Architecture with the Integrated logiDROWSINE IP Core

Applications

- Driver Drowsiness Monitoring Systems (ADAS)
- Other Advanced Driver Assistance (ADAS) applications
- Medical Applications, etc.

General Description

For the driver the main effect of drowsiness is a deteriorating driving performance and a progressive withdrawal of attention from the road. Impaired driving skills of sleepy drivers have been one of the major accident causes and can lead to severe physical injuries, deaths and significant economic losses. Many efforts have been made recently to develop reliable and non-intrusive detection of driver drowsiness that can save lives and property.

The logiDROWSINE is a computer vision IP core that detects driver drowsiness and distraction based on facial movements monitored through a camera placed in a vehicle cabin. The IP core monitors movements of driver's eyes, gaze, eyebrows, lips and head, and continuously tracks nine facial behavioral features indicating the drowsiness: PERCLOS (PERcentage of eyelid CLOSure), microsleep, eye closure duration, blink frequency, fixed gaze, yawn, yawning frequency, head angle and eyebrow rise.

Based on the behavioral features tracked during the driving in a real environment, the implemented logiDROWSINE classifier recognizes seven levels of drowsiness: not sleepy, slightly sleepy, sleepy, rather sleepy, very sleepy, extremely sleepy and sleeping. The recognized drowsiness levels are provided as IP core outputs and can be used as triggers for driver alerts, or inputs to higher level classifiers within ADAS systems that combine computer vision drowsiness detection with other detection methods.

The logiDROWSINE receives 3D coordinates of facial features from the logiFDT Face Detector and Tracker IP core (Figure 1) which finds and tracks the face and facial features in video sequences in a real time. Xylon has developed the logiFDT IP core for use with Xilinx All Programmable through a technology partnership with the provider of face tracking and analysis technology Visage Technologies AB (www.visagetechnologies.com).

Figure 2: Screenshot from the Xylon Demo System Integrated in a Test Vehicle
(Video clip: http://www.logicbricks.com/logicBRICKS-IP-Library/Video-Galleries/logicBRICKS-Face-Tracking-Demo.aspx)

The logiDROWSINE IP core is designed and carefully optimized for use in Xilinx Zynq-7000 All Programmable SoC. Digital Signal Processing (DSP) algorithms implemented in programmable logic assure high computing performance and off-load the SoC processing system. The IP core can be controlled by a single ARM Cortex™-A9 CPU core with a lightweight software library. Low resource utilization enables implementation and parallel execution of other ADAS applications on a single Xilinx SoC device.

Standard bussing architecture, software support and IP core deliverables compatible with the Xilinx Vivado Design Suite, enable ADAS designers to implement driver drowsiness applications in a plug-and-play manner.

Xylon provides the logiDROWSINE reference design as a part of the logiADAK Automotive Driver Assistance Kit. To find more about other evaluation options, please contact Xylon.

Xylon has developed measurement optical camera system suitable for driver fatigue monitoring during the night driving, while wearing sunglasses and during other road and weather conditions. To learn more about this measurement system, please contact Xylon at info@logicbricks.com.

Core Modifications

The core is supplied in an encrypted VHDL format which allows the user to take a full control over configuration parameters. Table 2 outlines some of the logiDROWSINE configuration parameters selectable prior to the VHDL synthesis. For a complete list of parameters, please consult the logiDROWSINE User's Manual delivered with the IP core.

Table 2: VHDL Configuration Parameters (Examples) of the logiDROWSINE IP core

Parameter	Description
C_DWIDTH	Input/output data word length
C_FRAMES_PER_SEC	Frame rate of camera, in fps
C_TBLINK	Period within which eye blink frequency is measured, in sec
C_THRESHOLD_EXTREMELYSLEEPY	Above this threshold is the Extremely sleepy state

The logiDROWSINE has been constructed with regard to adaptability to various application requirements. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach

the optimal use of the logiDROWSINE core or to supplement some of your specific functions, you can order the source code or allow us to tailor the logiDROWSINE to your requirements. The logiDROWSINE source code is available at additional cost from Xylon.

Core I/O Signals

The core I/O signals have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: logiDROWSINE I/O Signals

Signal	Signal Direction	Description
Register Interface		
AXI4-Lite Slave Interface	Bus	Refer to ARM AMBA AXI4 specification

Verification Methods

The logiDROWSINE test setups already have thousands of hours of testing on the fleet of test vehicles driven by professional drivers under different road and weather conditions.

The logiDROWSINE is fully supported by the Xilinx Vivado (IPI) Design Suite. This tight integration tremendously shortens IP integration and verification. A full logiDROWSINE implementation does not require any particular skills beyond general Xilinx tools knowledge. The logiDROWSINE IP core can be fully evaluated as a part of Xylon logiADAK Automotive Driver Assistance Kit. To learn more about this IP core, please visit: http://www.logicbricks.com/Products/logiDROWSINE.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

The logiFDT Face Detector and Tracker IP core finds and tracks the face and facial features in video sequences in real time and returns full 3D head pose, gaze direction, facial features coordinates and a wealth of other information. The logiDROWSINE IP core takes 3D coordinates from the logiFDT IP core outputs and processes them in order to detect classified drowsiness states. To learn more about this product, please contact Xylon or visit our website:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiFDT.aspx

The logiADAK Automotive Driver Assistance kit is Xilinx Zynq-7000 AP SoC based programmable platform for Advanced Driver Assistance (ADAS) that require intensive real-time video processing, parallel execution of multiple advanced algorithms and versatile interfacing with sensors and vehicle's communication backbones. The logiADAK deliverables include full logiDROWSINE reference design. To learn more about this product, please contact Xylon or visit our website:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiADAK.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.0	16.11.2015.	Initial Xylon release. IP core prepared for Vivado 2014.4.

visage I SDK™ Face Tracking and Analysis technology is sourced from our technology partner Visage Technologies AB.