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Features

- Supports Xilinx® 7 Series, UltraScale™ and UltraScale+™ SoCs and FPGAs
- Please contact Xylon for Spartan®-6, Virtex®-6, Spartan®-3 and other Xilinx FPGA family support
- Display controller IP core for LCD, CRT and other display types
- Available SW drivers for Linux, Android™, QNX and Microsoft® Windows® Embedded Compact
- Display resolutions up to 8192x8192 including 4K2K at 60fps
- Supports up to 5 layers; the last one configurable as a background color
- Programmable layer address, size and position
- Alpha blending and color keyed transparency allows blending of video and graphics content on the screen
- Pixel, Layer, or color lookup table (CLUT) alpha blending mode can be set for each layer independently
- Packed pixel layer memory organization supports 3, 6, 8 and 10 bits per color:
    - RGB - 8bpp 3-3-2, 8bpp with Color Look up Table, 16bpp 5-6-5, 24bpp 8-8-8 and 30bpp 10-10-10
    - YCbCr - 16bpp (4:2:2), 20bpp (4:2:2), 24bpp (4:4:4), 30bpp (4:4:4)
- Support for multiple output interfaces:
    - Parallel display data bus (RGB or YCbCr) with 1, 2 or 4 pix per clock: 12x2-bit, 15, 16, 18, 20, 24, 30 bit
    - AXI4-Stream with 1, 2 or 4 pix per clock
    - Digital Video ITU-656: PAL and NTSC
    - LVDS output format: 3 or 4 data pairs plus clock (currently not supported in US and US+ devices)
    - Camera link output format: 4 data pairs plus clock (currently not supported in US and US+ devices)
    - DVI output format (currently not supported in US and US+ devices)
- ARM® AMBA® AXI4 memory interface with configurable data width (32, 64, 128 or 256 bits)

Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	XDC
Reference Designs & Application Notes	Reference designs for ZC702 and ZC706 from Xilinx, and ZedBoard™ and MicroZed™ evaluation kits from Avnet Electronics Marketing.
Additional Items	SW drivers for different OSs
Supported Simulation Tools	
Mentor Graphics ModelSim® and QuestaSim® Aldec Active-HDL™ and Riviera-PRO™	
Support	
Support provided by Xylon	

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)			LUT	FF	IOB	BRAM Tile	DSP48	PLL/ MMCM	BUFG/ BUFR	GTx	Design Tools
	mclk	vclk	rclk									
Artix®-7 (XC7A100T-1)	234	220	192	489	791	28	1	0	0	0	0	Vivado® 2016.2
Kintex®-7 (XC7K355T-2)	384	266	200	477	791	28	1	0	0	0	0	Vivado® 2016.2
UltraScale+™ (XCZU9EG-1)	333	522	330	493	806	28	1	0	0	0	0	Vivado® 2016.2

1) Assuming the following configuration: RGB888 output, 1xRGB888 layer, AXI4-Lite register interface, 64-bit AXI4 interface
2) Assuming only display control signals are routed off-chip, register and memory interfaces are connected internally
3) Implementation statistics given for Artix-7, Kintex-7 and UltraScale FPGAs are also valid for the corresponding SoC and MPSoC families
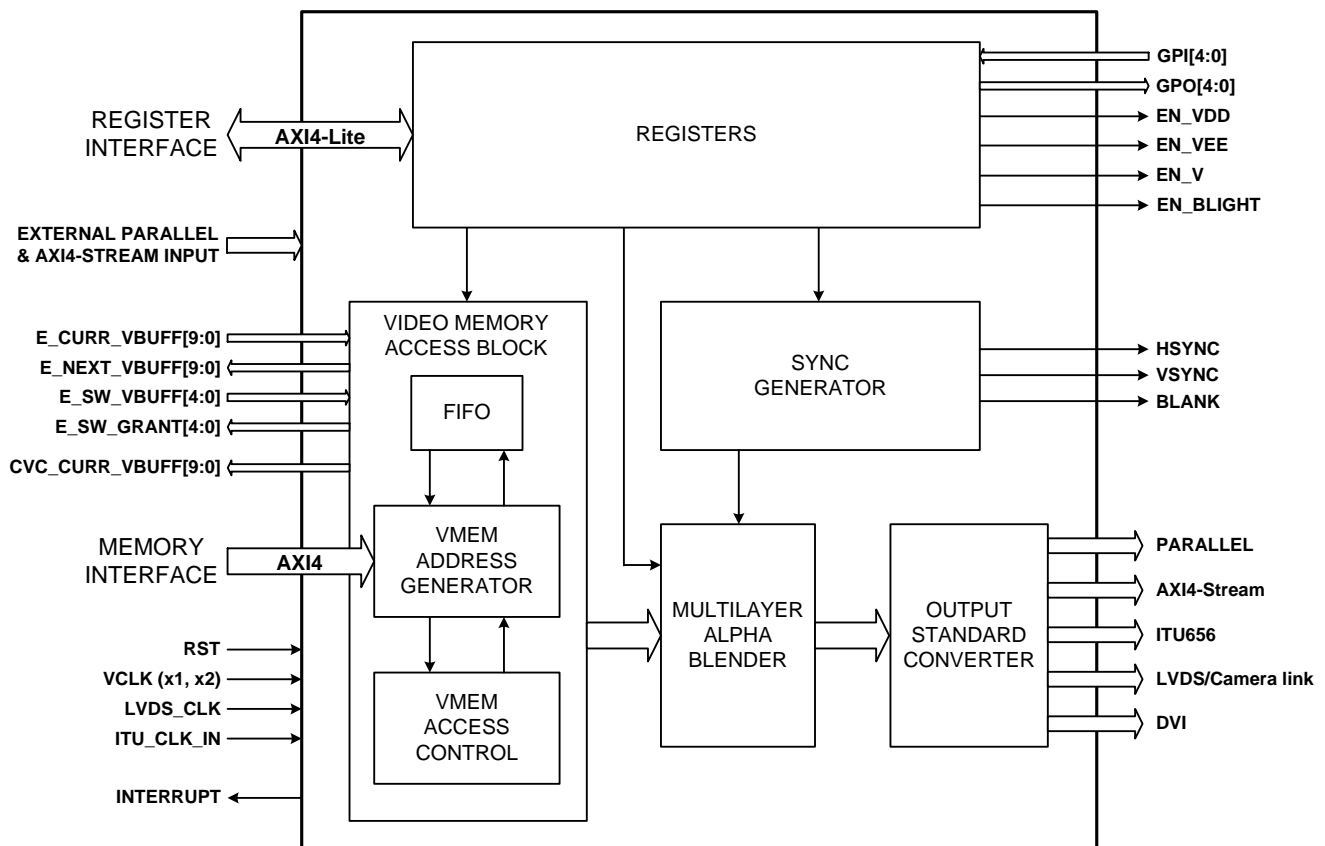
Figure 1: logiCVC-ML Architecture

Features (cont)

- Simple programming of control registers through AXI4-Lite interface
- Supports synchronization to external parallel or AXI4-Stream input (data used for one layer)
- Double/triple buffering enables flicker free reproduction of live video streams overlaid by graphics HMI
- Display power-on sequencing control signals
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepared for Xilinx Vivado® Design Suite implementation tools (Xilinx Platform Studio support on request)
- Simple Plug'n'Play with other Xylon logicBRICKS™ IP cores, such as:
    - logiISP Image Signal Processing (ISP) Pipeline
    - logiBITBLT Bit Block Transfer 2D Graphics Accelerator
    - logi3D Scalable 3D Graphics Accelerator
    - logiWIN Versatile Video Input Controller

Applications

This IP core can be used in all applications that require graphics/video display output. Example applications are:
- Car Infotainment and Driver Assistance
- Industrial Test Equipment, Surveillance and Robotics
- Medical applications
- Aerospace and Defense systems
- …

General Description

The logiCVC-ML Compact Multilayer Video Controller is a graphics/video display controller IP core optimized for Xilinx 7 Series, UltraScale and UltraScale+ SoC and FPGA devices. It controls TFT flat panel displays, DVI monitors and, by means of external video converters, S-Video, Composite Video devices and CRT displays (i.e. VGA monitors) and CVBS displays.

For use in Xilinx 7 Series, UltraScale and UltraScale+ SoC and FPGA based systems with no operating system, Xylon provides standalone logiCVC-ML (Bare Metal, no OS) software driver as a standard part of IP core's deliverables. In addition to the bare-metal SW driver, Xylon provides logiCVC-ML software drivers for several operating systems (OS): Linux, Android, QNX and Microsoft Windows Embedded Compact. The OS specific software drivers allow for an easy IP core use – standard SW drivers enable work with industry standard graphics libraries and graphics widget toolkits. They enable SW programmers to work fast and efficiently with familiar development tools, and within familiar software development environments.

Multilayer support provides on screen display functions: alpha blending, color keyed transparency among layers, hardware cursors and fast scrolling and pan functions. Powerful blending features enable easy mixing of streaming videos, which can be processed by custom made DSP modules, with graphics content generated by the CPU and/or graphics accelerators. All of these features are supported by hardware and require only low CPU processing power.

The interface to the frame buffer, or the video memory, is designed for SDRAM (SDR, DDR, DDR2, DDR3, …) or SRAM implementation. For easier system integration, logiCVC-ML uses ARM AMBA AXI4 buses.

Standard bussing architecture, rich software support and IP core's format compatible with Xilinx implementation tools, enable developers to add graphics/display support to their Xilinx 7 Series, UltraScale and UltraScale+ SoCs and FPGAs in a plug-and-play manner.

Xylon provides a number of free downloadable logicBRICKS reference designs to enable risk-free evaluation of logicBRICKS graphics IP cores on Xilinx Zynq-7000 All Programmable SoC based ZC702 and ZC706 Evaluation Board or ZedBoard from Avnet Electronics Marketing. To learn more, please visit:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

Functional Description

The logiCVC-ML internal structure is shown on the block diagram on Figure 1.

The logiCVC-ML's functional blocks are: Video Memory Access Block, Video Address Generator, FIFOs, Sync Generator, Multilayer Alpha Blender, Registers.

Video Memory Access Block

The Video Memory Access Block consists of three sub modules: Video Memory Access Control, Video Memory Address Generator and FIFOs. The Video Memory Access Block fetches video data from the video memory through AXI4 bus to the local FIFOs. The Video Address Generator calculates video memory pointers for each layer. The Video Memory Access Block ensures that each FIFO is filled with the required number of pixels and it performs arbitration between memory requests of each layer.

There is one FIFO per layer used for temporary storage of pixels. The FIFOs optimize the usage of video memory bandwidth and resynchronize incoming data to the display clock.

Sync Generator

The Sync Generator generates video synchronization signals. Duration of sync signals and their relative position to the display data (i.e., visible picture on the screen) and polarity can be adjusted through the set of logiCVC-ML registers. Additionally, external parallel or AXI4-Stream input stream can be used for synchronization and sync generation.

Multilayer Alpha Blender

The Multilayer Alpha blender block consists of five configurable layer blocks. The outputs of the layer blocks are converted to the appropriate color space and mixed according to alpha/transparent factors and layer priority. The Blender supports layer, pixel and color alpha blending methods.

Output Standard Converter

The Output Standard Converter receives pixel data and control signals and converts them to requested video output format defined in Vivado GUI. It can output ITU656, LVDS (LVDS with one clock and three or four data pairs or Camera link with one clock and four data pairs), DVI, parallel (RGB, YCbCr 4:4:4 or YCbCr 4:2:2) or AXI4-Stream format. Therefore, it consists of five main modules: ITU656 generator, LVDS generator, DVI generator, YCbCr 4:4:4 to 4:2:2 converter and AXI4-Stream generator.

Registers

All logiCVC-ML registers are instantiated in this block. The CPU has access to all these registers through the AXI4-Lite interface.

Core Modifications

The core is supplied in an encrypted VHDL format and packaged for Xilinx Vivado Design Suite, which allows the user to take full control over configuration parameters. Table 2 outlines the most important logiCVC-ML configuration parameters selectable prior to VHDL synthesis. For a complete list of parameters, please consult the logiCVC-ML User's Manual delivered with the IP core.

Table 2: Subset of logiCVC-ML configuration parameters

Parameter	Description
C_DISPLAY_INTERFACE	Video output type: Parallel, ITU656, LVDS, camera link, DVI, AXI4-Stream
C_DISPLAY_COLOR_SPACE	Video output interface color space (RGB, YCbCr 4:2:2, YCbCr 4:4:4)
C_PIXEL_PER_CLOCK	Number of pixels per clock pipeline and output (1, 2, 4)
C_PIXEL_DATA_WIDTH	Parallel video data output width
C_USE_EMB_SYNC	Use embedded syncs on parallel video output
C_USE_SIZE_POSITION	Layer size and position functionality implementation on/off
C_NUM_OF_LAYERS	Number of layers (up to 5)
C_LAYER_X_TYPE	Layer X type (RGB, YCbCr, Alpha)
C_LAYER_X_DATA_WIDTH	Layer X data width
C_LAYER_X_ALPHA_MODE	Layer X alpha blending mode
C_LAYER_X_ADDR	Layer X default memory address
C_BUFFER_X_OFFSET	Layer X buffer offset
C_USE_BACKGROUND	Last layer configuration as background on/off
C_MEM_LITTLE_ENDIAN	Memory access endianness
C_USE_MULTIPLIER	Defines type of multipliers
C_USE_XTREME_DSP	DSP resources implementation on/off
C_USE_E_INPUT	Synchronize logiCVC to external parallel or AXI4-Stream input and use data as a layer
C_E_DATA_WIDTH	Extern parallel layer data width

The logiCVC-ML has been constructed with regard to adaptability to various display types and has been tested on many popular displays. However, there may be instances where source code modification would be necessary. Therefore, if you wish to reach the optimal use of the logiCVC-ML core or to supplement some of your specific functions, you can order the source code or allow us to tailor the logiCVC-ML to your requirements. The logiCVC-ML source code (VHDL sources) is available at additional cost from Xylon.

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in the Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
RST	Input	Global reset input, high active
VCLK	Input	Video clock input
VCLK2	Input	Video clock input x2 (used for 12bit parallel multiplexed output interface)
ITU_CLK_IN	Input	ITU656 clock input (27 MHz and synchronous to VCLK)
LVDS_CLK	Input	LVDS clock
Memory Interface		
AXI4 Master Interface	Bus	Refer to Xilinx AXI Reference Guide
Register Interface		
AXI4-Lite Slave Interface	Bus	Refer to Xilinx AXI Reference Guide
Video Output Signals		
PIX_CLK	Output	Pixel clock
PIX_CLKN	Output	Pixel clock inverted
HSYNC	Output	Horizontal sync
VSYNC	Output	Vertical sync
BLANK	Output	Blank/display enable at TFT
D_PIX[n : 0]	Output	Video pixel data bus (1, 2 or 4 pixels per clock)
ITU656_CLK	Output	ITU656 clock
ITU656_DATA[n:0]	Output	ITU656 data
LVDS_DATA_OUT_P[3:0]	Output	LVDS pixel data, positive
LVDS_DATA_OUT_N[3:0]	Output	LVDS pixel data, negative
LVDS_CLK_OUT_P	Output	LVDS clock, positive
LVDS_CLK_OUT_N	Output	LVDS clock, negative
DVI_CLK_OUT_P	Output	DVI clock, positive
DVI_CLK_OUT_N	Output	DVI clock, negative
DVI_DATA_OUT_P[2:0]	Output	DVI pixel data, positive
DVI_DATA_OUT_N[2:0]	Output	DVI pixel data, negative
AXI4-Stream Master Video Interface	Bus	Refer to Xilinx AXI Reference Guide
External Input Signals		
E_VCLK	Input	External VCLK (used when external parallel input is used)
E_VSYNC	Input	External VSYNC (used when external parallel input is used)
E_HSYNC	Input	External HSYNC (used when external parallel input is used)
E_BLANK	Input	External BLANK (used when external parallel input is used)
E_DATA[n : 0]	Input	External parallel data (used when external parallel input is used)
E_VIDEO_PRESENT	Input	External video present (used when external parallel input is used)
AXI4-Stream Slave Video Interface	Bus	Refer to Xilinx AXI Reference Guide
Auxiliary Signals		
E_CURR_VBUFF[9:0]	Input	Current external stream video memory buffer (two bits per layer)
E_NEXT_VBUFF[9:0]	Output	Next external stream video memory buffer to write to (two bits per source)
E_SW_VBUFF[4:0]	Input	External switch logiCVC-ML video memory buffers request (one bit per layer)
E_SW_GRANT[4:0]	Output	External switch grant (one bit per source, handshaking signal for E_SW_VBUFF)

Signal	Signal Direction	Description
CVC_CURR_VBUFF[9:0]	Output	Current CVC reading video buffer (two bits per layer)
GPI[4:0]	Input	General purpose input
GPO[4:0]	Output	General purpose output
INTERRUPT	Output	CVC Interrupt signal, level sensitive, high active
EN_VDD	Output	Enable Vdd power supply
EN_BLIGHT	Output	Enable backlight power supply
EN_V	Output	Enable display control/data signals
EN_VEE	Output	Enable Vee power supply

Verification Methods

The logiCVC-ML is fully supported by the Xilinx Vivado Design Suite. This tight integration tremendously shortens IP integration and verification. A full logiCVC-ML implementation does not require any particular skills beyond general Xilinx tools knowledge. The encrypted IP supports running simulations in Mentor Graphics ModelSim and QuestaSim, and Aldec Active HDL and Riviera PRO.

The logiCVC-ML evaluation IP core can be downloaded from Xylon web site and fully evaluated in hardware.

URL: http://www.logicbricks.com/Products/logiCVC-ML.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon provides several free pre-verified reference designs for the most popular Xilinx Zynq-7000 AP SoC based evaluation kits: ZC702, ZC706, MicroZed and ZedBoard. Design deliverables include: evaluation logicBRICKS IP cores, hardware design files prepared for Xilinx Vivado Design Suite, complete Linux OS image, Xylon logicBRICKS software drivers for Linux OS and demo software applications.

To learn more about the Xylon reference designs, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

To learn more about the available software support for the logiCVC-ML display controller IP core, please visit:

URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/OS-IP-Core-Support.aspx

The latest Linux software drivers are available from:

URL: https://github.com/logicbricks?tab=repositories

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.06.	09.04.2010.	New doc template
2.00.	15.09.2010.	AXI Interface update
2.01.	14.03.2011.	DVI output interface support
2.04.	11.11.2011.	Support of new FPGA families
2.05.	21.03.2012.	Xilinx Zynq^{TM} 7000 EPP support. YCbCr 4:4:4 or 4:2:2 output support.
3.00.	17.09.2012.	Support for YCbCr layers, display color space, alpha plane, reset input, configurable FIFO size.
3.01.	07.03.2013.	Support for DVI in 7 Series. Removed vclksel and vcdivsel and added gpi and gpo signals.
3.02.	03.05.2013.	Small text corrections.
4.00.	01.02.2014.	Support for programmable layer address; removed C_LAYER_OFFSET, C_VMEM_BASEADDR and C_VMEM_HIGHADDR generics; added LAYER_ADDR generics.
4.01.	21.05.2014.	Added current CVC reading buffer output port; renamed v_en output port to en_v.
5.0	03.04.2015.	Added support for 10 bit per color, up to 8192x8192 resolution, parallel pixel pipeline, AXI4-Stream interface, 256 bit AXI4 data interface. Removed support for XPS (ISE) Design Suite and PLB, XMB and OPB interfaces.
5.1	27.09.2016.	Added support for Xilinx UltraScale and UltraScale+ families.
5.2	14.12.2016.	Updated example implementation statistics for new IP version.