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Core Facts

Provided with Core	
Documentation	SW User's Manual
Design File Formats	Precompiled SW library, Encrypted VHDL
Constraints Files	Reference designs .xdc
Verification	Simulated and hardware validated
Reference Designs & Application Notes	Reference designs for the ZC702 kit from Xilinx and MicroZed™ Embedded Vision Kit from from Avnet Electronics Marketing
Additional Items	Bare-metal software driver
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Configurable face tracking engine optimized for Xilinx® Zynq®-7000 All Programmable SoC
- Real-time face and facial features tracking in video sequences from a camera (up to 30fps)
- Depending on the configuration, the tracked facial features include the mouth contour, chin pose, eyebrow contours, eye closure, gaze direction...
- Easy-to-Use API for accessing the tracking data:
  - 3D head pose (translation and rotation)
  - Gaze direction and eye closure
  - Facial feature coordinates in global 3D space
  - Feature points specified according to the MPEG-4 FBA standard
  - Action units describing the current facial expressing, i.e. brow raise, lips stretch, jaw drop, etc.
  - 3D model of the face in current pose and expression returned as signle textured 3D triangle mesh
  - Other tracking data…
- Fully automatic operation and robust recovering from losses due to occlusions, face turning away and similar
- Tracking internally works on a single-channel YUV video (Y – luminance component used), which can be recorded by color, grayscale and infrared camera. For thermal video info, please contact Xylon.
- Carefully hardware/software partitioned to assure max. performance and min. resources utilization
- The tracking engine uses single ARM® Cortex™-A9 CPU core supported by hardware acceleration of the most used computing intensive operations implemented in programmable logic
- The required Zynq-7000 AP SoC resources utilization and achievable performance allows for parallel execution of other real-time vision applications on the same SoC device
- Hardware accelerated IP block performs normalized cross-corelation and finds the preprogrammed template (image pattern) in the captured source image

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz) aclk	Slices[1] (FFs/LUTs)	IOB[2]	BRAM	MULT/ DSP48/E	CMT (PLLs/DCMs)	GTx	Design Tools
Zynq®-7000 (XC7Z020)	120	2104 (5680/5597)	0	9	59	0 (0/0)	N/A	Vivado 2014.3

Notes:
1) Assuming the following configuration: 32-bit AXI4-Lite register interface with readable registers, 64-bit AXI4 memory interface (pattern and image) with 16-word burst size, with pattern maximal size of 64x64 pixels and image maximal size of 128x128 pixels
2) Assuming register and memory interfaces, as well status signals are connected internally.

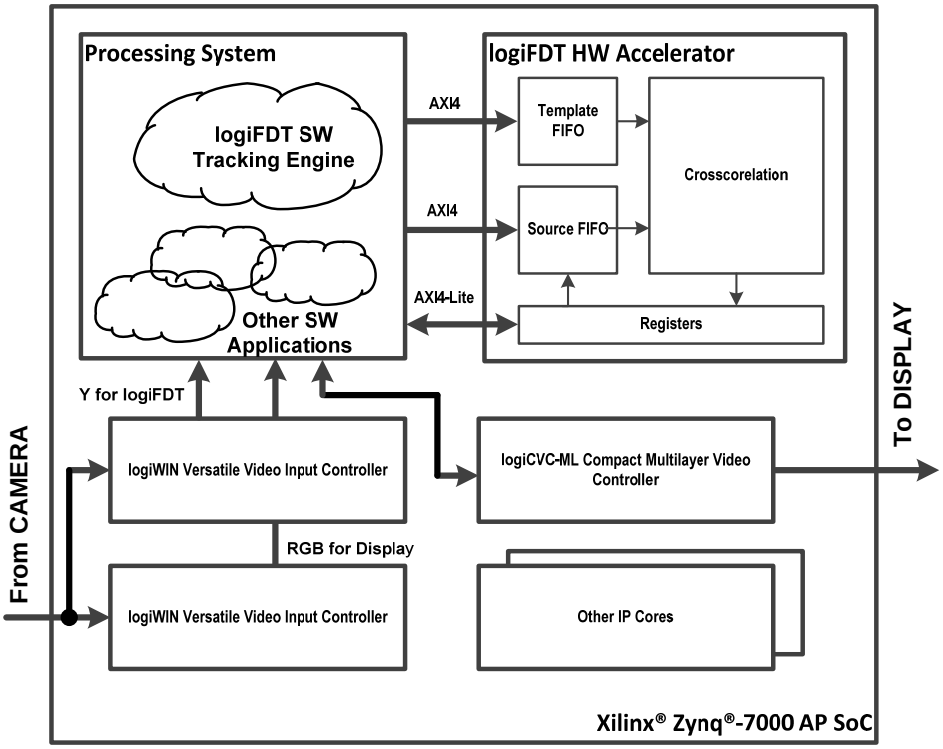

Figure 1: Example SoC Architecture with the Integrated logiFDT IP Core

- Configurable template and source images sizing and array image addressing modes
- Optional templates operational FIFO that allows for overlapping with the software execution and faster face tracking
- Adjustable hardware accelerator's size/performance through the Xilinx tools GUI interface
- Separated ARM AMBA® AXI4 compliant memory interfaces for template and source image fetching
- ARM AMBA AXI4-Lite bus compliant registers interface
- Prepackaged for Xilinx Vivado® Design Suite (IP Integrator) and ISE® Design Suite (XPS)
- Plug-and-play with Xilinx, third-party and other Xylon logicBRICKS IP cores, such as the logiWIN Versatile Video Input IP core for fast and efficient video frame grabbing implementations
- Free downloadable reference for the Embedded Vision Kit from Avnet Electronics Marketing enables full and risk-free evaluation
- IP deliverables include the logiFDT HW acceleration IP, the precompiled library, C API, low-level software driver, documentation and technical support
- Supported and distributed solely by Xylon

Applications

Driver drowsiness and distraction detection (ADAS), video conferencing systems, surveillance identification, biometrics research systems, marketing and retail, assistive technologies for the disabled, games and entertainment (character animation), health, robotics, audio processing and others.

General Description

A human face provides a variety of different communication functions in complex interactions between humans. Beside to identification, humans use head pose and facial expressions during conversation to express emotions, reveal intents, display attention and more. The face detection and tracking is a computer technology that uses video images captured by the video camera to determine and track those distinctive facial features.

The technology significantly improves human-machine interaction and opens a very wide range of applications, such as driver drowsiness detection in automotive safety systems that prevent accidents, speaker detection in video conferencing systems capable to automatically zoom to the current speaker, hands-free interfacing helping disabled people to improve their daily lives, character animations in virtual reality entertainment and gaming, etc.

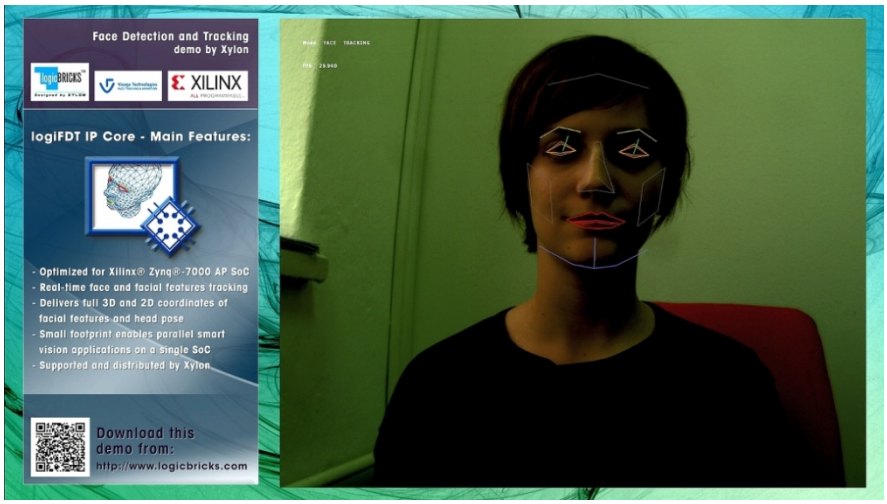

Figure 2: Screenshot from Xylon Demo

Xylon and Visage Technologies AB (http://www.visagetechnologies.com) have entered a technology partnership with the goal of jointly delivering Visage Technologies' state-of-the-art face detection and tracking technology through the Xylon logicBRICKS IP Library. As the result of this partnership, Xylon has designed the logiFDT Face Detector and Tracker IP core optimized for use with Xilinx Zynq-7000 All Programmable SoC (System on Chip). The logiFDT IP core finds and tracks the face and facial features in video sequences in real time and returns full 3D head pose, gaze direction, facial features coordinates and a wealth of other information that can be used in different applications developed on top of it.

Special care has been taken to off-load the processing system and to assure a lot of free programmable logic resources for other IP cores in order to enable parallel execution of other real-time vision and other applications alongside the face detection and tracking in the same Xilinx Zynq-7000 AP SoC. The logiFDT Face Detector and Tracker IP core is carefully partitioned betwen hardware and software to assure the highest performances and optimal utilization of the Zynq-7000 AP SoC resources; i.e complex face tracking algorithms run on a single ARM Cortex-A9 CPU core (Figure 1: logiFDT SW Tracking Engine), while the most used computing intensive per-pixel operations works fully in the on-chip programmable logic (Figure 1: the logiFDT HW Accelerator block).

The logiFDT hardware part is a template matching accelerator that significantly off-loads the processing system and improves the face tracking speed. The accelerator fetches a template (image pattern) and source images from the memory, makes cross-correlation between each corresponding pixel in the template and the source image (Figure 3), and finds the most probable match between the source and the template image. The matching is examined by stepping the template image in one pixel steps (left-right and top-down) over the whole source image.

Figure 3: Pattern Matching – Principle Illustration

Both, software and hardware parts of the logiFDT IP core can be configured differently; i.e. the software can track less facial features at higher speed, the hardware part can use more programmable logic for faster calculations on multiple pixels in a parallel, etc. System designers can leverage this flexibility and adopt the logiFDT IP core regarding speed and precision, overall SoC design and other application requirements.
Figure 1 shows architecture details of the Zynq-7000 AP SoC design used in Xylon's free and downloadable logiREF-FACE-TRACK reference design for the Embedded Vision Kit from Avnet Electronics Marketing:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Face-Detection-for-Zynq-AP-SoC.aspx

The SoC design includes two instances of Xylon's logiWIN Versatile Video Input IP core. One logiWIN IP core does full resolution frame grabbing, color-space conversion, formats and stores video for the display. The other logiWIN IP core scales the video input to the resolution required by the logiFDT SW Tracking Engine and, as it is requested by the face tracking software, generates the single-channel video containing only the Y (luminance) component of the YUV video input. Xylon's logiCVC-ML Compact Multilayer Video Controller IP core displays the camera video overlaid by graphically presented face tracking results (Figure 2).

The logiFDT Face Detector and Tracker IP core is prepackaged for Xilinx Vivado (IP Integrator) and ISE (Platform Studio) Design Suits, requires no skills beyond general tools knowledge and can be used in same ways as Xilinx IP cores. The IP is AMBA AXI4 and AXI4-Lite bus protocol compliant and can be smoothly integrated with other Xylon logicBRICKS, Xilinx or third-party IP cores.

Besides the logiFDT IP core and the related software, Xylon offers technical support, consultancy and design services around the presented product and technology. The logiFDT Face Detector and Tracking IP core is supported and marketed solely by Xylon.

Functional Description

The logiFDT IP core consists of the Face Tracking Engine running on the CPU and the hardware acceleration part consisting of: Template FIFO, Source FIFO, Crosscorelation and Registers.

The Face Tracking Engine offers easy-to-use API for accessing the tracking data on–the-fly during tracking operation. The API description is provided within the documentation delivered with the logiFDT IP core.

The following text is related the hardware acceleration part of the logiFDT Face Detection and Tracking IP core.

Template FIFO

The template (pattern, patch) image data is stored in the external memory (DDRAM) connected to the Xilinx Zynq-7000 AP SoC. The Template FIFO is ARM AMBA AXI4 bus compliant and designed to optimize and increase memory bandwidth utilization.

Source FIFO

The source image data is also stored in the external DDRAM memory. The Source FIFO is ARM AMBA AXI4 bus compliant and designed to optimize and increase memory bandwidth utilization.

Crosscorelation

The Crosscorelation block calculates cross-corelation between template and source images. It starts from the upper left corner of the source image and repeates calculation until the lower right corner (Figure 3). At the end of each calculation step, the block performs normalization and comparsion between the current and the previous calculation result. The determined location and parameters of the highest matching probability are kept in registers.

Registers

The Registers module is accessible through the ARM AMBA AXI4-Lite bus. It includes different registers to enable versatile software control of the hardware acceleration.

Core Modifications

The core is supplied as the precompiled library and an encrypted VHDL format compatible with Xilinx Vivado IP Integrator and ISE Xilinx Platform Studio implementation tools. Different configuration parameters are selectable prior to VHDL core's code synthesis, and the following table presents a list of the available parameters:

Table 2: logiFDT VHDL Configuration Parameters

Parameter	Description
C_TEMPLATE_SIZE	Maximal supported template image size
C_SOURCE_SIZE	Maximal supported source image size
C_PARALLE_CALC	Number of calculations to be performed in parallel
C_NMBR_OF_TEMPLATES	Number of operations in "operation" FIFO

If you wish to adopt the logiFDT IP core to your specific needs and/or to supplement the IP core's features set, you can allow us to modify the source code and tailor the IP core to your requirements.

Core I/O Signals

The logiFDT hardware accelerator I/O signals have not been fixed to any specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Memory Interface		
AXI4 template master interface	Bus	Refer to ARM's AMBA AXI4 specification
AXI4 source master interface	Bus	Refer to ARM's AMBA AXI4 specification
Register Interface		
AXI4-Lite slave interface	Bus	Refer to ARM's AMBA AXI4 specification
Status signals		
interrupt	Output	Interrupt signal port, level sensitive, active high

Verification Methods

The logiFDT is fully supported by the Xilinx Vivado and ISE Design Suites. This tight integration tremendously shortens IP integration and verification. A full logiFDT implementation does not require any particular skills beyond general Xilinx tools knowledge.

The logiFDT evaluation IP core can be downloaded fron Xylon web site and fully evaluated in hardware:

URL: http://www.logicbricks.com/Products/logiFDT.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- Camera systems

Available Support Products

Xylon provides the logiREF-FACE-TRACK free pre-verified reference design to showcase the logiFDT face tracker on the Zynq-7000 AP SoC based MicroZed Embedded Vision Kit from Avnet Electronics Marketing. The reference design contains everything you need to immediately start evaluating and working with the face tracking technology: the SoC design including evaluation logicBRICKS IP cores and hardware design files, software drivers, demo application and documentation.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Face-Detection-for-Zynq-AP-SoC.aspx

The face tracking and other computer vision applications require quality video input. Xylon's logiISP Image Signal Processing Pipeline IP core is a full high-definition ISP pipeline designed for digital processing and image quality enhancements of an input video stream in Smarter Vision embedded designs based on Xilinx Zynq-7000 All Programmable SoC and 7 Series FPGA devices. Free logiREF-VIDEO-ISP pre-verified reference design for the Zynq-7000 AP SoC based MicroZed Embedded Vision Kit from Avnet Electronics Marketing is available from:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/ISP-Pipeline-for-Xilinx-All-Programmable.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: http://www.logicbricks.com/Products/logiFDT.aspx

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.00.	17.10.2014	Xylon pre-release
1.10.	09.12.2014	Initial Xylon release

visage I SDK™ Face Track tracking engine is sourced from Technology Partner Visage Technologies AB.