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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference designs .ucf examples
Reference Designs & Application Notes	Vivado® IP Integrator reference designs
Additional Items	Free reference design for Xilinx ZC702 Evaluation Kit and the ZedBoard™ from Avnet Electronics Marketing SW drivers
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq®-7000 All Programmable SoC, Zynq® UltraScale+™ MPSoC and all Xilinx FPGA families
- Available Linux V4L2 and bare-metal SW drivers
- Supports versatile digital video input formats:
  - ITU656 and ITU1120 (PAL and NTSC)
  - RGB
  - YUV 4:2:2
- Can switch between two video inputs with same or different video formats
- Maximum input and output resolutions are 2048 x 2048 pixels
- Built-in YCrCb to RGB converter, YUV to RGB converter and RGB to YCrCb converter
- Embedded image color enhancements (contrast, saturation, brightness and hue), separately for ITU and YUV video inputs
- Real-time video scale-up (zoom in) up to 64x

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)			LUT[1]	FF[1]	IOB[2]	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
	Mclk	vclk	rclk									
Spartan®-6 (XC6SLX150T-3)	150	150	120	1695	1462	9	0	5	6	0	N/A	ISE14.7
Kintex®-7 (XC7K325T-3)	180	160	120	2195	1856	9	0	2	6	0	N/A	Vivado 2015.3
Zynq®-7000[3] (XC7Z020-1)	180	160	120	1275	1417	9	0	3	6	0	N/A	Vivado 2015.3
Zynq® UltraScale+™ (XCZU9EG-1)	200	160	120	1455	1604	9	0	2	6	0	N/A	Vivado 2016.2

Notes:
1) Assuming the following configuration: ITU656, RGB565 output, 32-bit AXI4-Lite register interface, 64-bit AXI4 memory interface with max. burst size of 64 words, scaling in both directions with multipliers (DSP48s), output stride set to 1024 pixels.
2) Assuming only video inputs are routed off-chip, register and memory interfaces are connected internally.
3) Only burst size of 16 words is supported on HP ports in Zynq-7000 SoC.

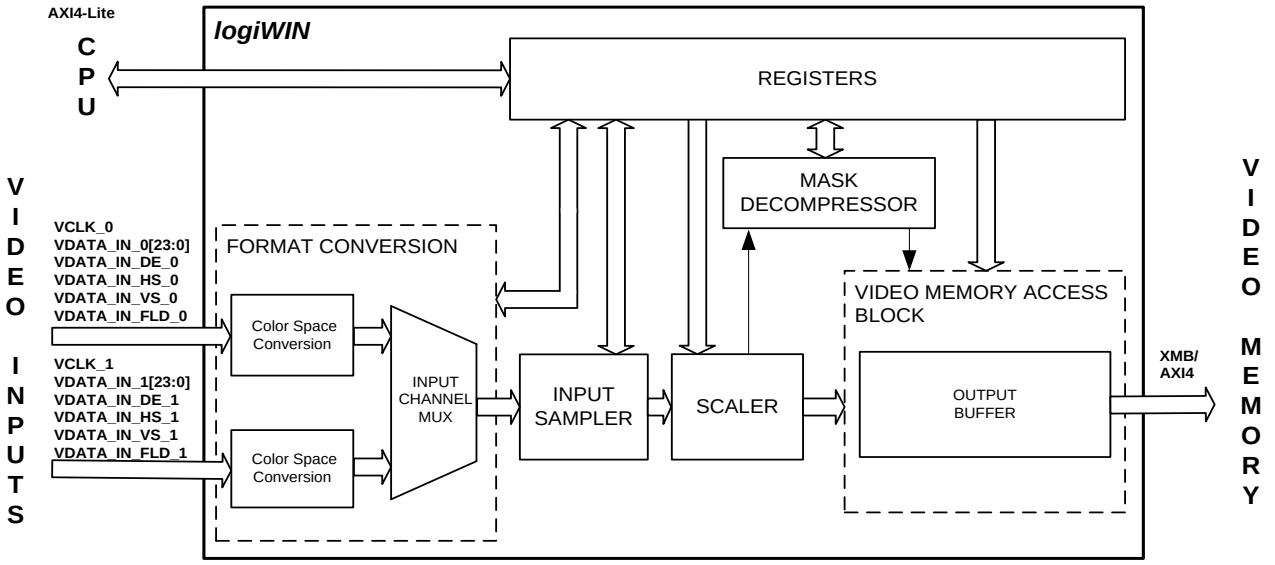

Figure 1: logiWIN Architecture

Features (cont)

- Real-time video scale-down (zoom out) down to 16 times
- Lossless 2x scaling down or 4x in the cascade scaling mode
- Supports video input cropping and smooth image positioning
- ARM® AMBA® AXI4-Lite bus compliant register interface
- Configurable video memory interface: XMB (Xylon Memory Bus) or ARM® AMBA® AXI4
- Compressed stencil buffer in BRAM (mask over output buffer)
- Supports pixel alpha blending – program the alpha channel in the output video stream
- Provides “Bob” and “Weave” de-interlacing algorithms
- Supported Big and Little Endianness memory layout
- Double or triple buffering for flicker-free video
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepared for Xilinx Vivado® IP Integrator (IPI) and ISE® (XPS)* implementation tools
- Free Vivado IPI and ISE XPS reference designs for Xilinx Zynq-7000 AP SoC ZC702 Evaluation Kit
- Plug-and-Play with Xilinx, third-party and other Xylon logicBRICKS IP cores, like the logiCVC-ML (Compact Video Controller with Multilayer Alpha Blending) and logiVIEW Perspective Transformation and Lens Correction Image Processor IP core for complex real-time video processing

** The last available logiWIN IP core version for ISE Design Suite: v4_01_b*

Applications

- Advanced Driver Assistance
- Industrial imaging: Surveillance, Test equipment and Robotics
- Medical Applications
- Aerospace and Defense systems, etc.

General Description

The logiWIN is a frame grabber IP core from the Xylon logicBRICKS™ IP core library optimized for Xilinx All Programmable devices. It is designed to capture video input stream and to give an output video formatted in several digital video formats. The logiWIN IP core functions include scaling, cropping, positioning and masking of the output image by non-rectangular masks. The interlaced PAL/NTSC input video streams can be de-interlaced. The interface to the video memory is designed for SDRAM (SDR, DDR, DDR2, DDR3…) and SRAM frame buffer implemenations. For easier system integration, the logiWIN uses ARM AMBA AXI4 and AXI4-Lite buses, as well as the optional Xylon's proprietary XMB interface. Multiple logiWIN IP core instances enable simultaneous processing of multiple video inputs by a single Xilinx Zynq-7000 AP SoC or FPGA chip.

Standard bussing architecture, software support and IP core deliverables compatible with the Xilinx Vivado and ISE Design Suits, enable developers to implement video frame grabbers in a plug-and-play manner.

Xylon provides a number of free downloadable logicBRICKS reference designs to enable risk-free IP core evaluations and jump-start new developments. For example, the logiREF-MEDIA-ZED pre-verified reference design for the ZedBoard kit demonstrates video frame grabbing, audio recording and playback, and design of Graphics Human Machine Interfaces (HMI) under the Linux operating system:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Multimedia-for-Zynq-AP-SoC-ZedBoard.aspx

Functional Description

The logiWIN internal structure is shown on the block diagram on Figure 1. The logiWIN functional blocks are: Video Input Multiplexer and Formatting Block, Input Sampler, Scaler with Cropping Block, Mask Decompressor, Output Buffer (Memory Address Generator, AXI4/XMB Interface and Double/Triple Buffering) and Registers.

Video Input Multiplexer and Formatting Block

Video Input Multiplexer and Video Input Formatting block (ITU decoder, YCrCb to RGB converter, YUV to RGB converter and RGB to YCrCb converter) are instantiated depending on a number of input channels, nature of the input video stream and the desired video output format.

Input Sampler

The input sampler module samples the input video stream and transfers it into a memory clock domain. Re-sampled data and video memory clock are driven as input to the Scaler block.

Scaler

The Scaler uses the bilinear interpolation for up and down scaling of the input video resolution. The input video can be zoomed in 64 times (scale up 64x), or zoomed out 16 times (scale down 1/16). This scaling range is quite wide, but needs to be carefully used in order to preserve the image quality. The video resolution can be maximally scaled down two times without image quality losses. Further high-quality lossless scaling down is possible in the logiWIN cascade scaling mode.

The Scaler block can also crop the image in both vertical and horizontal direction.

Mask Decompressor

The logiWIN can generate non-rectangular frames from output frame buffers by means of an optional compressed stencil programmed in the BRAM memory. The stencil's masking image is compressed with the Run-Length Encoding algorithm (RLE).

Output Buffer

The Output Buffer sub-block packs output data and bursts them towards external SDRAM or SRAM memories. It consists of three main parts: Memory Address Generator, Xylon Memory Bus (XMB) interface, and a part that handles the double/triple buffering.

The Memory Address Generator can be configured to store odd and even video image lines of the interlaced video input (ITU656 or ITU1120) to different, or to the same memory addresses. That can be used for de-interlacing algorithms. Otherwise, odd and even fields are stored at the same address.

The logiWIN implements the double or the triple frame buffering to prevent video flicker, shearing, and tearing artifacts.

logiWIN Registers

All logiWIN registers arre instantiated in this block. The CPU has access to all these registers through the AXI4-Lite bus.

Core Modifications

The core is supplied in an encrypted VHDL format which allows the user to take a full control over configuration parameters. Table 2 outlines the most important logiWIN configuration parameters selectable prior to the VHDL synthesis. For a complete list of parameters, please consult the logiWIN User's Manual delivered with the IP core.

Table 2: logiWIN VHDL Configuration Parameters

Parameter	Description
C_NUM_OF_INPUTS	Number of video inputs
C_INPUT_0_TYPE	Channel 1 video input type: ITU, RGB or YUV
C_INPUT_1_TYPE	Channel 2 video input type: ITU, RGB or YUV
C_ITU_TYPE	ITU video input type: ITU656 or ITU1120
C_ITU_BITS	Number of ITU bits. Valid values are 8 bits or 10 bits
C_YUV_BITS	Number of YUV bits. Valid values are 8 bits or 16 bits
C_OUTPUT_TYPE	Video output type: RGB565, RGB888, ARGB6565, ARGB8888, YCrCb
C_USE_COLOR_MANAGEMENT	Includes or excludes color enhancement module for ITU or YUV input
C_CONVERTER_USE_MULTIPLIER	Defines type of multipliers in color space converters
C_CASCADE_ON	Enables cascaded scaling for lossless scale-down operations
C_USE_XSCALE	Horizontal scaling implementation on/off
C_USE_YSCALE	Vertical scaling implementation on/off

The logiWIN has been constructed with regard to adaptability to various cameras and other video input sources. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiWIN core or to supplement some of your specific functions, you can order the source code or allow us to tailor the logiWIN to your requirements. The logiWIN source code is available at additional cost from Xylon.

Core I/O Signals

The core I/O signals have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Memory Interface		
AXI4 Master Interface	Bus	Refer to ARM AMBA AXI4 specification
XMB Interface	Bus	Xylon Memory Bus. Refer to logiMEM specification
Register Interface		
AXI4-Lite Slave Interface	Bus	Refer to ARM AMBA AXI4 specification
Video Input Signals		
vclk_in	Input	Video input clock used for both channels if C_USE_EXT_CLOCKING = 1
vclk_in_sel	Output	Video input clock select, controlled by bit 4 in control register
vclk_0	Input	Channel1: video input clock
vdata_in_0[23:0]	Input	Channel1: video input data: • RGB[7:0] is blue color, RGB[15:8] is green color and RGB[23:16] is red color component • for 8-bit ITU656 input type only 7:0 is in use • for 10-bit ITU656 input type only 9:0 is in use • for 8-bit ITU1120 input type, 7:0 is in use for luma components (Y), while 15:8 is in use for chroma components (CrCb) • for 10-bit ITU1120 input type, 9:0 is in use for luma components (Y), while 19:10 is in use for chroma components (CrCb) • for 8-bit YUV 4:2:2 input type only 7:0 is in use • for 16-bit YUV 4:2:2 input type, 7:0 is in use for luma component (Y), while 15:8 is in use for chroma components (CrCb).
vdata_in _de_0	Input	Channel1: data enable (use only for RGB and YUV input types)
vdata_in _hs_0	Input	Channel1: vsync (use only for RGB and YUV input types)
vdata_in _vs_0	Input	Channel1: hsync (use only for RGB and YUV input types)
vdata_in _fld_0	Input	Channel1: field (use only for RGB and YUV input types)
vclk_1	Input	Channel2: video input clock
vdata_in_1[23:0]	Input	Channel2: video input data: • RGB[7:0] is blue color, RGB[15:8] is green color and RGB[23:16] is red color component • for 8-bit ITU656 input type only 7:0 is in use • for 10-bit ITU656 input type only 9:0 is in use • for 8-bit ITU1120 input type, 7:0 is in use for luma components (Y), while 15:8 is in use for chroma components (CrCb) • for 10-bit ITU1120 input type, 9:0 is in use for luma components (Y), while 19:10 is in use for chroma components (CrCb) • for 8-bit YUV 4:2:2 input type only 7:0 is in use • for 16-bit YUV 4:2:2 input type, 7:0 is in use for luma component (Y), while 15:8 is in use for chroma components (CrCb).
vdata_in _de_1	Input	Channel2: data enable (use only for RGB and YUV input types)
vdata_in _hs_1	Input	Channel2: vsync (use only for RGB and YUV input types)
vdata_in _vs_1	Input	Channel2: hsync (use only for RGB and YUV input types)
vdata_in _fld_1	Input	Channel2: field (use only for RGB and YUV input types)
Auxiliary Signals		
curr_vbuff[1:0]	Output	Triple buffering: current video memory buffer
next_vbuff[1:0]	Input	Triple buffering: next video memory buffer to write to
sw_ vbuff _req	Output	Triple buffering: request for buffer switching
sw_ vbuff _grant	Input	Triple buffering: buffer switching granted
fifo_error	Output	Active (logic high) when any of the FIFOs error occurs. Remains active until vertical synchronization signal arrives
capture_stop	Input	Image capture stop signal
Interrupt	Out	Interrupt signal, level sensitive, active high

Verification Methods

The logiWIN is fully supported by the Xilinx Vivado (IPI) and ISE (XPS) Design Suits. This thight integration tremendously shortens IP integration and verification. A full logiWIN implementation does not require any particular skills beyond general Xilinx tools knowledge. The IP core version packaged for the Xilinx Vivado Design Suit is shipped with compiled simulation libraries for ModelSim simulator from Mentor Graphics. For information about Vivado compatible IP core simulations, please contact Xylon.

The logiWIN evaluation IP core can be downloaded from Xylon web site and fully evaluated in hardware:

http://www.logicbricks.com/Products/logiWIN.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

The pre-verified logiREF-MEDIA-ZED reference design presents logicBRICKS IP cores for multimedia processing under the Linux operating system running on the Xilinx Zynq-7000 AP SoC based ZedBoard Development Kit from Avnet Electronics Marketing. It demonstrates video frame grabbing, audio recording and playback and HMI implementations, and includes the following Linux software drivers and libraries: Advanced Linux Sound Architecture (ALSA), Video4Linux2, Linux Framebuffer driver, Xylon QPA 2D plugin for 2D accelerated Qt application framework and the OpenGL® ES 1.1 API:

URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Multimedia-for-Zynq-AP-SoC-ZedBoard.aspx

The logiWIN V4L2 software driver enables Linux software designers to program video frame grabbing applications with no need to know anything about the underlying hardware. To learn more and get the driver, please visit:

URL: http://www.logicbricks.com/Products/Xylon-Video4Linux-logiWIN-Driver.aspx

logiREF-VROT-FMC Reference Design works on the ZedBoard Development Kit from Avnet Electronics Marketing. Built with standard evaluation logicBRICKS IP cores, this demo showcases real-time low latency video input rotation. Graphic touchscreen HMI allows for dynamic changes of an angle of rotation in sub-degree steps. The video rotation works with no help from the processing system and can be also used in Xilinx FPGAs.

Email: support@logicbricks.com
URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Low-Latency-Video-Rotation-for-Xilinx-SoC-FPGA.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
2.02.	12.03.2009.	Initial Xylon release – new doc template.
2.03.	27.03.2009.	Added VCLK_IN and VCLK_IN_SEL signals to the Table 3: Core I/O Signals.
2.05.	15.03.2010.	Updated Table 1 and Table 3.
2.05.	06.04.2010.	New doc template.
2.06.	07.07.2010.	Document name changed.
2.07.	31.12.2010.	Added RGB to YCrCb converter to Features and Figure 1: logiWIN Architecture.
3.01	23.11.2011.	Added YUV 4:2:2 input, including YUV to RGB converter and color enhancement block. Added AXI4 Master interface for memory access and AXI4-Lite Slave interface for registers.
3.02	17.07.2012.	Byte swapping option added for register and memory bus interface. Endianness correction removed for registers layout. Color format order in output pixel format selectable between: ARGB and ABGR, as well as between CrY2CbY1 <-> Y2CrY1Cb.
4.00	29.01.2014.	Removed OPB and PLB busses. Added field signal on both video inputs.
4.01	23.09.2014.	Updated Table 1 and Table 3. Added capture_stop input signal. Added fifo_error output signal. Added default register settings. Scaler module optimized for better routing.
4.1	26.11.2014.	IP core version naming convention modified for Vivado IP-XACT package compliance. Patch level designation is replaced by IP core's revision tag.
4.2	30.10.2015.	Corrected description of C_YUV_BITS generic parameter in Table 2 Corrected input signals' description in Table 3. IP core prepared for Vivado 2015.2.
4.2	26.10.2016.	Added utilization information for Zynq® UltraScale+™ XCZU9EG-1 MPSoC. Updated Table 1.

