Proposal for future Physical Layer M-Bus

A) Electrical Requirements Slave

I) Static requirements

1.) Master to Slave voltages

a) Maximum permanent voltage: -50V...0V...+50V (no damage)
b) Voltage range for meeting all specifications: +-(12V..42V)
c) Bus voltage at the slave terminals in mark-(quiescent) state of master slave communication (=UMark) shall be +-(21..42V) . The mark voltage shall be stored by a voltage maximum detector with an asymmetric time constant. The discharge time constant shall be greater than 30*(charge constant) but less than 1s. The stored voltage maximum UMark may drop in 50ms by not more than 0.2V for all voltages between 12V and UMark.
d) Bus voltage Mark/Space state for master slave communication
Space: UBus< UMark-8.2V
Mark: UBus >= UMark-5.7V
Maximum space state time 50ms
Maximum space state duty cycle: 0.92

2.) Quiescent slave bus current (Mark-Send-State)

Definition 1UL (unit load)=1.5mA

a) Bus current IMark <=1UL.
b) Variation over bus voltages of +-(12V..42V): <0.2% of 1UL/V.
c) Short term variation: <= +-1%/10s.
d) Long term variation over allowed temperature range of slave device: <10%.
e) Bus current for any single semiconductor defect: <100mA.

3.) Startup current

a) Slow start

For any bus voltage in the range of 0..+-42V the bus current shall be

limited to <= 1 UL.

b) Fast change

After any bus voltage change the bus current shall be <=1UL within

1ms.

4.) Space-Send current

The bus current for a slave space state send shall be higher by 11..20mA than in the mark state for all allowed bus voltages:
ISpace=IMark+(11..20)mA.

5.) Input capacitance at the slave terminals

<= 0.5nF.

This capacitance shall be measured with a DC-bias of (15-30)V.

6.) Startup delay

In case of a bus voltage drop below 12V for longer than 0.1s the recovery time after applying an allowed mark state voltage until reaching full communication capabilities shall be less than 3s.

7.) Multiple Unit-Loads

A slave device may require a max. mark current of multiple (N) unit loads if it meets all requirements for a parallel connection of N terminal device with 1 UL each. Each terminal device shall be marked with the unit load number N (If >1) and the device description shall contain a note on the multiple unit loads for this device.

8.) Optional reversible mains protection

The slave interface can be equipped with an optional reversible mains protection. This guarantees that even for a prolonged period (test duration: 1min) the slave interface can withstand mains voltages of 230V (-15%.. +10%) and 50Hz or 60Hz and that afterwards all specifications are met again. This mains protection function is recommended for all mains operated terminal devices.

9.) Galvanic Isolation

The isolation resistance between any bus terminal and all metal parts acces- sable without violating seals shall be >1MOhm. Excluded are terminals for the connection of other floating or isolated external components. The test voltage is 500V. For mains operated terminal devices the appropriate safety rules apply.

II) Dynamic requirements

Any link layer or application layer protocol of up to 38 400 Baud is acceptable if it guarantees that a mark state is reached for at least one bit time at least once in every 11 bit times and not later than after 50ms. Note that this is true for any asynchronous protocol with 5-8 databits and with or without a parity bit for any baudrate of at least 300 baud, including a break signal of 50ms. It is also true for many synchronous protocols with or without bit coding.

B) Electrical Requirements Master

I) Definition

1.) Characterizing parameters

a) Max. current IMax

A master for this physical layer is characterized by its maximum current IMax. For all bus currents between zero and IMax it shall meet all functional and parametric requirements. For a maximally loaded segment with up to 250 slaves with 1 UL each (375mA) plus an allowance for one slave with a short circuit (+100mA) plus the maximum space send current (+20mA) an IMax >= 0.5A is required.

b) Max. voltage drop Ur

The max. voltage drop Ur is defined as the minimum space state voltage minus 12V. Ur divided by the maximum segment resistance gives the maximum usable bus current for a given combination of segment resistance and master.

c) Max. baudrate BMax

Another characterisation of a master is the maximum baud rate BMax up to which all specifications are met. The minimum baudrate is always 300 Baud.

2.) Function Types

a) Simple Level Converter

The master function can be realized as a logically transparent level converter between the M-bus physical layer and some other standar-dized physical layer (e.g.V24). It is then bit transparent for all allowable baudrates of 300..BMax. No bit time recovery is

possible.
Hence a simple level converter can not be used as a repeater.

b) Intelligent level converter

An intelligent level converter can perform space bit time recovery for any asynchronous byte protocol at its maximum baudrate IMax. Other baudrates IMax/L (L=2..LMax) are allowed, but bit time recovery can not be guaranteed for these other baudrates. Such a level converter can be used as a physical layer repeater for its maximum baudrate.

c) Bridge

The master function can be integrated with a link layer unit thus forming a (link layer) bridge. If this bridge can support the required physical and link layer management functions it can support also multiple baudrates.

d) Gateway

The master function can be integrated into the application layer of a gateway or it can be fully integrated into an application.

II) Requirements

1.) Mark- (quiescent state)- voltage for currents between 0..IMax
UMark= (24V+Ur)..42V

2.) Space- (signal state)-voltage
USpace <UMark-12V, but >=12V+Ur

3.) Bus short circuit

Reversible automatic recovery to full function not later than 3s after the end of any current higher than IMax. 1ms after the beginning of a short circuit situation the bus current shall be limited to <3A.

4.) Minimum voltage slope

The transition time between space state and mark state voltages from 10% to 90% of the steady state voltages shall be <=1/2 of a nominal bit time. The
asymmetry of these transition times shall be <=1/8 of a nominal bit time.

Test conditions

a) Baudrate 300 Baud CLoad= 1.5µF:
b) Baudrate 2400 Baud CLoad=1.2µF
c) Baudrate 9600 Baud: CLoad=0.82 µF
d) Baudrate 38400 Baud: CLoad= 0.39 µF

5.) Effective source impedance

Voltage drop of the bus voltage for a short (<50ms) increase of the bus current by 20mA: <=1.2V.

6.) Hum, ripple and short term stability (<10s) of the bus voltages

< 200mV peak to peak.

7.) Data detection current (Reception from slave current pulses)

Bus current <=Bus idle current + 6mA: Mark state receive
Bus current >=Bus idle current + 9mA: Space state receive
Measurement with current pulses of <50ms, duty cycle <0.92

8.) Reaction at large data currents (collision)

If for a duration of >(2-22) bit times the momentary bus current is greater than the quiescent current+25mA, the master may, for bus currents >= quiescent current+50mA the master has to emit to the bus a break signal (bus voltage =USpace) with a duration of >= 22 bit times but less than 50ms. To the user side this state should also be signalled with a break signal of equal duration. If the bus current is > IMax, the master may switch off the bus voltage completely. Note that for switch off times >100ms the minimum recovery time of 3s shall be taken into account.

9.) Ground symmetry

For mains powered masters or masters with connection to ground based systems (e.g. connection to the V24 port of a mains powered PC) the static
and dynamic bus voltages shall be symmetric (40-60%) with respect to ground.

C) Electrical Requirements Mini-Master

I) Definition

A Mini-Master can be used ins systems which can accept the following restrictions:

1.) Maximum wiring length of its segment: <=50 m.
2.) Maximum baudrate: 2400 baud.
3.) No function required if any device fails with overcurrent.
4.) No automatic search for secondary adresses (collision mode) required.

A Mini-Master can be implemented as a simple level converter to some other standardized physical layer interface (e.g..V24) or it can be integrated into a data processing device. It usually can not be used as a repeater. It can be implemented as a stationary or as a portable device. It can be powered from mains or it can be battery powered.

II) Requirements

A Mini-Master has the following reduced requirements as compared to a full standard master:

1.) Minimum transition slopes

For a load capacitance of 75nF: Transition time between mark and space state voltages in both directions between 10% and 90% of the voltage step of the two static signal voltages: Maximum transition time tmax <=50µs.

2.) Behaviour at higher data currents (collision):

No requirements

3.) Ground symmetry: No requirements

D) Inductively coupled Micro Master

It is possible to realize a micro master with an open inductive coupler consisting of a stationary secondary (bus) side without a power supply and an inductive readout head. If slaves with a reduced maximum additional space state current (=<6mA instead of <= 20mA) are used, up to 3 slaves can be connected. For details see appendix X.

E) Requirements for Repeaters

I) General

A physical layer repeater shall meet at its slave side all requirements for a slave and at its master side all requirements of a master.

II) Additional

1.) Isolation

The bus terminals at the master side shall be isolated from the bus terminals
at the slave side. The isolation resistance shall be >=1MOhm for the test voltage of 500V. Any pertinent safety regulations for mains powered devices (e.g. VDE 0884 or others) shall be considered.

2.) Bit recovery

Incoming data bytes with acceptable bit time distortions for a reception according to the requirements of the link layer used shall be transmitted at the other side in such a way that all the timing requirements of the link layer are met.
A repeater may therefore be restricted to certain baudrate(s) or may be

restricted to certain byte formats or link layers.

F) Cable Installation

According to measurements at the University of Paderborn, the following segment types will ensure safe physical layer communication. A cabling of either a shielded (4*0.8mm diam./0.5mm²) telephone type or a standard mains type (1.5mm²) have been investigated. For telephone cabling with 0.6mm diameter wires either the maximum distance or the maximum number of devices has to be halved.

Type A: Small in house installation

Description:

distance (resistive cable length) <=350 m
total length of segment wiring: <=1 km
cable type: telephone type, 0.8mm diam. shielded

copper cross section 0.5mm², resistance < 30 Ohm
Usage:

a) Max. device number: max. 250 Unit Loads @9600 Baud
b) Max. speed: max. 64 Unit Loads @38400 Baud

Type B: Large in house installation

Description:

distance (resistive cable length) <=350 m
total length of segment wiring: <=4 km
cable type: telephone type, 0.8mm diam. shielded

copper cross section 0.5mm², resistance < 30 Ohm
Usage:

a) Max. device number: max. 250 Unit Loads @2400 Bd
b) Max. speed: max. 64 Unit Loads @9600 Bd

Type C: Small wide area net

Description:

distance (resistive cable length) <=1km
total length of segment wiring: <=4 km
cable type: telephone type, 0.8mm diam. shielded

copper cross section 0.5mm², resistance < 90 Ohm

Usage: max. 64 Unit Loads @2400 Bd

Type D: Large wide area net

Description:

distance (resistive cable length) <=3km
total length of segment wiring: <=5 km
cable type: mains, 1.5mm² resistance < 90 Ohm

Usage: max. 64 Unit Loads @2400 Bd

Type M: Mini installation

Description:

distance (resistive cable length) <=50 m
total length of segment wiring: <=50m
cable type: telephone type, 0.8mm diam. shielded

copper cross section 0.5mm², resistance < 5 Ohm
Usage: max. 16 Unit Loads @2400 Bd