

Features

- Integrates Image Reject (Balanced) Mixer, LO Buffer, LO Quadrupler and RF Buffer
- 13 dB Conversion Gain
- +20 dBm Input Third Order Intercept (IIP3)
- -30 dBm (4x) LO Leakage (@ RF Port)
- 18 dBc Image Rejection
- Variable Gain with Adjustable Bias
- Lead-Free 4 mm, 24 Lead QFN Package
- RoHS[^] Compliant

Description

The MAUC-011009 is an integrated up-converter that has a typical conversion gain of 13 dB, and an image rejection of 18 dBc. The device includes a LO quadrupler, LO buffer amplifier, and RF buffer amplifier. Variable gain can be achieved by adjusting the bias, with turn-down trajectories optimized to maintain linearity and 4xLO leakage over the gain control range. The output IP3 is 32 dBm at maximum gain.

The MAUC-011009 is ideally suited for 38 GHz band point-to-point radios under both LSB and USB operation.

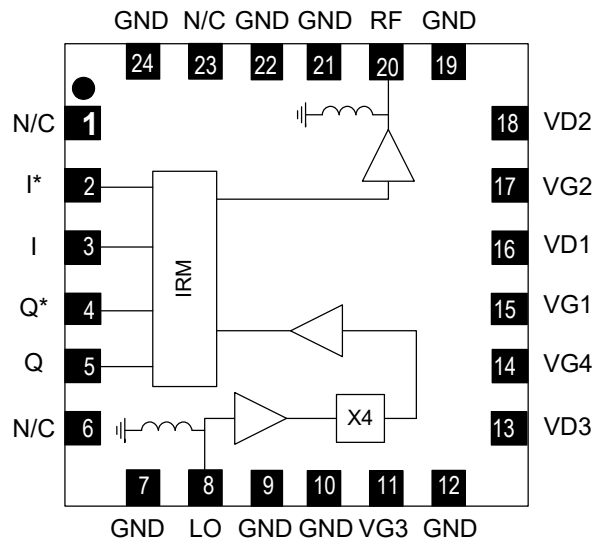
Each device is 100% RF tested to ensure performance compliance.

Ordering Information^{1,2}

Part Number	Package
MAUC-011009-TR0500	500 Piece Reel
MAUC-011009-000SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

Functional Schematic



Pin Configuration³

Pin No.	Function	Pin No.	Function
1	N/C	13	VD3
2	I*	14	VG4
3	I	15	VG1
4	Q*	16	VD1
5	Q	17	VG2
6	N/C	18	VD2
7	GND	19	GND
8	LO	20	RF
9	GND	21	GND
10	GND	22	GND
11	VG3	23	N/C
12	GND	24	GND
		25	Paddle ⁴

3. MACOM recommends connecting all N/C (no connection) package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

[^] Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Up Converter 37 - 40 GHz

Rev. V2

Electrical Specifications⁵:

LO = 0 dBm, IF = -10 dBm, T_A = +25°C

V_{D1} = V_{D2} = V_{D3} = 4 V, I_{D1} = 45 mA, I_{D2} = 135 mA, I_{D3} = 200 mA

Parameter	Units	Min.	Typ.	Max.
Frequency Range (RF)	GHz	37	—	40
Frequency Range (LO)	GHz	8.375	—	10.875
Frequency Range (IF)	GHz	DC	—	3.5
LO Input Power (PLO)	dBm	—	0	—
USB Conversion Gain (IF = 3.5 GHz)	dB	9.5	13	—
Image Rejection	dBc	—	18	—
Input IP3 (P _{IN} = -10 dBm/tone, IF = 3.5 GHz, ΔIF = 10 MHz)	dBm	—	19	—
USB Output IP3 (P _{IN} = -10 dBm/tone, IF = 3.5 GHz, ΔIF = 10 MHz)	dBm	28	32	—
Spurious (4xLO) [tuned - IF voltages ~ 0.2 V]	dBm	—	-30	—
Spurious (1xLO)	dBm	—	-70	—
RF Return Loss	dB	—	10	—
LO Return Loss	dB	—	15	—
IF Return Loss	dB	—	15	—
Current, Drain 1 (I _{D1})	mA	—	45	—
Current, Drain 2 (I _{D2})	mA	—	135	—
Current, Drain 3 (I _{D3})	mA	—	200	—
Gate Voltage (V _{G4})	V	—	-3.25	—
Gate Current (I _{G4})	mA	—	-1	—

5. Apply gate voltages prior to drain voltages. Adjust V_{G1}, V_{G2} and V_{G3} between -1.0 and -0.1 V to achieve specified drain current. Typical current 380 mA = 45 (I_{D1}) + 135 (I_{D2}) + 200 (I_{D3}) mA. Refer to App Note [1] for biasing details.

Absolute Maximum Ratings^{6,7}

Parameter	Absolute Max.
Drain Voltage	+4.3 V
Gate Bias Voltage ($V_{G1,2,3}$)	$-1.5 \text{ V} < V_G < +0.3 \text{ V}$
Gate Bias Voltage (V_{G4})	$-4.0 \text{ V} < V_G < 0 \text{ V}$
Input Power	10 dBm
LO Input Power	13 dBm
Storage Temperature	-55°C to $+150^{\circ}\text{C}$
Operating Temperature	-40°C to $+85^{\circ}\text{C}$
Junction Temperature ⁸	$+150^{\circ}\text{C}$

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Junction Temperature (T_J) = $T_C + \Theta_{jc} * (V * I)$
Typical thermal resistance (Θ_{jc}) = $36^{\circ}\text{C}/\text{W}$.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Biasing Quickstart

Turn ON:

- Step 1: Turn on the fixed voltage on VG4 first.
- Step 2: Turn on VG1, VG2 and VG3 at approximately -1.0V .
- Step 3: Turn on IF voltages at the fixed voltage.
- Step 4: Turn on VD1, VD2 and VD3 at the fixed voltages, and adjust corresponding VG to get the required current levels.

Turn OFF:

Reverse steps indicated in **Turn ON** sequence

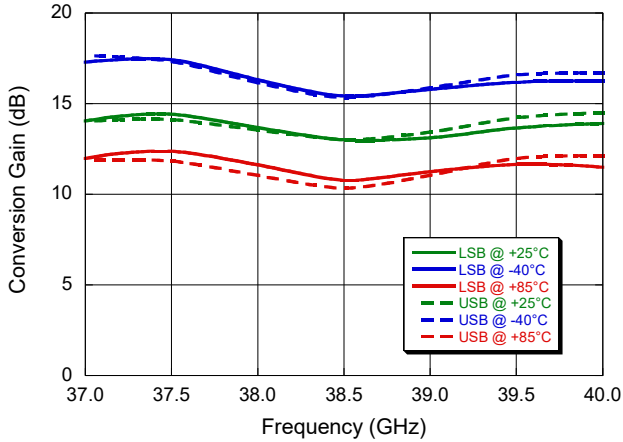
For further details please see App Note [1]

Up Converter 37 - 40 GHz

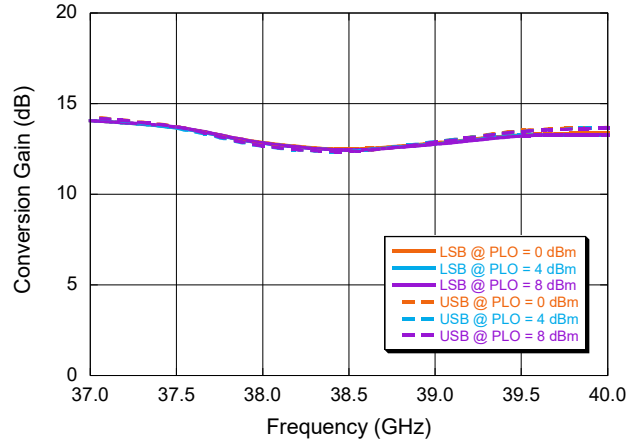
Rev. V2

Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, P_{DC} = 1.52 W

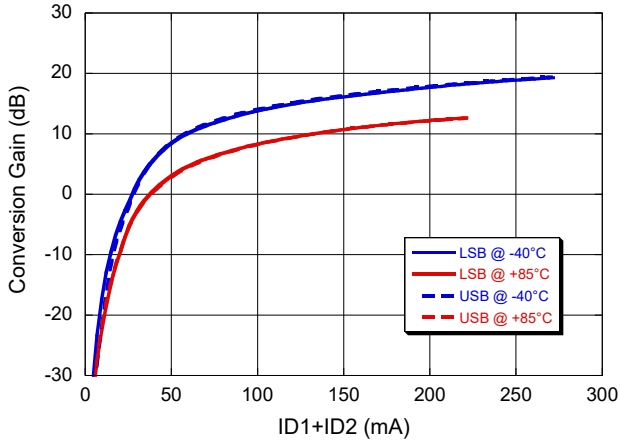
Conversion Gain



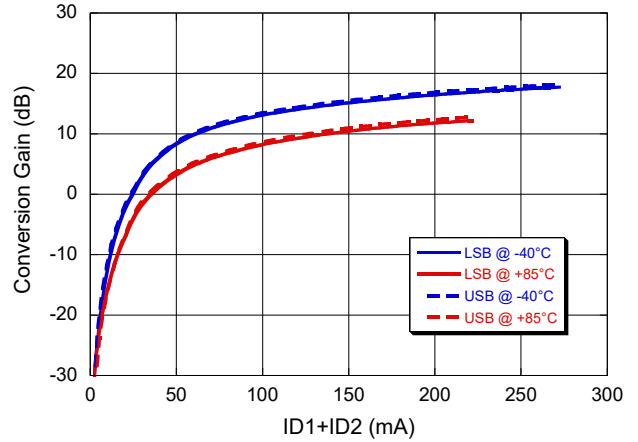
Conversion Gain, LO Power swept



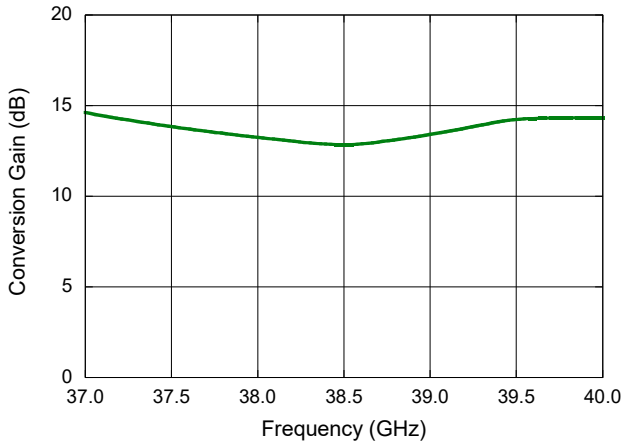
Conversion Gain @ 37 GHz



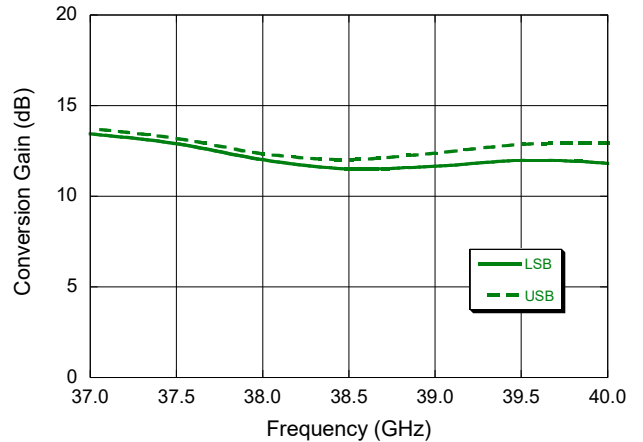
Conversion Gain @ 40 GHz



Conversion Gain @ IF = 21.4 MHz



Conversion Gain @ IF = 3.5 GHz

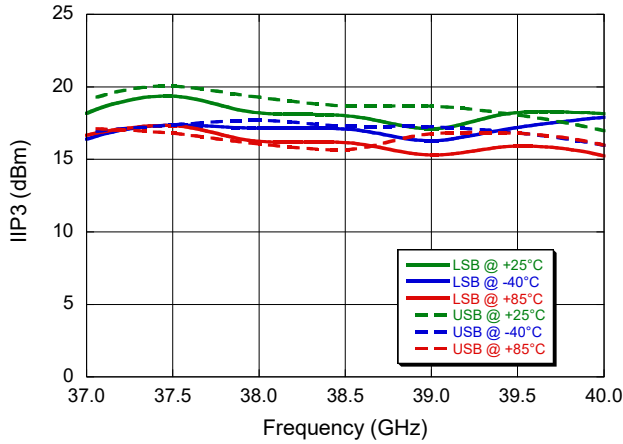


Up Converter 37 - 40 GHz

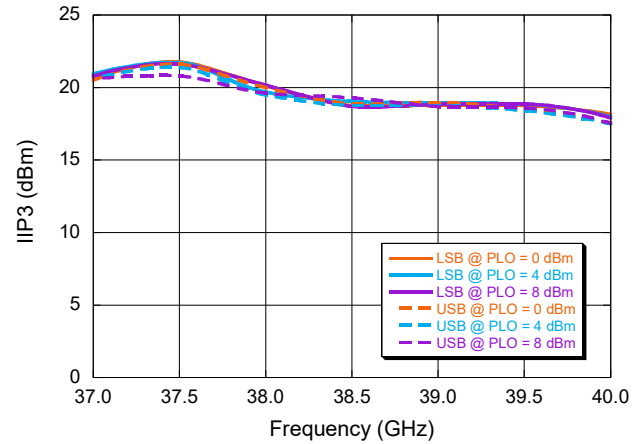
Rev. V2

Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, P_{DC} = 1.52 W

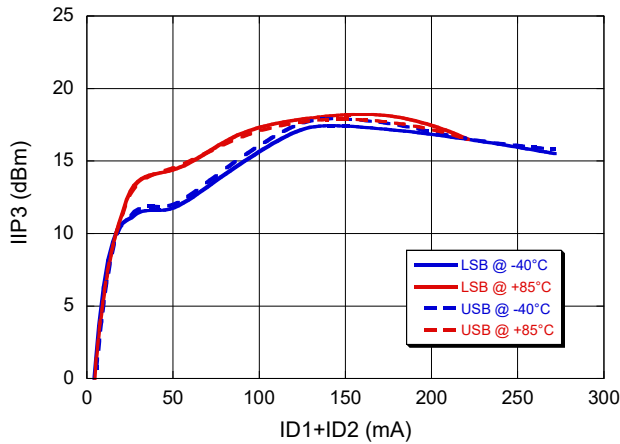
Input IP3



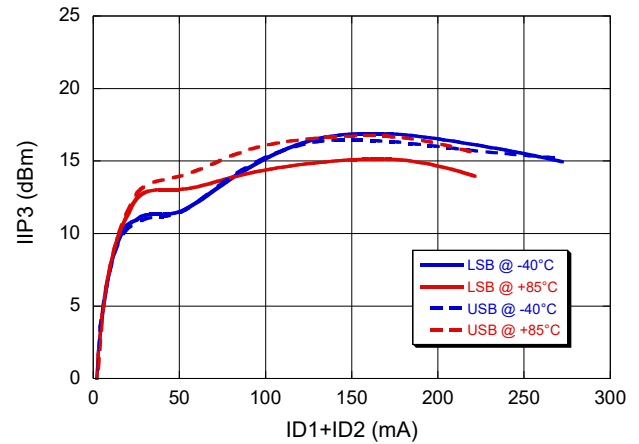
Input IP3, LO Power swept



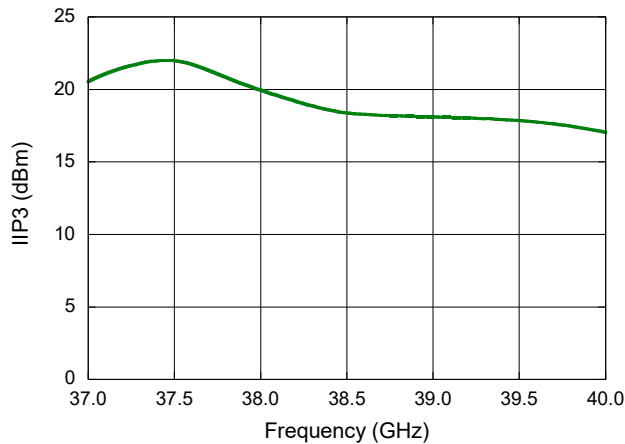
Input IP3 @ 37 GHz



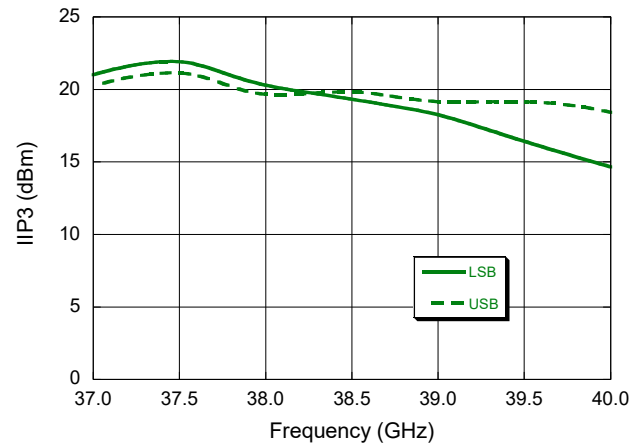
Input IP3 @ 40 GHz



Input IP3, IF = 21.4 MHz



Input IP3, IF = 3.5 GHz

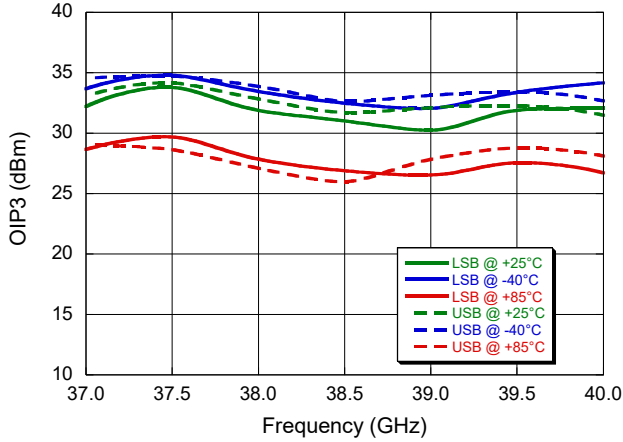


Up Converter 37 - 40 GHz

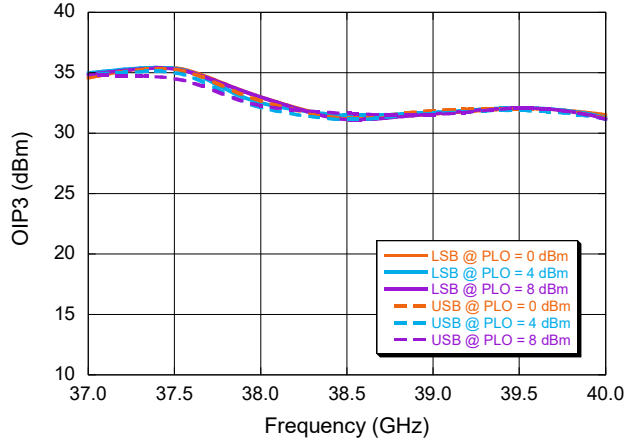
Rev. V2

Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, P_{DC} = 1.52 W

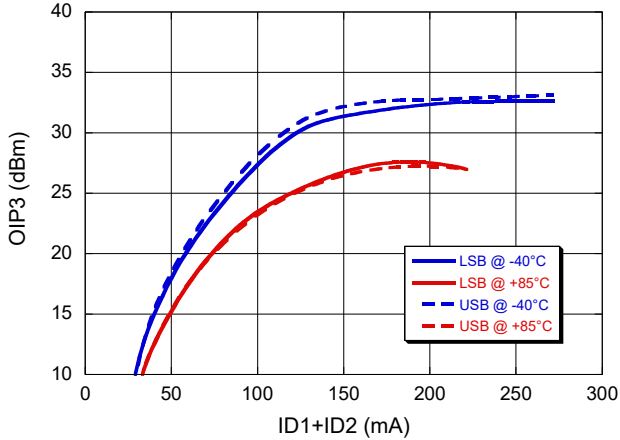
Output IP3



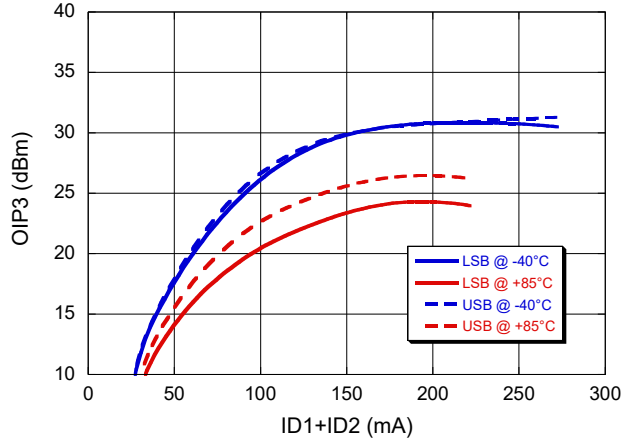
Output IP3, LO Power swept



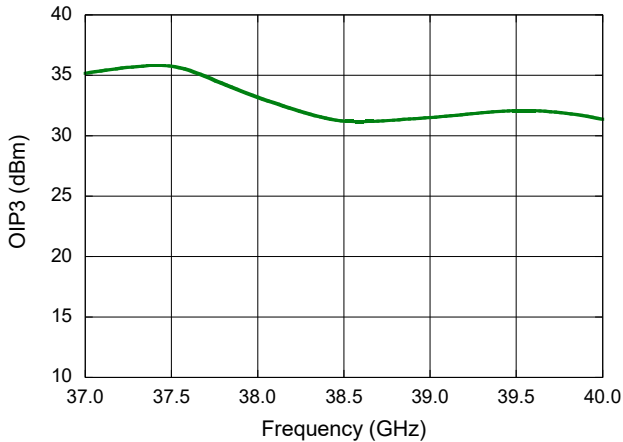
Output IP3 @ 37 GHz



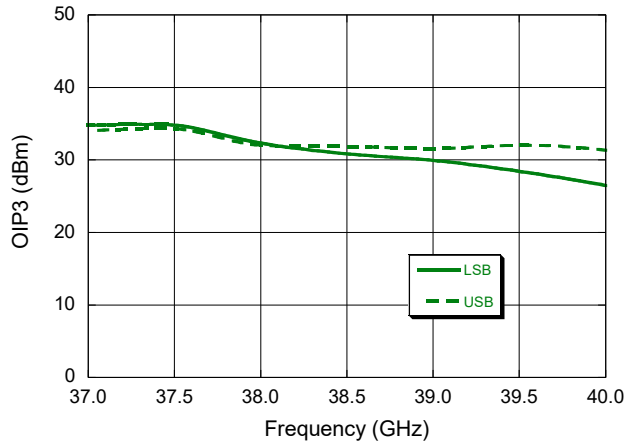
Output IP3 @ 40 GHz



Output IP3, IF = 21.4 MHz



Output IP3, IF = 3.5 GHz

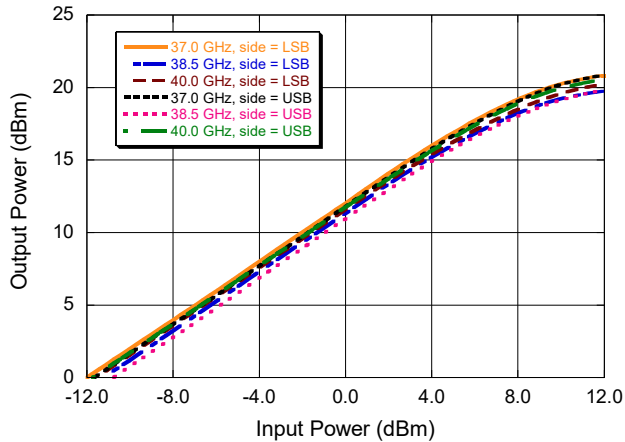


Up Converter 37 - 40 GHz

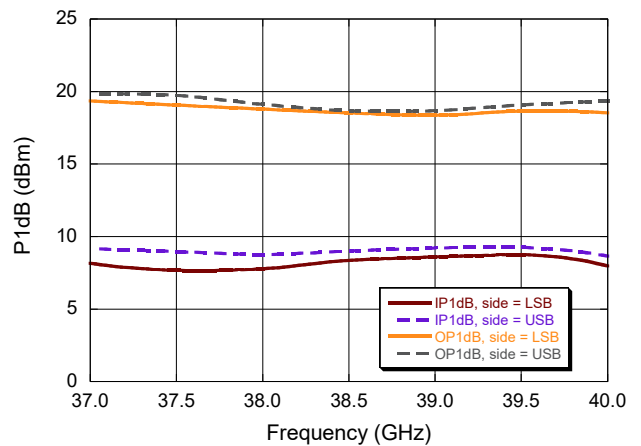
Rev. V2

Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, P_{DC} = 1.52 W

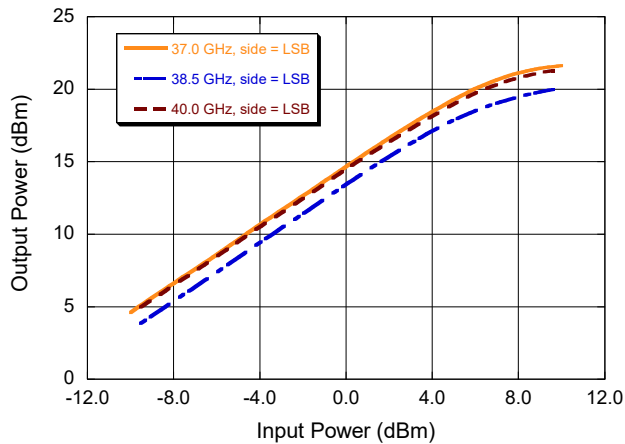
P_{OUT} vs. P_{IN}



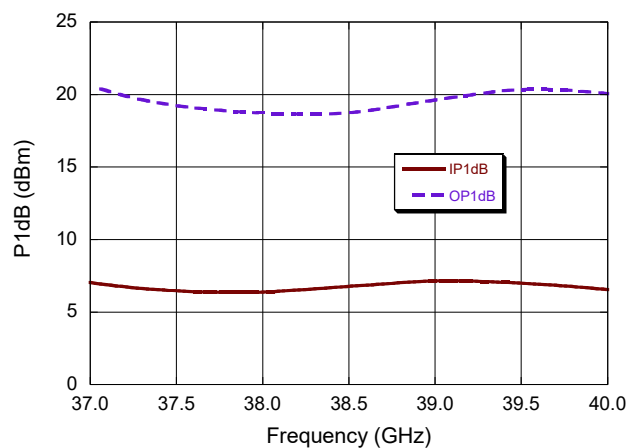
P1dB, Input & Output



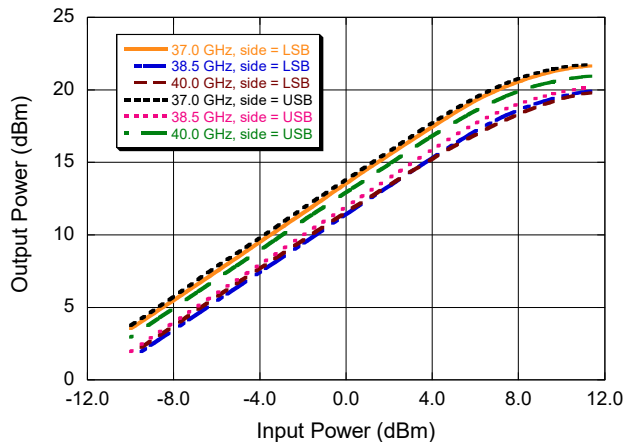
P_{OUT} vs. P_{IN} @ IF = 21.4 MHz



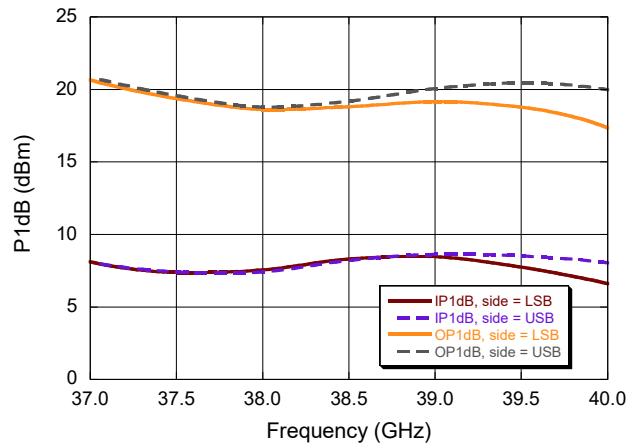
P1dB @ Input & Output, IF = 21.4 MHz



P_{OUT} vs. P_{IN} @ IF = 3.5 GHz



P1dB @ Input & Output, IF = 3.5 GHz



Up Converter 37 - 40 GHz

Rev. V2

Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, P_{DC} = 1.52 W

Image Rejection

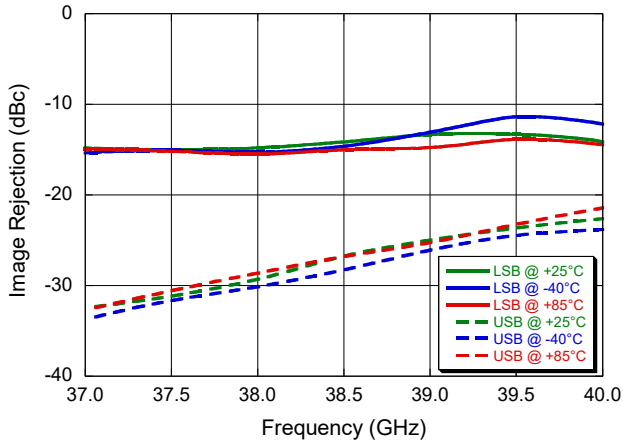


Image Rejection, LO Power swept

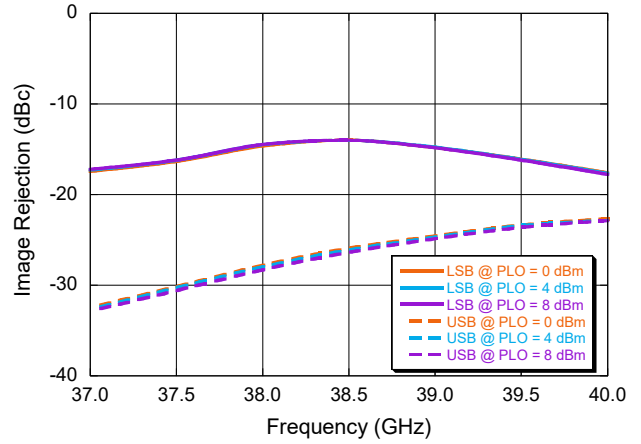


Image Rejection, IF = 21.4 MHz

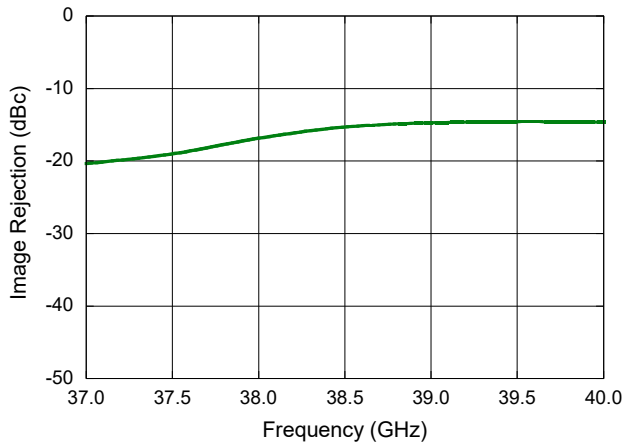
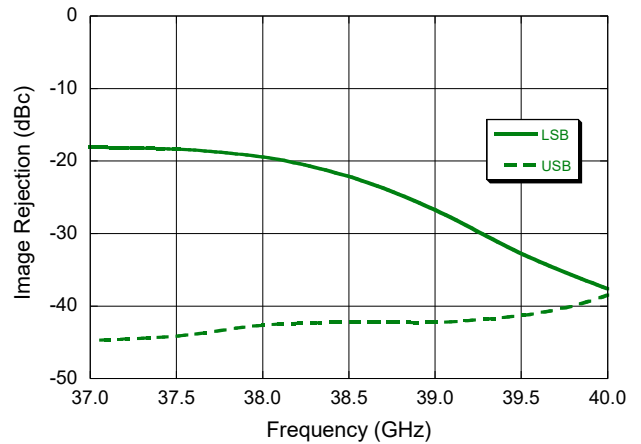
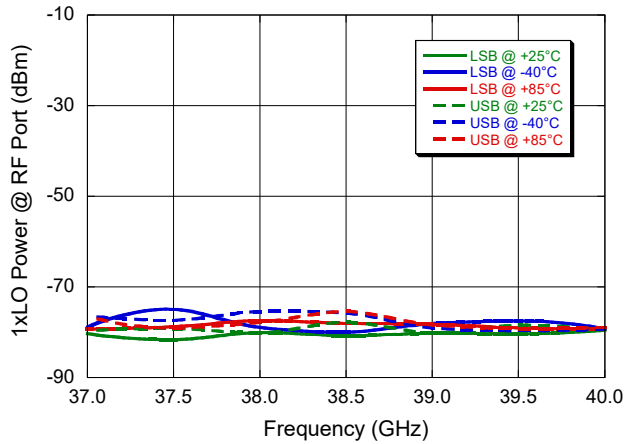


Image Rejection, IF = 3.5 GHz

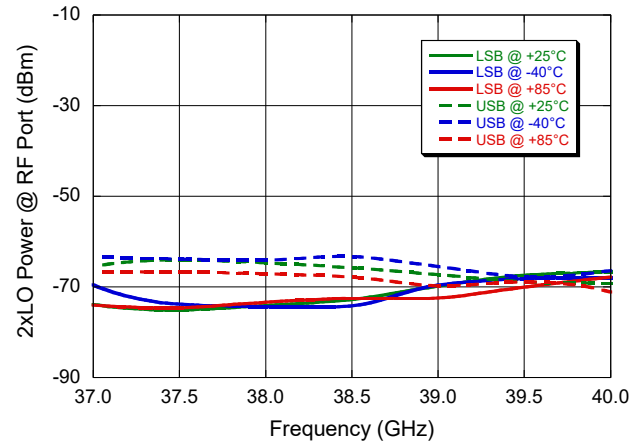


Typical Performance Curves

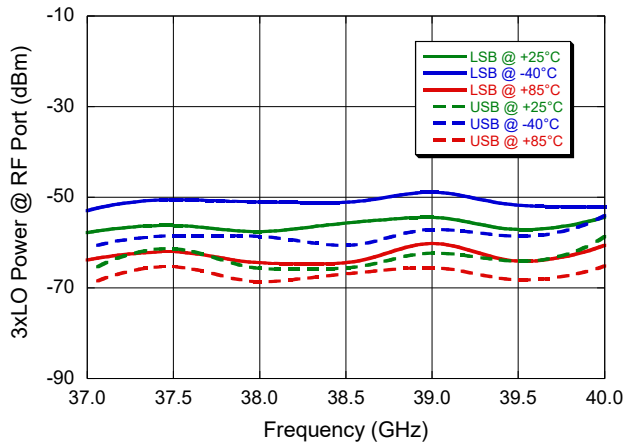
1xLO Leakage @ RF port



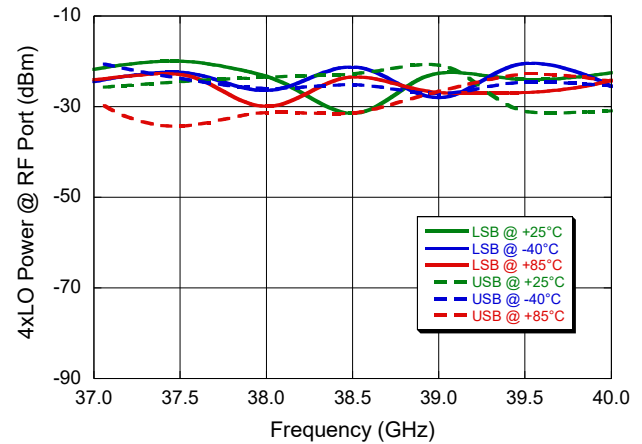
2xLO Leakage @ RF Port



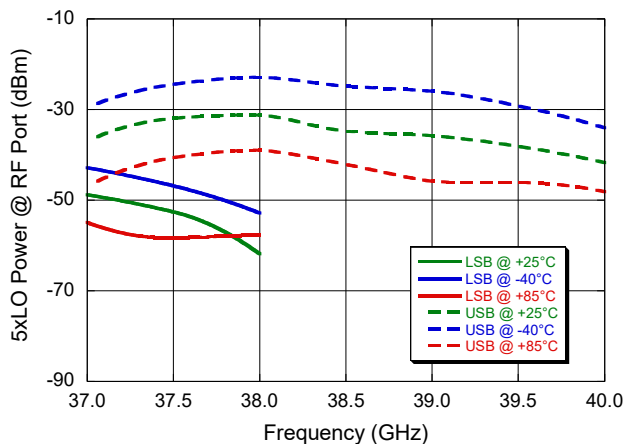
3xLO Leakage @ RF Port



4xLO Leakage @ RF Port

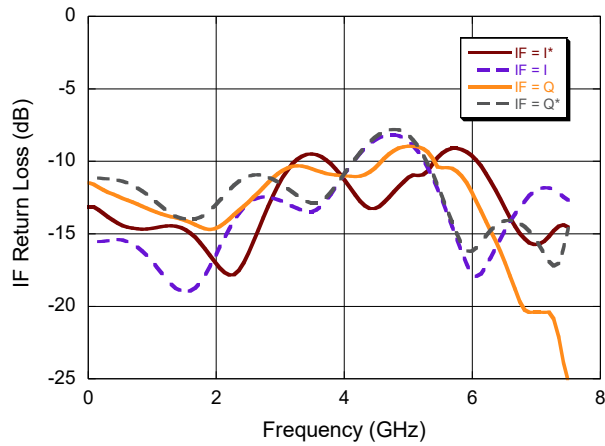


5xLO Leakage @ RF Port

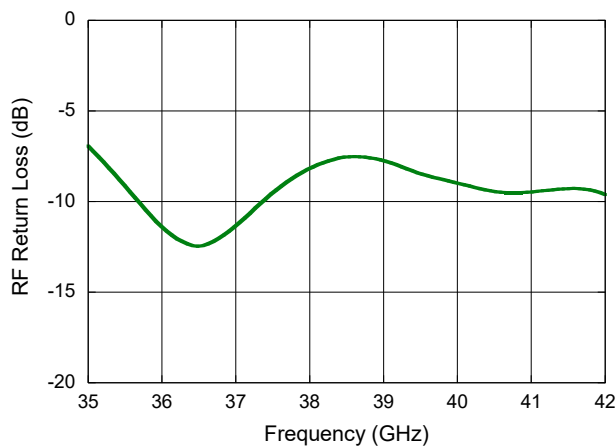


Typical Performance Curves

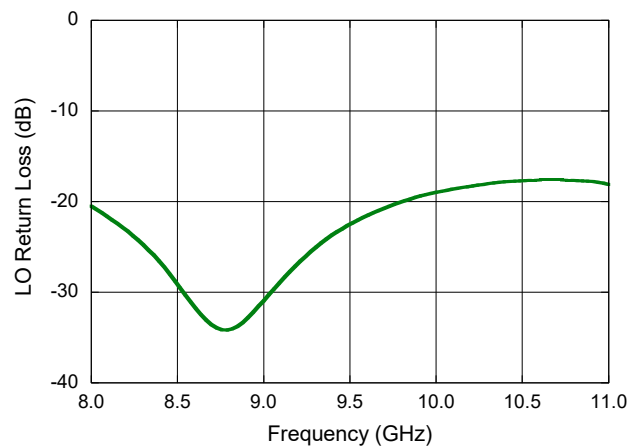
IF Return Loss



RF Return Loss



LO Return Loss

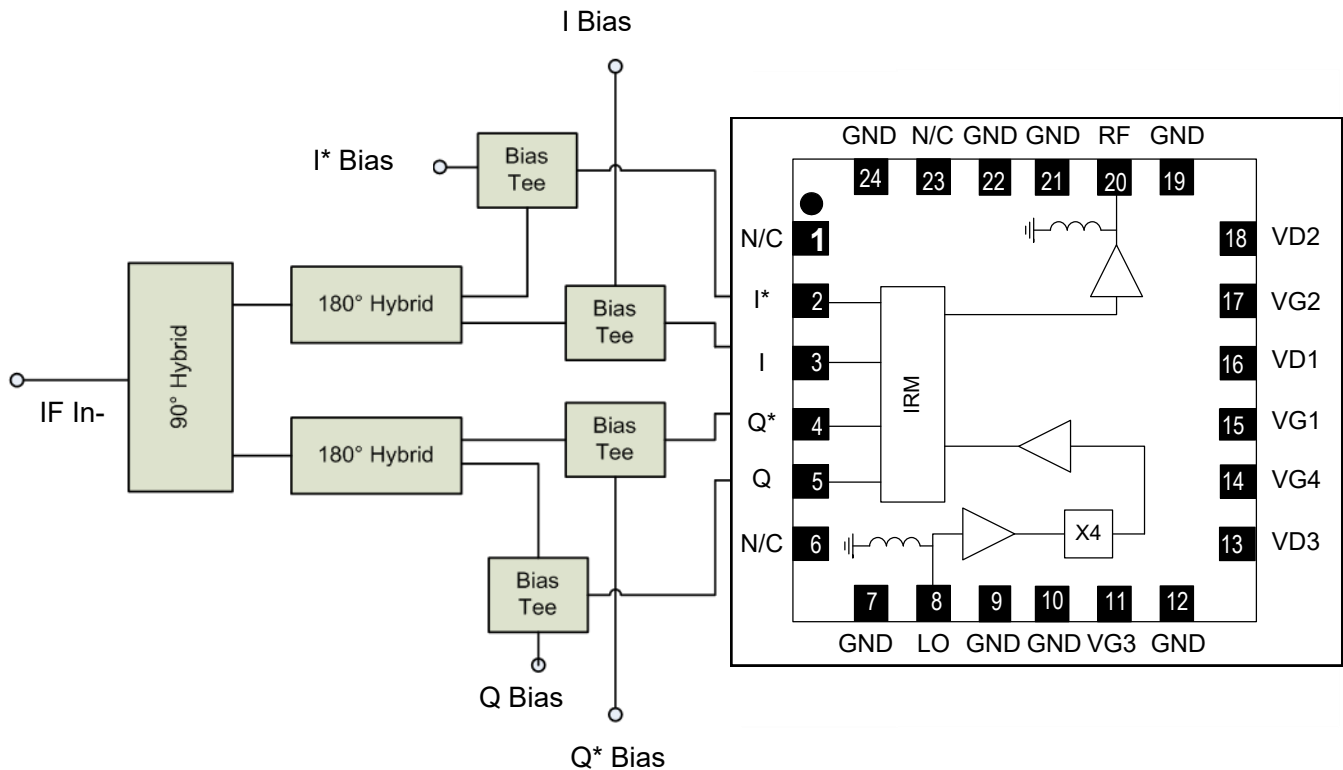


App Note [1] Biasing

MAUC-011009 is operated by biasing V_{D1} , V_{D2} and V_{D3} at 4.0 V. The corresponding drain currents are set to 45 mA, 135 mA and 200 mA respectively. V_{G4} requires a fixed voltage bias of nominally -3.25 V. It is recommended to use active bias on V_{G1} , V_{G2} , V_{G3} to keep the currents in V_{D1} , V_{D2} and V_{D3} constant, in order to maintain the best performance over temperature. Depending on the supply voltages available and the power dissipation constraints, the bias circuits may include a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply to sense the current. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply. If IF bias is to be used, it is important that V_{G4} is applied first.

App Note [2] IF Inputs

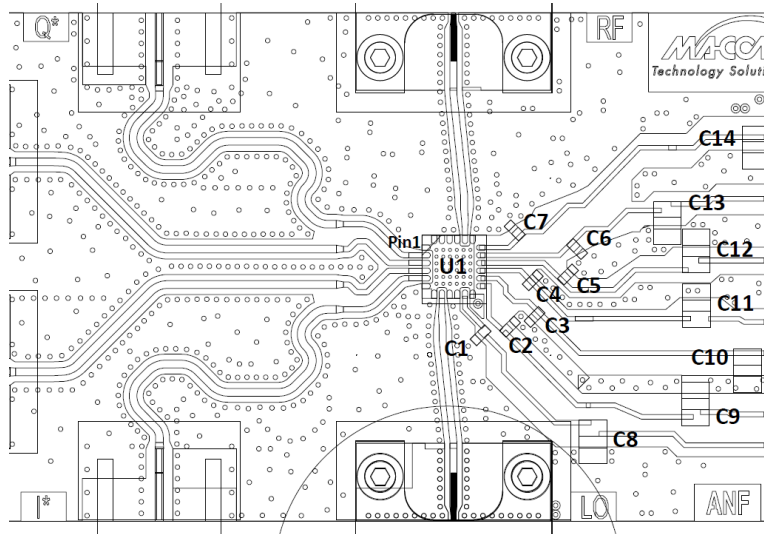
The IF input to the typical configuration is through a 90° hybrid coupler. The hybrid splits the IF input into inphase and quadrature phase components which feed into two 180° hybrid couplers splitting into 4 signals. These four signals enter the MAUC-011009 on I/I^* , Q/Q^* IF inputs through bias tees. For highest gain, best image rejection and highest OIP3, all the 4 IF inputs should be used. See App Note [4] for IF bias.



App Note [3] Board Layout

As shown in the recommended board layout, it is recommended to provide 100 pF decoupling capacitors as close to the bias pins as possible. Additional 10 nF and 1 μ F on each of the bias lines are recommended placed a distance further away.

Recommended Board Layout



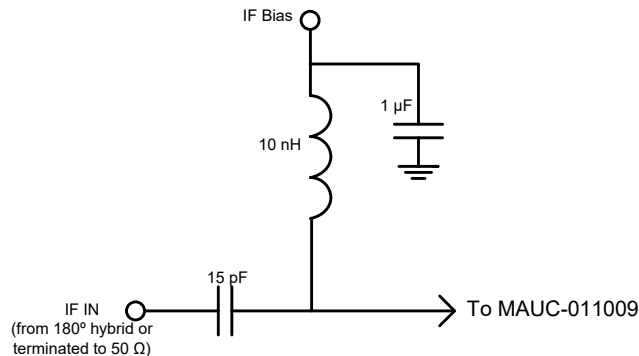
App Note [4] IF Bias

To obtain optimum 4xLO leakage performance, tuning is achieved by adjusting the DC bias on each of the IF inputs (I, Q, I*, Q*). DC bias is implemented by adding simple bias tees to each of the four IF ports (see drawing from App Note [2] for the bias tees location). The diagram below shows a typical bias tee design used.

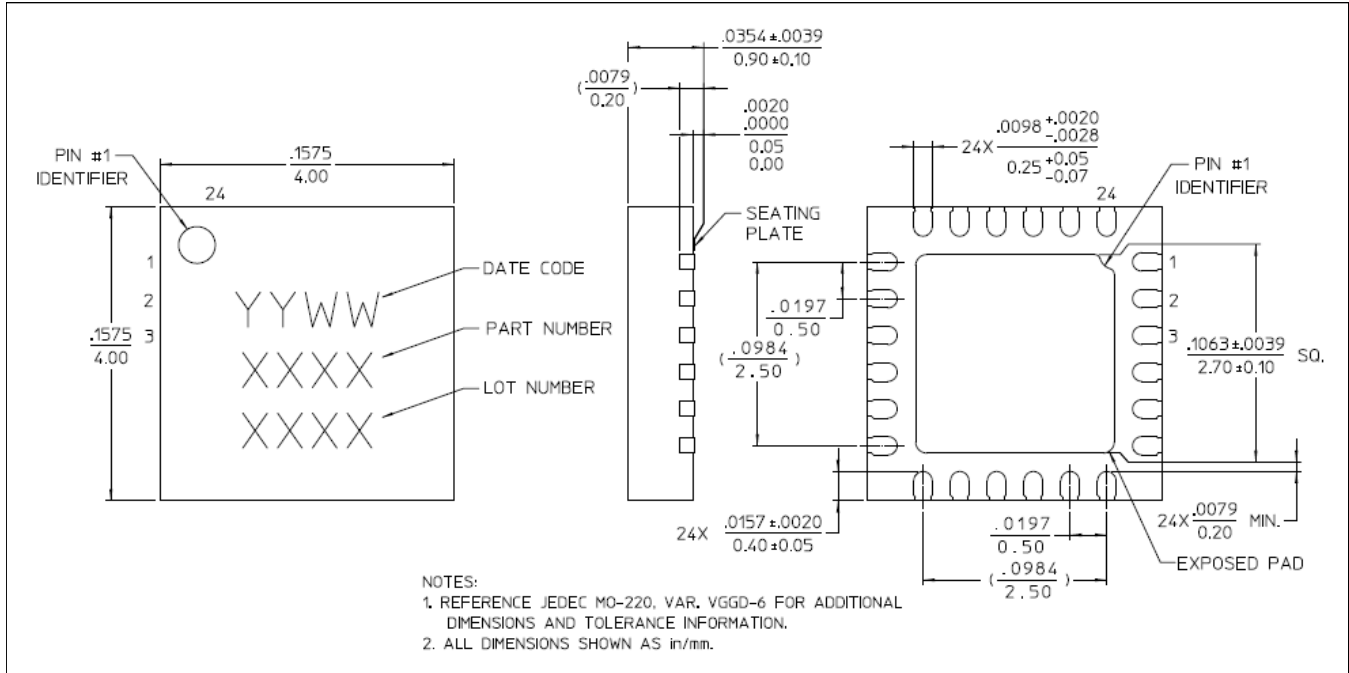
A typical tuning arrangement is to apply a fixed 0.2 V DC bias to I, Q. The remaining two IF ports can be tuned independently between - 0.5 and 1 V for minimum 4xLO leakage. Please note that V_{C4} must be applied to the device before IF bias is applied.

For minimum 4xLO leakage in a system, it may be necessary to correct the IF DC bias for different frequency and temperature conditions. This can be implemented by calibration and offset tables stored in memory, and used to control IF bias over all practical conditions.

Typical Configuration



Lead-Free 4 mm 24-Lead PQFN †



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is NiPdAuAg over copper.

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