MAAM-011168

Differential CATV Variable Gain Amplifier 5 - 300 MHz

Rev. V2

Features

- 40 dB Gain
- 15.5 dB, 0.5 dB steps, 5 Bit Digital Step Attenuator
- 36 dB MER, 64 QAM 39 Channels, 52 dBmV/ch.
- 8 V Operation
- 2.6 dB Noise Figure
- Serial or Parallel Attenuator Control
- Differential Input and Output
- Low Harmonics
- Power Down Mode
- Lead-Free 7 mm 48-lead PQFN Package
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant

Description

The MAAM-011168 is an integrated 2 stage differential amplifier with embedded digital step attenuator (DSA) assembled in a lead-free 7 mm 48-lead PQFN package.

The module provides excellent linearity and high output power with greater than 30 dB MER for 64 QAM modulation with 39 channels and 52 dBmV per channel. Gain in the minimum attenuation state is typically 40 dB. The internal DSA offers 15.5 dB attenuation range with 0.5 dB steps. The device is optimized for high output power with 8 V bias and can also operate from 5 V bias if lower DC power consumption and output level is desired. The module also provides a power down function for each of the amplifier stages.

This amplifier is ideally suited for use in CATV reverse path applications.

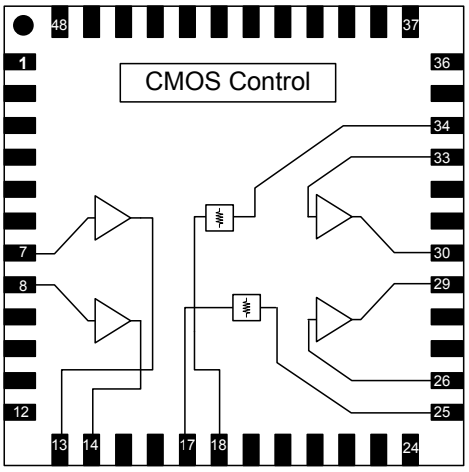
Ordering Information[1,2]

Part Number	Package
MAAM-011168-TR1000	1000 piece reel
MAAM-011168-TR3000	3000 piece reel
MAAM-011168-001SMB	Sample Test Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Functional Schematic



Pin Configuration[3]

Pin No.	Description	Pin No.	Description
1	Latch Enable	30	Stage 2 Output (+)
6	Stage1 Feedback (+)	32	Stage 2 Feedback(+)
7	Stage 1 input (+)	33	Stage 2 Input (+)
8	Stage 1 input (-)	34	Attenuator Output (+)
9	Stage 1 Feedback(-)	36	DSA Serial Output
13	Stage 1 Output (+)	37	Power Up Select 2
14	Stage 1 Output (-)	38	Power Up Select 1
15	Enable Stage 1	39	V_{DD} CMOS Controller
16	Stage 1 Bias Voltage	40	Unused Control (B5)[5]
17	Attenuator Input (-)	41	Attenuator Bit 4 (8 dB)
18	Attenuator Input (+)	42	Attenuator Bit 3 (4 dB)
20	Stage 2 Bias Voltage	43	Attenuator Bit 2 (2 dB)
21	Enable Stage 2	44	Attenuator Bit 1 (1 dB)
25	Attenuator Output (-)	45	Attenuator Bit 0 (0.5 dB)
26	Stage 2 Input (-)	46	Parallel/Serial Select
27	Stage 2 Feedback(-)	47	Clock
29	Stage 2 Output (-)	48	Serial Input
		49	RF and DC Ground[4]

3. All pins not listed in the table are "No Connection" and should be left unconnected.
4. The exposed pad centered on the package bottom must be connected to RF and DC ground.
5. MACOM recommends grounding pin 40. It is connected to the CMOS controller but does not affect attenuator setting.

Electrical Specifications: T_A = +25°C, V_{CC} = 8 V, minimum attenuation state, Z_0 = 75 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	Max. Gain State @ 100 MHz, -29 dBm P_{IN}	dB	38	40	42
Gain Slope	Positive tilt from 5 - 200 MHz	dB	—	1.0	—
Noise Figure[6]	—	dB	—	2.6	—
Input Return Loss	—	dB	—	22	—
Output Return Loss	—	dB	—	22	—
Reverse Isolation	—	dB	—	50	—
Attenuation Range	100 MHz, Relative to maximum gain, -29 dBm P_{IN}	dB	14.6	15.5	16.4
64 QAM Modulated Error Ratio[7]	39 Channels (5 - 250 MHz), 51 dBmV/Ch. Single Channel (8 - 200 MHz), 71 dBmV/Ch. Single Channel (250 MHz), 70 dBmV/Ch. 16 Channels (5 - 250 MHz), 56 dBmV/Ch.	dB	— — — 30	36 35 35 34	—
P1dB	—	dBm	—	27	—
OIP2	2-tone,+9 dBm/tone, 1 MHz tone spacing, 200 MHz	dBm	—	74	—
OIP3	2-tone,+9 dBm/tone, 1 MHz tone spacing, 200 MHz	dBm	—	44	—
T_{ON}, T_{OFF}	50% Control to 90 / 10 % RF	ns	—	400	—
I_{CC}	EN1 = EN2 = 5 V	mA	—	290	315
I_{CC_OFF}	EN1 = EN2 = 0 V	mA	—	3	10
I_{EN1}, I_{EN2}	EN1 = EN2 = 5 V	mA	—	0.7	—

6. Includes Balun loss
7. Modulation error ratio each channel 64 QAM 5.12 MS/s

Absolute Maximum Ratings[8,9,10]

Parameter	Absolute Maximum
RF Input Power	-8 dBm
Bias Voltage (V_{CC})	10 V
Control Voltage	-0.5 V to 5.5 V
Operating Temperature	-40°C to +100°C
Junction Temperature[11]	+150°C
Storage Temperature	-65°C to +150°C

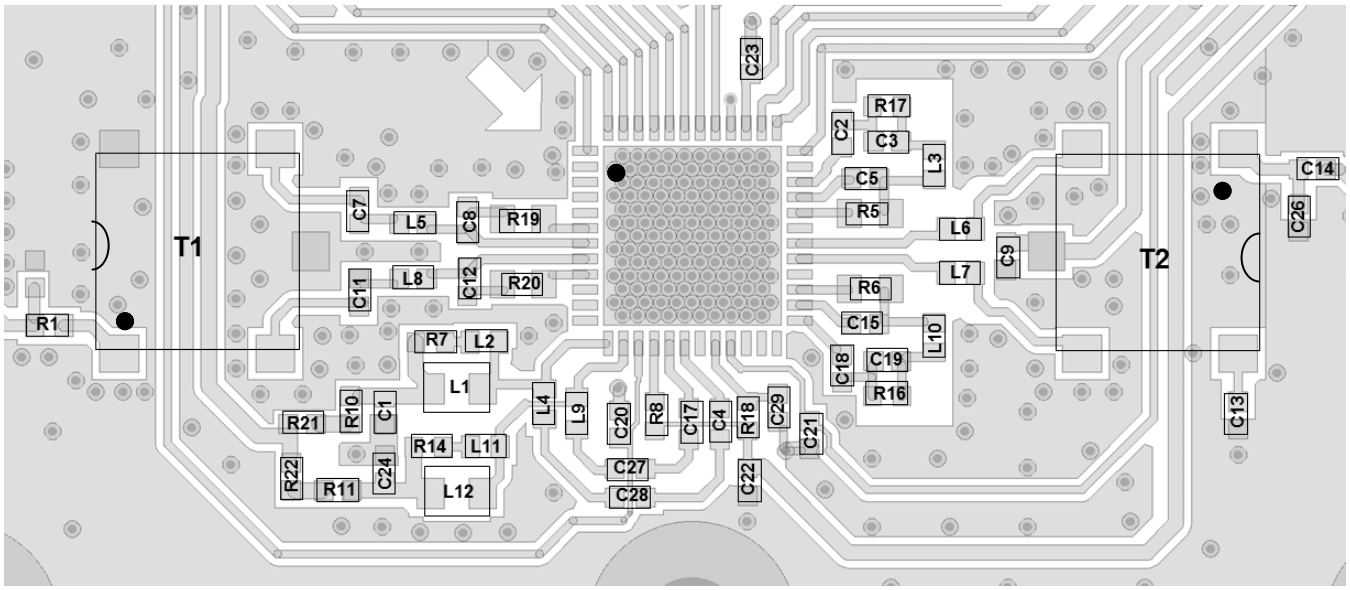
8. Exceeding any one or combination of these limits may cause permanent damage to this device.
9. MACOM does not recommend sustained operation near these survivability limits.
10. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1 x 10^6 hours.
11. Junction Temperature (T_J) = T_C + Θjc * (V * I)
    Typical thermal resistance (Θjc) = 8.85° CW.
    a) For T_C = +25°C,
    T_J = 47°C @ 8 V, 315 mA
    b) For T_C = +100°C,
    T_J = 122°C @ 8 V, 315 mA

Truth Table[12]

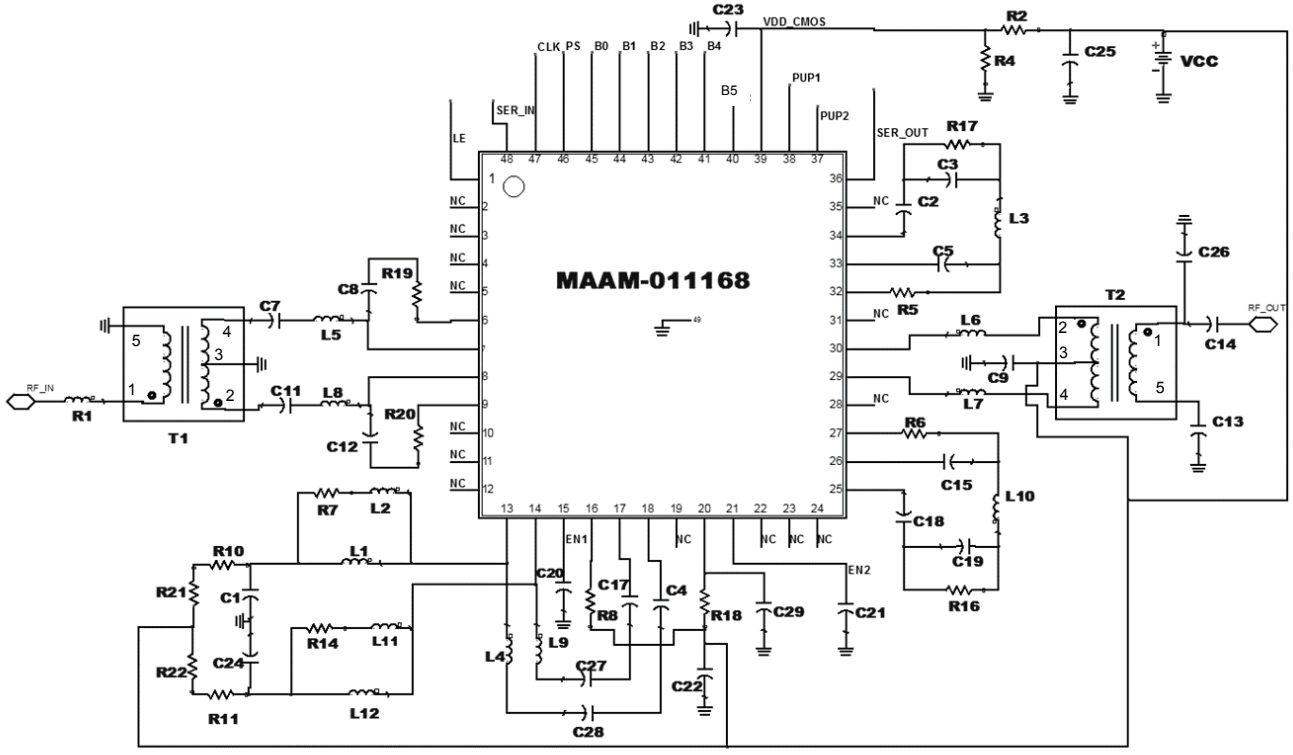
B5	B4	B3	B2	B1	B0	Attenuation (dB)
X	1	1	1	1	1	Minimum
X	1	1	1	1	0	0.5
X	1	1	1	0	1	1
X	1	1	0	1	1	2
X	1	0	1	1	1	4
X	0	1	1	1	1	8
X	0	0	0	0	0	15.5

12. Logic “0” = 0 V to 0.8 V ± 0.2 V,
    Logic “1” = 2 V to 5 V ± 0.2 V.

PCB Layout



Application Schematic



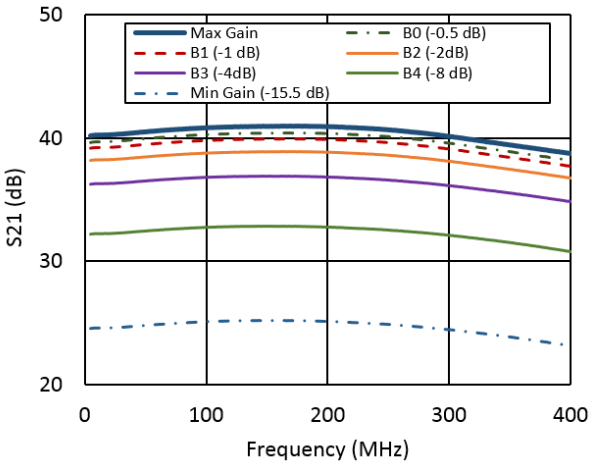
Parts List : 8 V Application circuit

Part	Value	Case Style	Function/Notes
C1, C9, C20, C21, C22, C23, C24, C29	0.1 µF	0402	RF Bypass
C2, C4, C5, C7, C8, C11, C12, C13, C14 C15, C17, C18, C27, C28	0.1 µF	0402	DC Block
C3, C19	150 pF	0402	Gain Tilt (with R16 and R17)
C25	1 µF	0805	Low Frequency Bypass
C26	1 pF	0402	Output Match
L1, L12	47 µH	0806	V_CC1 Choke. Murata LQH2MCN470K02L
L2, L11	250 nH	0402	Gain Tilt (with R7 & R14). Coilcraft 0402AF-251XJLU
L3, L10	22 nH	0402	Input Match Stage2 Amp
L4, L9	22 nH	0402	Output Match Stage1 Amp
L5, L8	27 nH	0402	Input Match Stage1 Amp
L6, L7	33 nH	0402	Output Match Stage2 Amp
R1	0 Ω	0402	Input Match
R18	30 Ω	0402	Increase value can reduce stage 2 current
R2	3 kΩ	0402	Voltage divider to set V_{DD}_CMOS[13]
R4	5 kΩ	0402	Voltage divider to set V_{DD}_CMOS[13]
R7, R14	249 Ω	0402	Gain Tilt (with L2, L11)
R16, R17	22 Ω	0402	Gain Tilt (with C3, C19)
R8	10 kΩ	0402	Increase value can reduce stage 1 current.
R10, R11, R21, R22	50 Ω	0402	Drop V_{CC}1 to 5 V. Pdiss 1/20 W. 0 Ω for 5 V V_{CC}
R5, R6, R19, R20	150 Ω	0402 or 0603	Additional feedback resistors for Stage1 & Stage2. May be used to adjust gain or implement temperature compensation if replaced with thermistors.
T1, T2	1:2		MABA-011050

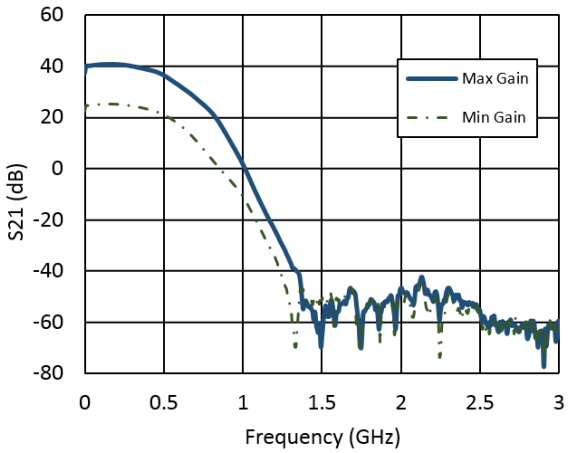
13. These components may be omitted if 5 V supply is available for V_{DD}_CMOS.

Typical Performance Curves:

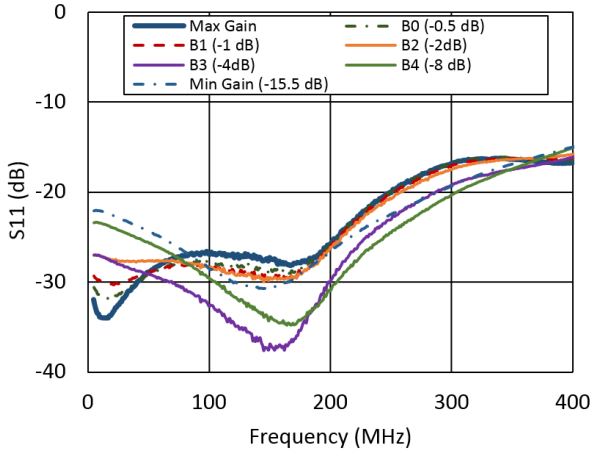
Gain



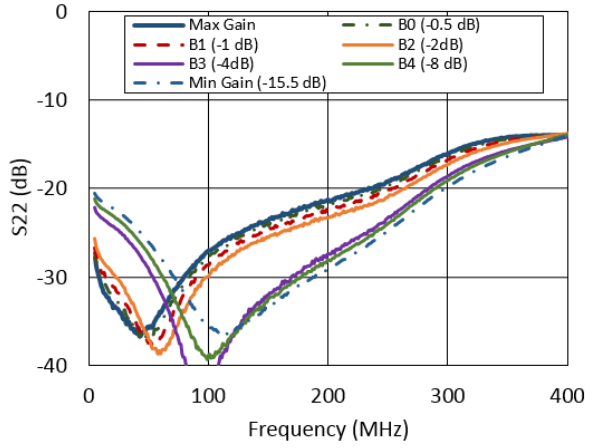
Gain - Wideband



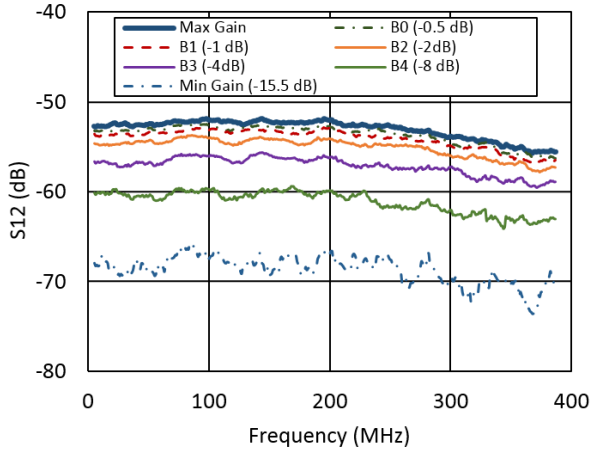
Input Return Loss



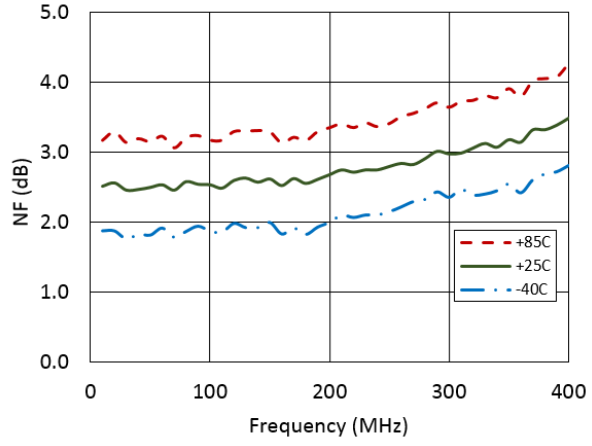
Output Return Loss



Reverse Isolation

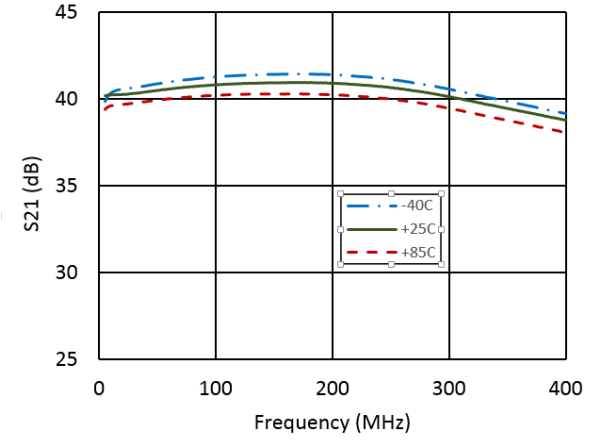


Noise Figure

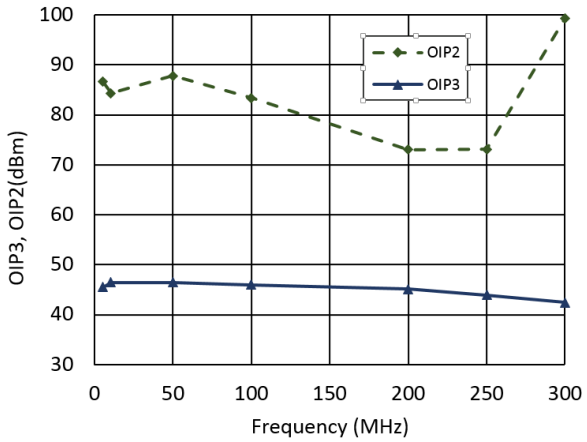


Typical Performance Curves:

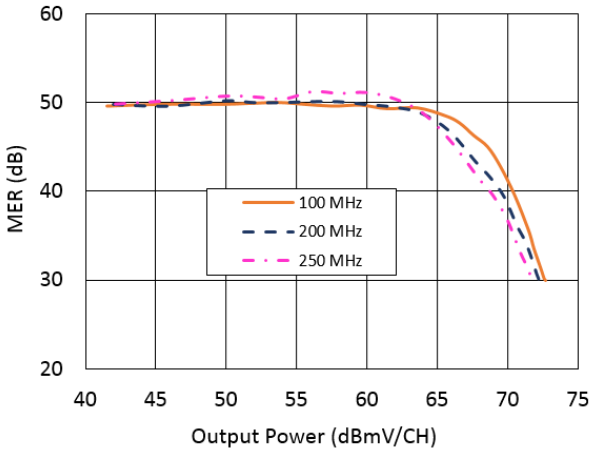
Gain



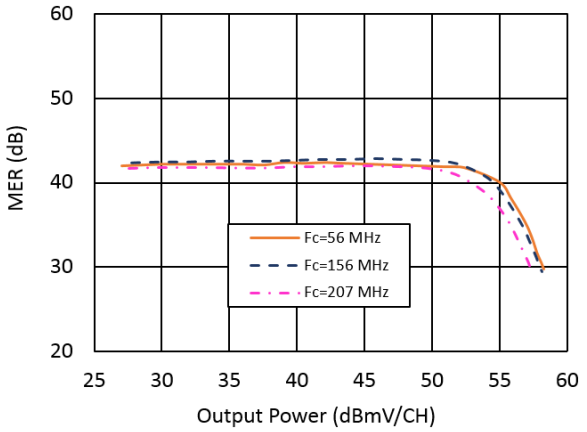
OIP3, OIP2



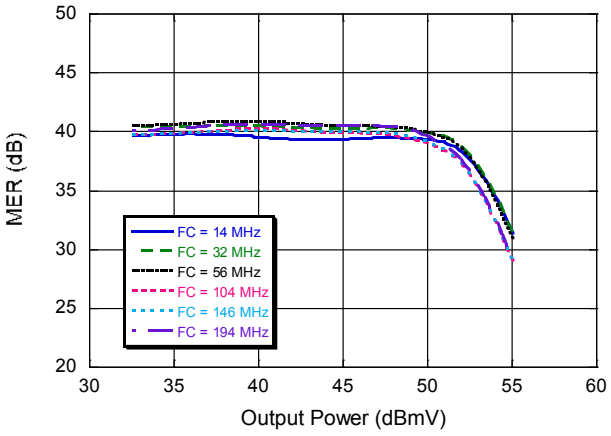
Modulation Error Ratio (64 QAM, single channel)



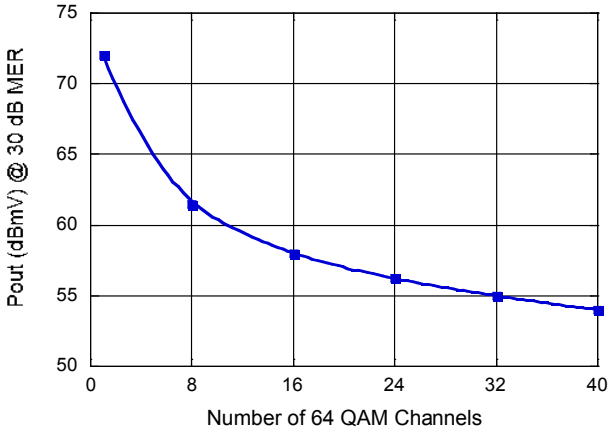
Modulation Error Ratio (64 QAM, 16 channel)



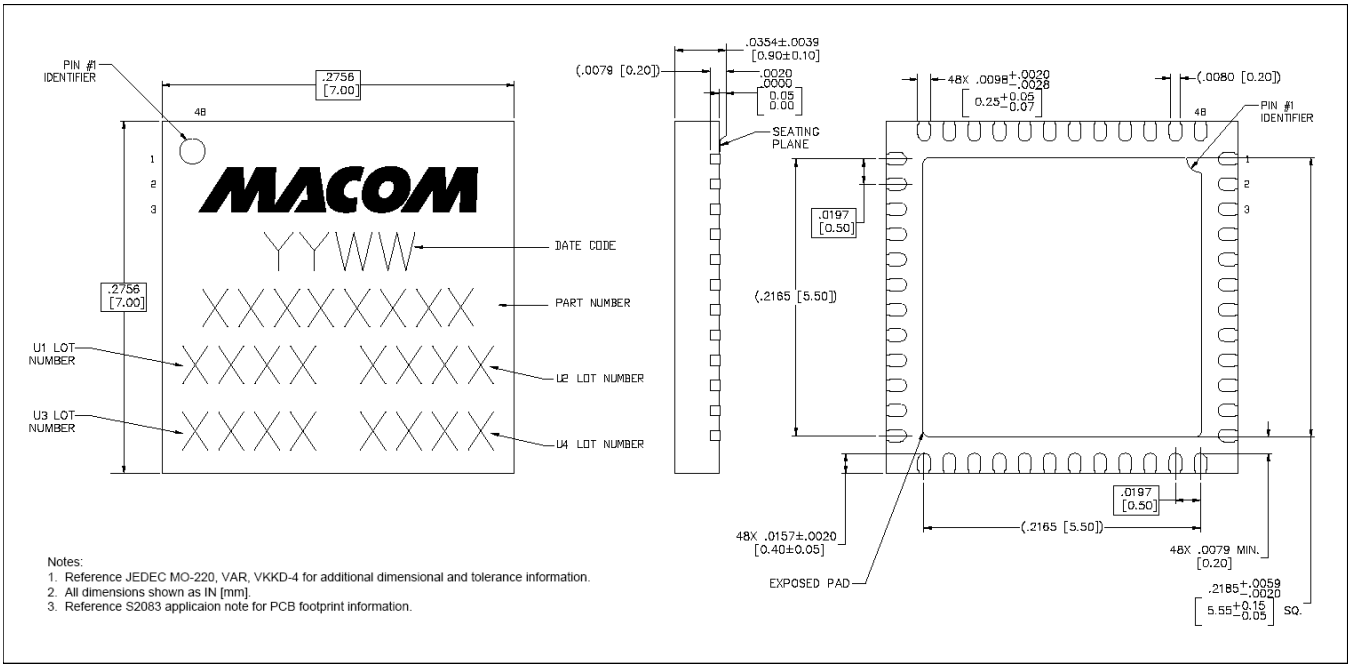
Modulation Error Ratio (64 QAM, 32 channel)



P_{OUT} @ 30 dB Modulation Error Ratio

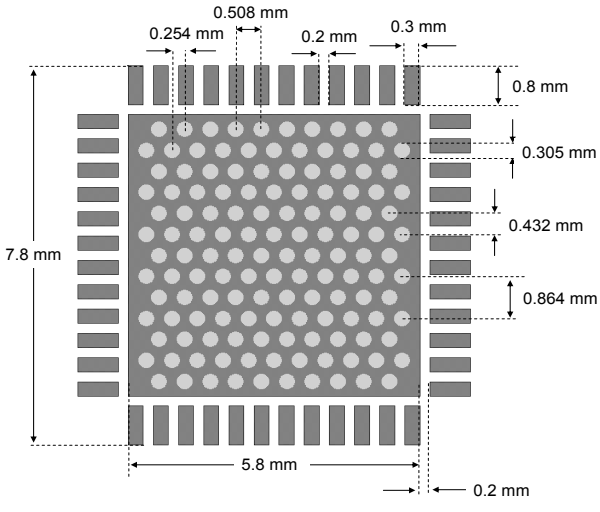


Lead-Free 7 mm 48-lead PQFN



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAuAg.

Recommended Land Pattern



Copper plating (board and vias) should be ≥ 0.05 mm thick.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1B devices.

Applications Section

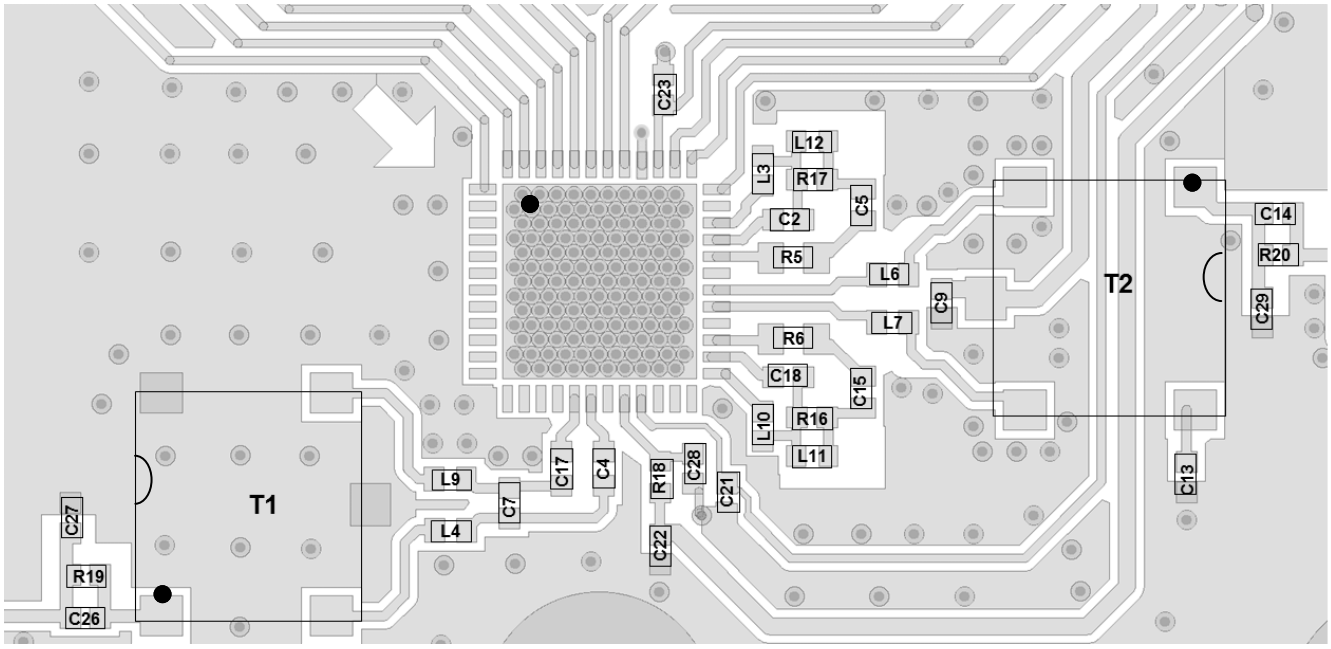
First Stage Bypass Application

If a lower gain VGA solution is desired the MAAM-011168 may be implemented with the first stage bypassed. Typical Performance and Application Details for implementing the First Stage Bypass Application are presented below.

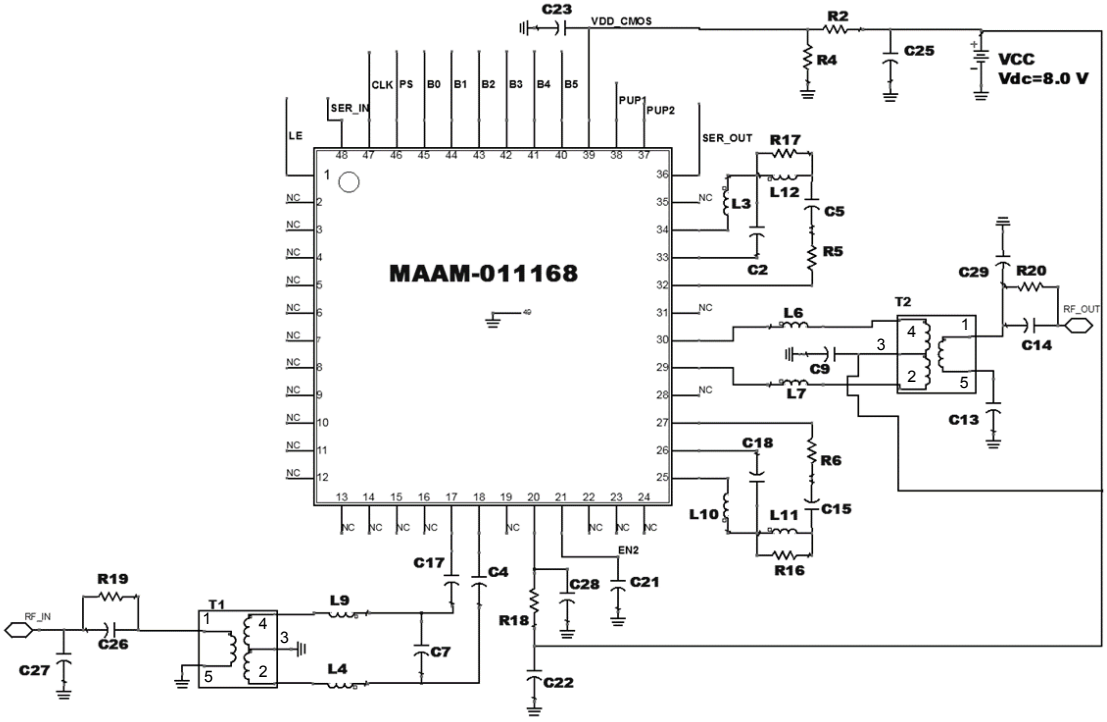
Typical Performance: T_A = +25°C, V_{CC} = 8 V, minimum attenuation state, Z_0 = 75 Ω

Parameter	Test Conditions	Units	Typical
Gain	Max. Gain State @ 100 MHz, -29 dBm P_{IN}	dB	19
Gain Slope	Positive tilt from 5 - 250 MHz	dB	0
Input Return Loss	—	dB	22
Output Return Loss	—	dB	22
Noise Figure	—	dB	4.3
Attenuation Range	100 MHz, Relative to maximum gain, -29 dBm P_{IN}	dB	15.5
64 QAM MER[7]	39 Channels (5 - 250 MHz), 51 dBmV/Ch. Single Channel (8 - 200 MHz), 71 dBmV/Ch. Single Channel (250 MHz), 70 dBmV/Ch. 16 Channels (5 - 250 MHz), 56 dBmV/Ch.	dB	36 35 35 34
P1dB	—	dBm	27
OIP2	2-tone,12 dBm/tone, 1 MHz tone spacing, 200 MHz	dBm	76
OIP3	2-tone,12 dBm/tone, 1 MHz tone spacing, 200 MHz	dBm	46
I_{CC}	EN1 = EN2 = 5 V	mA	225

PCB Layout: First Stage Bypass



Application Schematic: First Stage Bypass

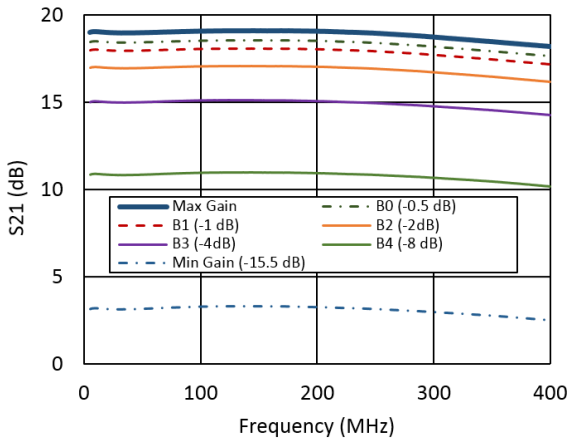


Parts List : First Stage Bypass

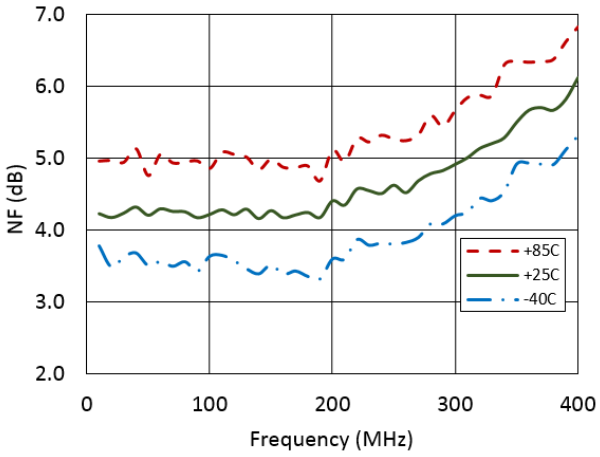
Part	Value	Case Style	Function/Notes
C9, C13, C21, C22, C23, C28	0.1 µF	0402	RF Bypass
C2, C4, C5, C15, C17, C18	0.1 µF	0402	DC Block
C14	470 pF	0402	Gain Flatness
C25	1 µF	0805	Low Frequency Bypass
C27, C29	1pF	0402	Input, Output Matching
C26	270 pF	0402	Gain Flatness
C7	DNI	-	Matching if needed
L3, L10	18 nH	0402	Input Match Stage2 Amp
L4, L9	22 nH	0402	Input Match DSA
L6, L7	24 nH	0402	Output Match Stage2 Amp
L11, L12	120 nH	0402	Gain Flatness
R18	30 Ω	0402	Increase value can reduce stage 2 current
R19, R20	6.8 Ω	0402	Gain Flatness
R2	3 kΩ	0402	Voltage divider to set V_{DD}_CMOS[13]
R4	5 kΩ	0402	Voltage divider to set V_{DD}_CMOS[13]
R16, R17	100 Ω	0402	Gain Flatness
R5, R6	150 Ω	0402 or 0603	Additional feedback resistors for Stage1 & Stage2. May be used to adjust gain or implement temperature compensation if replaced with thermistors.
T1, T2	1:2		MABA-011050

Typical Performance Curves: First Stage Bypass Application

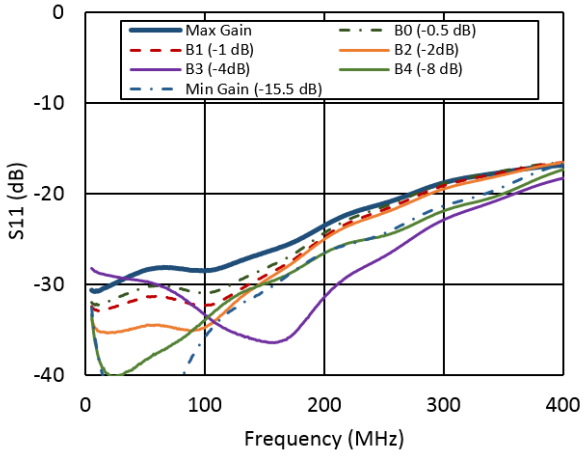
Gain



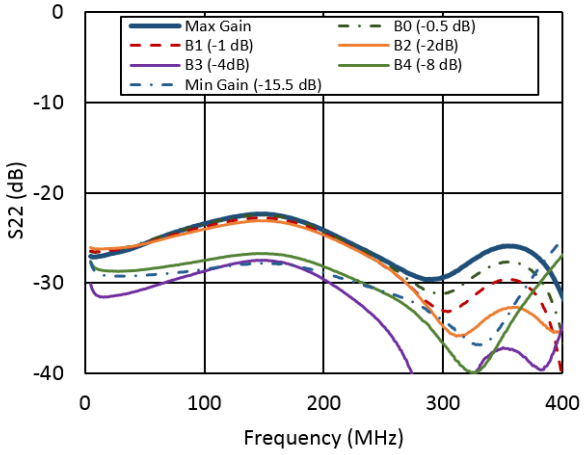
Noise Figure



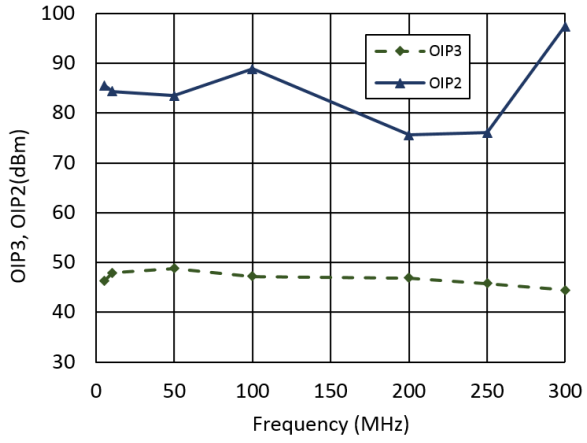
Input Return Loss



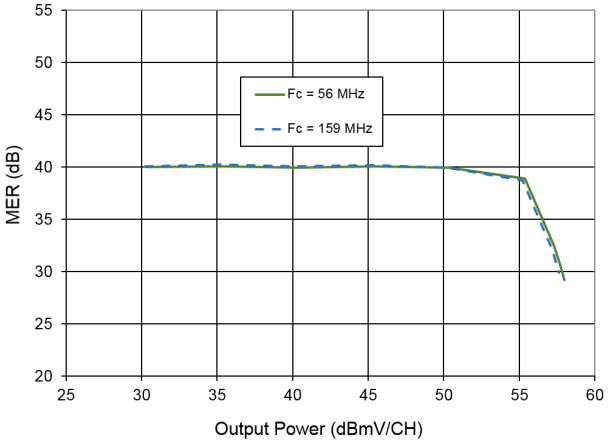
Output Return Loss



OIP3, OIP2



MER vs Pout - 16 Channels



Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

Mode Truth Table

P/S	LE	Mode
1	X	Serial
0	Constant High	Direct Parallel
0	Pulsed	Latched Parallel

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with MSB first. After shifting in the 6 bit word, bringing LE high will set the attenuator to the desired state. While LE is high the CLK is masked to protect the data while implementing the change . SEROUT is the SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled and the serial input register is loaded asynchronously with parallel digital inputs.

Direct Parallel Mode

The parallel mode is enabled when P/S is set to low. In the direct parallel mode, the attenuator is controlled by the parallel control inputs directly. The LE must be at logic high to control the attenuator in this mode.

Latched Parallel Mode

In the latched parallel mode, the parallel control inputs will be buffered by registers, and loaded to the outputs when LE is high. The outputs shall not change states when LE is low.

Power-up States

The power-up (PUP) states will work in both serial and parallel modes, and initiate the attenuator according to the PUP truth table. During power up, the digital inputs shall be held constant for at least 1 µs after V_{CC} reaches 90% of final value. For serial mode, the PUP states will only work when LE is held low. The PUP state shall be locked out after the first LE pulse. Proper operation of power up states requires fast rise time (<200 ns) for V_{DD}-CMOS.

Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

PUP Truth Table

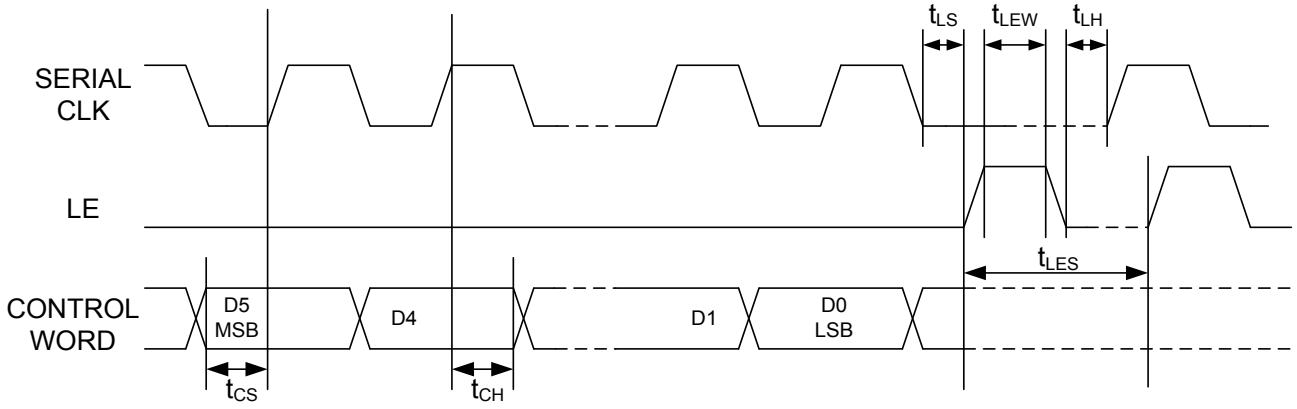
Inputs				Gain Relative to Max. Gain	Notes
PS	LE	PUP2	PUP1		
0	0	0	0	-15.5 dB	Parallel Mode
0	0	0	1	-8 dB	
0	0	1	0	0 dB	
0	0	1	1	0 dB	
0	1	X	X	0 to –15.5 dB (Set B0 - B4)	
1	0	X	X	0 to –15.5 dB (Set B0 - B4)	Serial Mode
1	1	X	X	No Definition	

Serial Interface Timing Characteristics

Symbol	Parameter	Typical Performance			Units
		-40°C	+25°C	+85°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{CS}	Min. Control Set-up Time	20	20	20	ns
t_{CH}	Min. Control Hold Time	20	20	20	ns
t_{LS}	Min. LE Set-up Time	10	10	10	ns
t_{LEW}	Min. LE Pulse Width	10	10	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t_{LES}	Min. LE Pulse Spacing	630	630	630	ns

Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

Serial Input Interface Timing Diagram



Parallel Control Word