M21330

4.25 Gbps Quad-Channel Cable Driver and Adaptive Equalizer with 4x4 Crosspoint Switch

The M21330 is a quad channel device designed to enable the transmission of multi gigabit serial data through the most challenging environments. The device features four independent adaptive equalizers that automatically equalize data at rates up to 4.25 Gbps. Full register control of the M21330 is provided through an I^2C compatible software control interface. The M21330 can also self-configure from an external EEPROM without the need for a host processor. For compatibility with PCI-Express and S-ATA/SAS systems, the M21330 is designed with an electrical idle pass-through function to drive the differential output to the common mode level during OOB signaling. Boundary scan is provided for high-speed input and output pins through a JTAG port, and the device is available in a 6x6 mm, 40-pin QFN package.

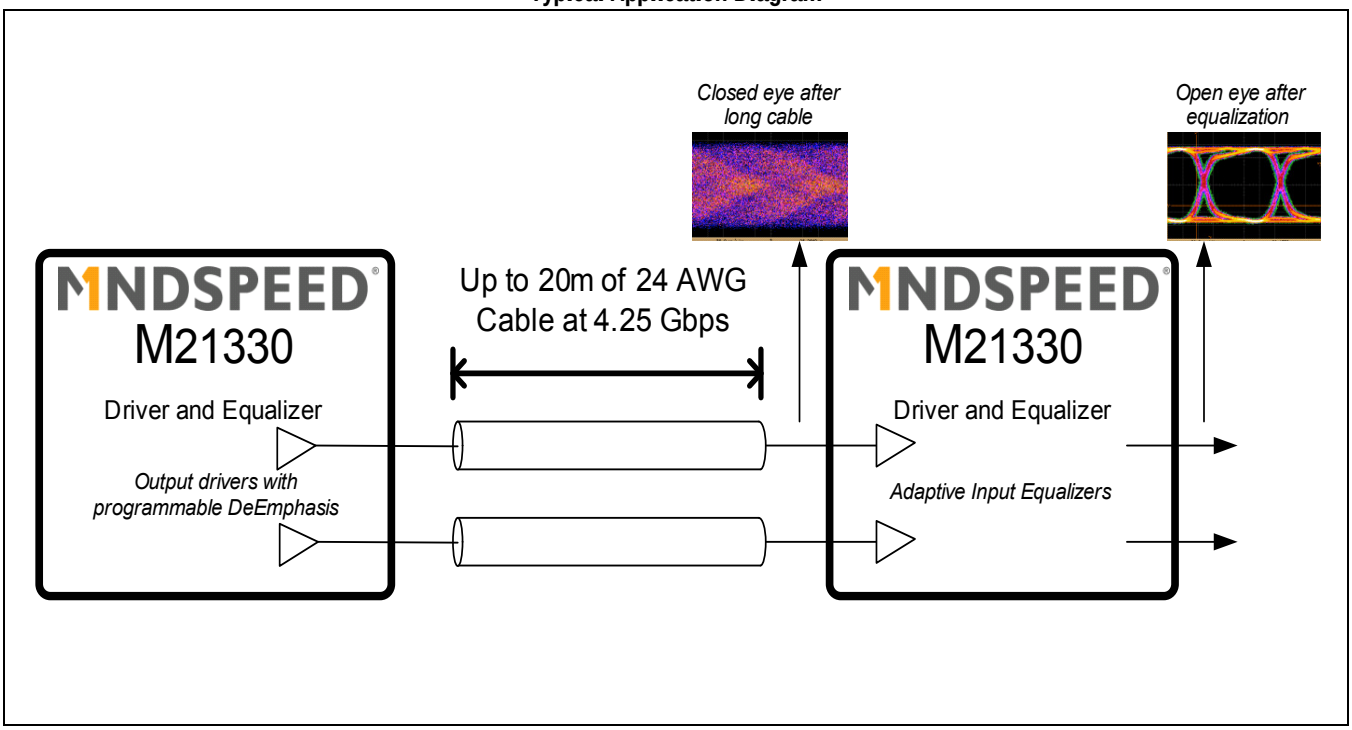
Features

- Adaptive equalization for up to 20m of 24 AWG cable at 4.25 Gbps
- Supports electrical idle signaling for PCIe and OOB signaling for S-ATA/SAS
- Low power dissipation: 145 mW per channel, 580 mW total power at 1.2V
- Up to 35 dB of input equalization and 6 dB of output de-emphasis
- Software and EEPROM programmable
- 6x6 mm, 40-pin QFN package
- Extended operating case temperature range (-20°C to 85°C)
- Integrated 4x4 Crosspoint Switch Matrix

Applications

XAUI	3.125 Gbps	—	—
S-ATA/SAS	1.5 Gbps	3.0 Gbps	—
PCIe	2.5 Gbps	—	—
Fibre Channel	1.0625 Gbps	2.125 Gbps	4.25 Gbps
InfiniBand	2.5 Gbps	—	—
SDI Video	270 Mbps	1.485 Gbps 1.485/1.001 Gbps	2.97 Gbps 2.97/1.001 Gbps

Typical Application Diagram



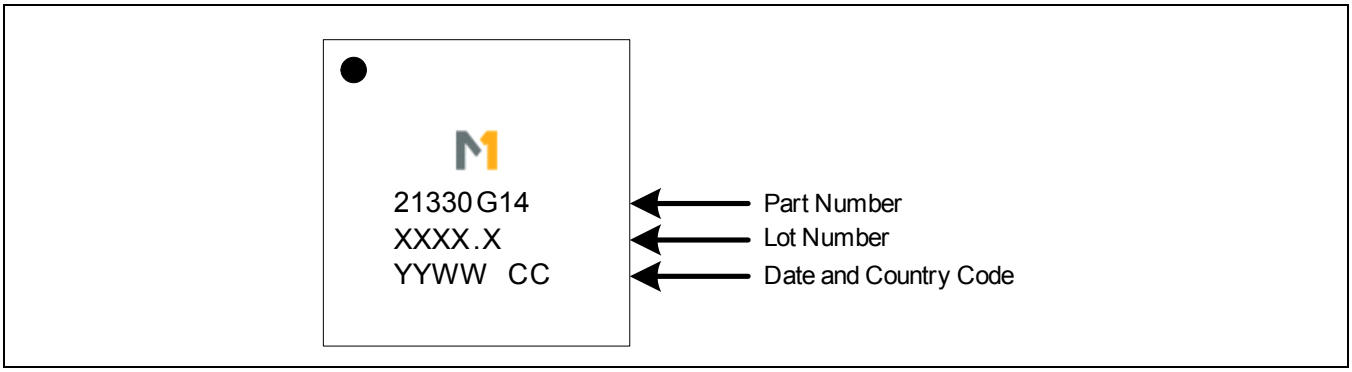
Ordering Information

Part Number	Package	Operating Case Temperature
M21330G-14*	6x6 mm, 40 pin QFN package	-20°C to 85°C
* The letter “G” designator after the part number indicates that the device is RoHS compliant. Refer to www.mindspeed.com for additional information. The RoHS compliant devices are backwards compatible with 225°C reflow profiles.		

Revision History

Revision	Level	Date	Description
E	Released	December 2010	Updated control pin type definitions to define inputs and outputs in Table 3-1.
D	Released	August 2010	Updated the Marking Diagram to add legend. Updated Package Outline Drawing to match new package and height requirements (Figure 3-1). Corrected input equalization note on registers 04h and 05h to read “1111” instead of “111” for the lowest setting. Removed 3.4 MHz I^2C data rate and reduced capacitor bus loading to 100 µF and 400 µF (Section 5.12). Updated MIC system diagram quazi master I^2C address to match documentation (0x50) (Figure 5-4).
C	Released	May 2010	Section 5.1 rewritten to include EEPROM timing information. Added timing diagram (Figure 5-2). Section 5.13 rewritten. Added Figure 5-4.
B	Released	August 2009	Refer to prior revision for details on data sheet changes.
A	Released	January 2009	Initial release.

M21330 Marking Diagram



1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
AV_{DDIO}	Analog I/O power supply voltage	—	2.1	V
V_{DDCORE}	Core power supply voltage	—	1.5	V
DV_{DDIO}	Digital I/O power supply voltage	—	3.6	V
T_{STORE}	Storage Temperature	–65	150	°C
$V_{ESD, HBM}$	Electrostatic discharge voltage (HBM)	—	2000	V
$V_{ESD, CDM}$	Electrostatic discharge voltage (CDM)	—	500	V

NOTES:

Exposure of the device beyond the minimum/maximum limits may cause permanent damage.

Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
AV_{DDIO}	Analog I/O power supply voltage	1.14	1.2, 1.8	1.89	V
V_{DDCORE}	Core power supply voltage	1.14	1.2	1.26	V
DV_{DDIO}	Digital I/O power supply voltage	2.37	2.5, 3.3	3.47	V
T_{CASE}	Case Temperature	–20	—	85	°C
θ_{JA}	Junction to ambient thermal resistance (no airflow)	—	34.4	—	°C/W
θ_{JA}	Junction to ambient thermal resistance (2.5 m/s airflow)	—	26.9	—	°C/W
θ_{JC}	Junction to case thermal resistance	—	3.3	—	°C/W

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
AI_{DDIO}	Analog I/O power supply current (AV_{DDIO} = 1.2V)	1	—	70	80	mA
AI_{DDIO}	Analog I/O power supply current (AV_{DDIO} = 1.8V)	2	—	130	150	mA
AI_{DDCORE}	Core power supply current (AV_{DDIO} = 1.8V)	2	—	440	530	mA
DI_{DDIO}	Digital I/O power supply current	—	—	2	—	mA
P_{TOTAL}	Total power dissipation (AV_{DDIO}=1.2V)	1, 3	—	580	735	mW
P_{TOTAL}	Total power dissipation (AV_{DDIO}=1.8V)	2, 3	—	765	955	mW

NOTES:

1. Valid with nominal (800 mV_{PPD}) output swing for all channels.
2. Valid with maximum (1500 mV_{PPD}) output swing on all channels.
3. Typical calculated with nominal current and voltage. Maximum calculated with maximum current and 5% over voltage.

Unless noted otherwise, specifications in this section are valid with AV_{DDIO} = 1.8V, 25°C case temperature, 800 mV_{PP} differential input voltage swing, nominal (800 mV_{PPD}) output swing level PRBS 2^{15} - 1 test pattern at 4.25 Gbps, R_{LOAD} = 50Ω, short traces and/or cables.

Table 1-4. Input/Output Electrical Characteristics (1 of 2)

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DR	NRZ Data Rate	—	100	—	4250	Mbps
V_{IN}	Input p-p differential voltage swing (AC-Coupled), voltage measured at the device input	—	200	—	2000	mV
V_L	Input launch amplitude (Voltage used to drive a signal across 40" of FR-4 trace)	—	500	—	—	mV_{PPD}
V_L	Input launch amplitude (Voltage used to drive a signal across 40" of FR-4 trace, pathological video pattern)	—	700	—	—	mV_{PPD}
R_{TERM}	PCML Input differential input impedance termination	—	80	100	120	Ω
V_{OH}	PCML single ended output logic-high	—	AV_{DDIO} - 0.05	—	AV_{DDIO}	V
V_{OD}	PCML p-p differential output swing	1,2,3,6	350	—	1750	mV
t_R/t_F	PCML output rise/fall time (20–80%)	6	—	60	—	ps
t_{DJ}	Deterministic output jitter	4	—	35	200	mUI
t_{RJ}	Random output jitter	4	—	6	9	mUI RMS
t_{PD}	Propagation delay	—	—	1	—	ns
$t_{SKEW, CH}$	Channel to Channel Skew	—	—	100	—	ps
V_{IH}	CMOS Input logic high	—	0.85 x DV_{DDIO}	—	—	V
V_{IF}	CMOS input logic floating state	—	0.25 x DV_{DDIO}	—	0.75 x DV_{DDIO}	V
V_{IL}	CMOS input logic low	—	—	—	0.15 x DV_{DDIO}	V

Table 1-4. Input/Output Electrical Characteristics (2 of 2)

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{OH}	CMOS output logic high	5	0.85 x DV_{DDIO}	—	—	V
V_{OL}	CMOS output logic low	5	—	—	0.15 x DV_{DDIO}	V

NOTES:

1. AV_{DDIO} must be 1.8V to achieve higher than 800 mV output swing.
2. Output swing is specified with output de-emphasis disabled.
3. Six output swing levels can be selected. Refer to Figure 2-5 for typical output swing levels for each setting.
4. Additive output jitter with minimal media length
5. Two-wire serial interface can drive 400 pF @ 100 kHz and 100 pF @ 400 kHz.
6. Measured using a CID pattern with a minimum CID length of 10 bits.

2.0 Typical Performance Characteristics

Unless noted otherwise, test conditions in this section are: AV_{DDIO} = 1.8V, 25°C case temperature, 800 mV differential input data swing, nominal (800 mV_{PPD}) output swing, PRBS 2^{15} - 1 test pattern at 4.25 Gbps, R_{LOAD} = 50Ω, short traces and/or cables.

Figure 2-1. Eye Diagram at 3.125 Gbps

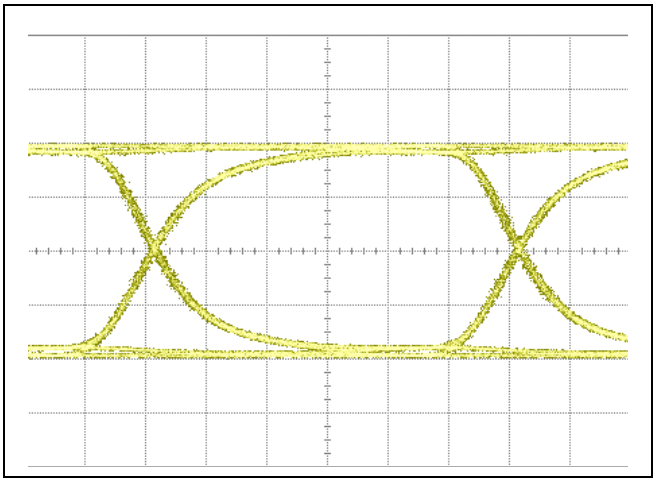


Figure 2-2. Eye Diagram after 15m of 24 AWG Cable at 4.25 Gbps

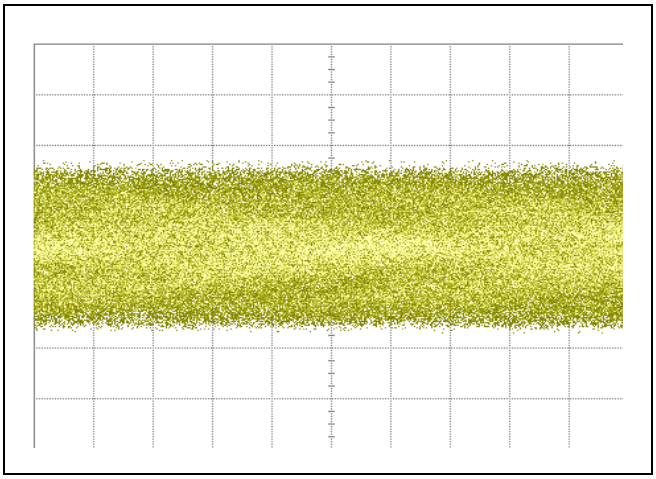


Figure 2-3. Eye Diagram at 4.25 Gbps

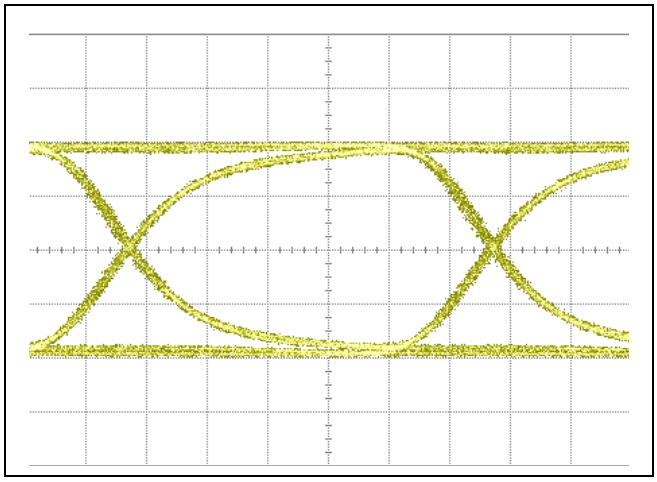


Figure 2-4. Eye Diagram after Equalizing 15m 24 AWG Cable at 4.25 Gbps

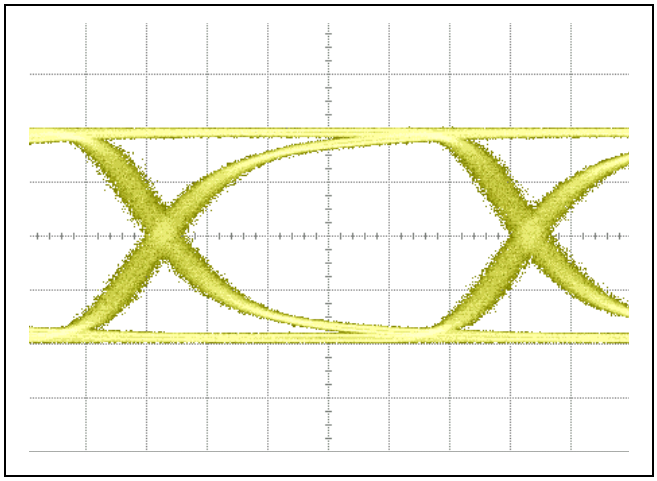


Figure 2-5. Differential Output Swing vs. OutctrlN[7:5] Setting as a Function of AV_{DDIO}

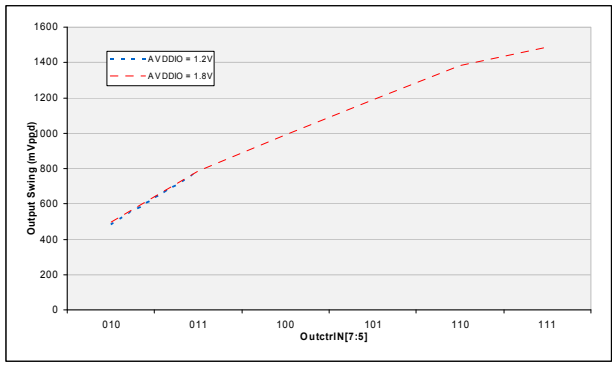


Figure 2-6. Random Jitter Distribution

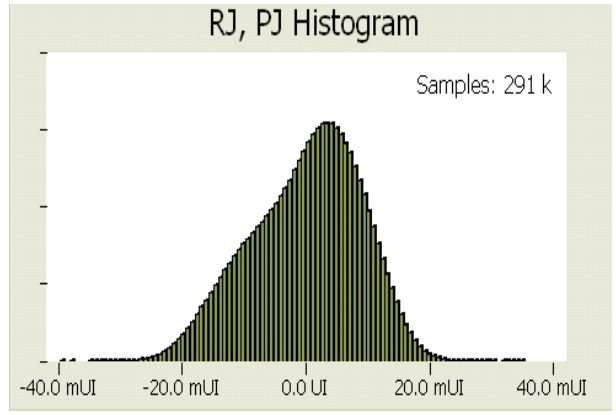


Figure 2-7. Output Waveform With COMWAKE OOB Signal

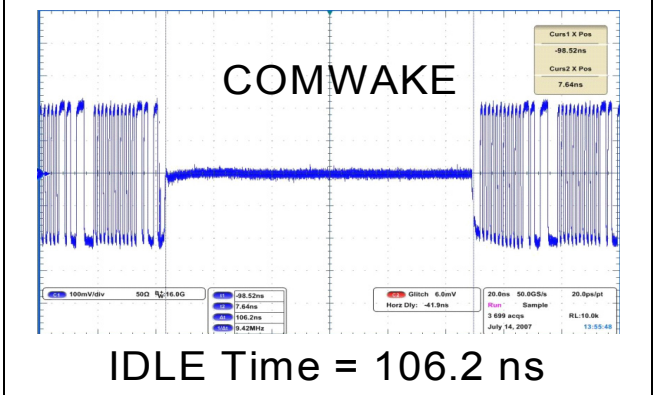


Figure 2-8. Jitter vs. Data Rate as a Function of 24 AWG Cable Length

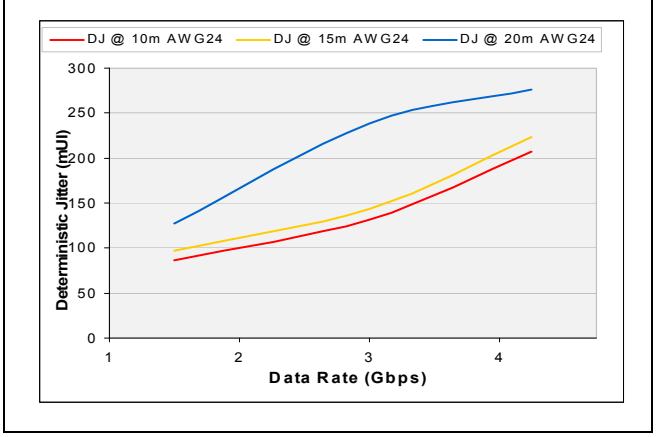


Figure 2-9. Bathtub Curve

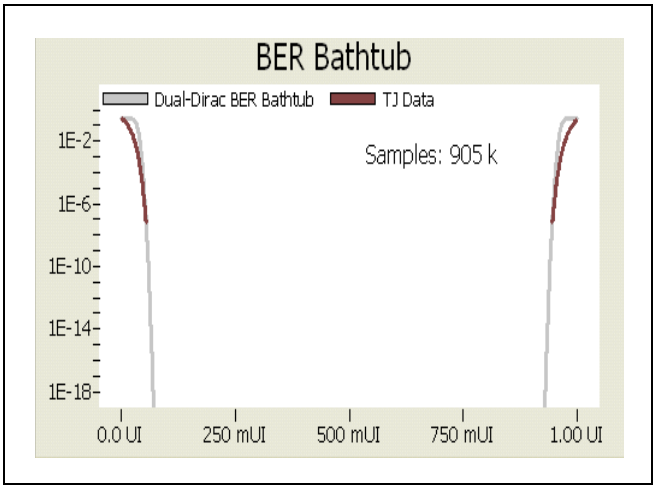


Figure 2-10. Deterministic Jitter vs. Launch Amplitude as a Function of Data Rate (After Equalizing 10m 24 AWG Cable)

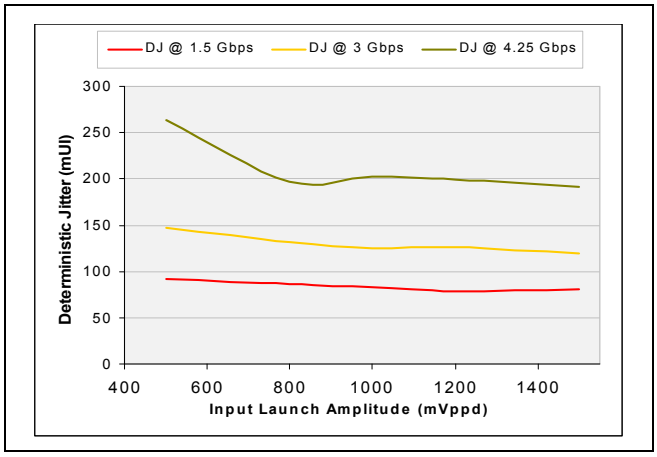
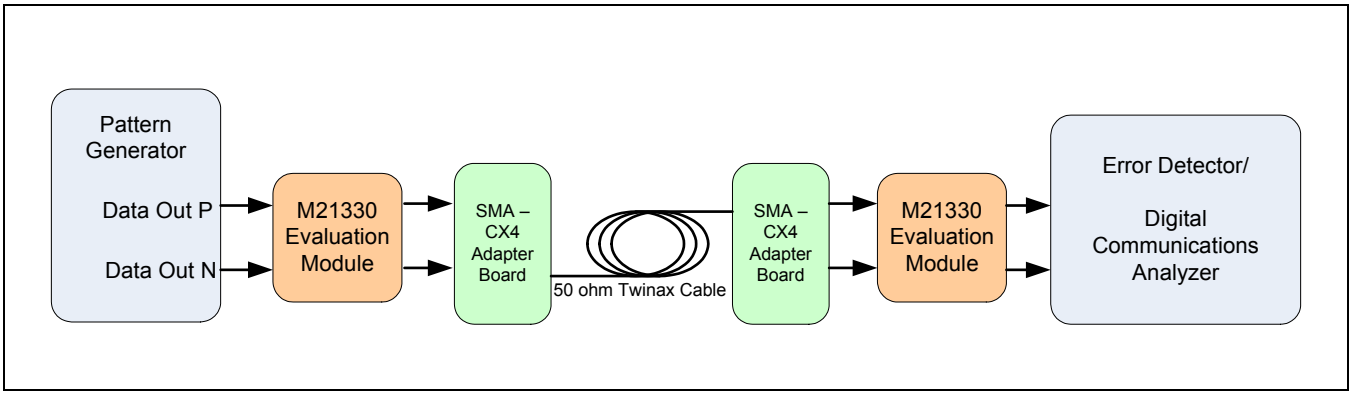


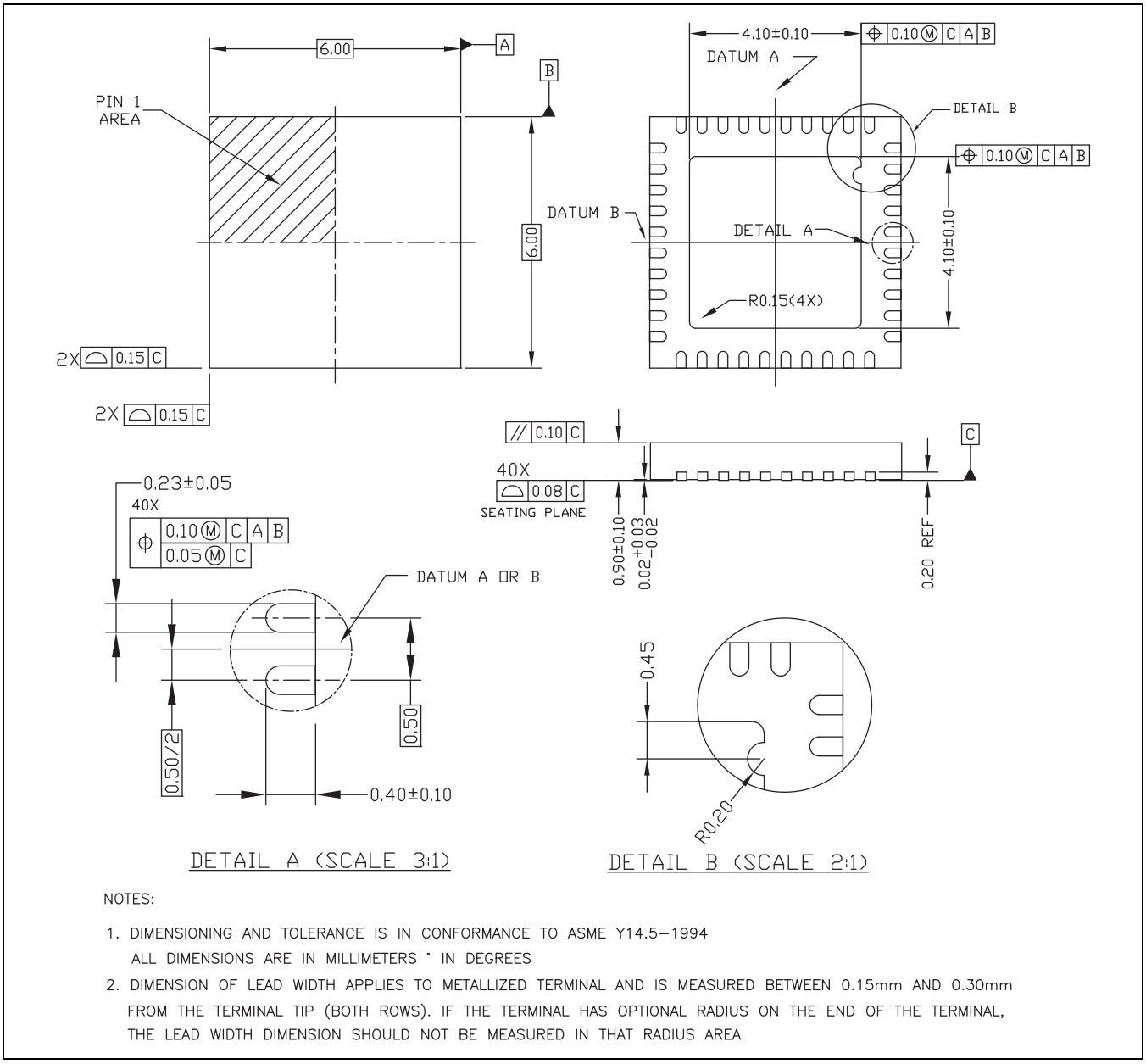
Figure 2-11. Input Equalization Test Setup Utilizing CX4 Cables



3.0 Package Description and Package Outline Drawing

The M21330 is assembled in a 6 x 6 mm, 40-pin QFN package. The package paddle is used to provide the device ground connection as well as a thermal path.

Figure 3-1. Package Outline Drawing



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Figure 3-2. Pinout Diagram (Top View Shown)

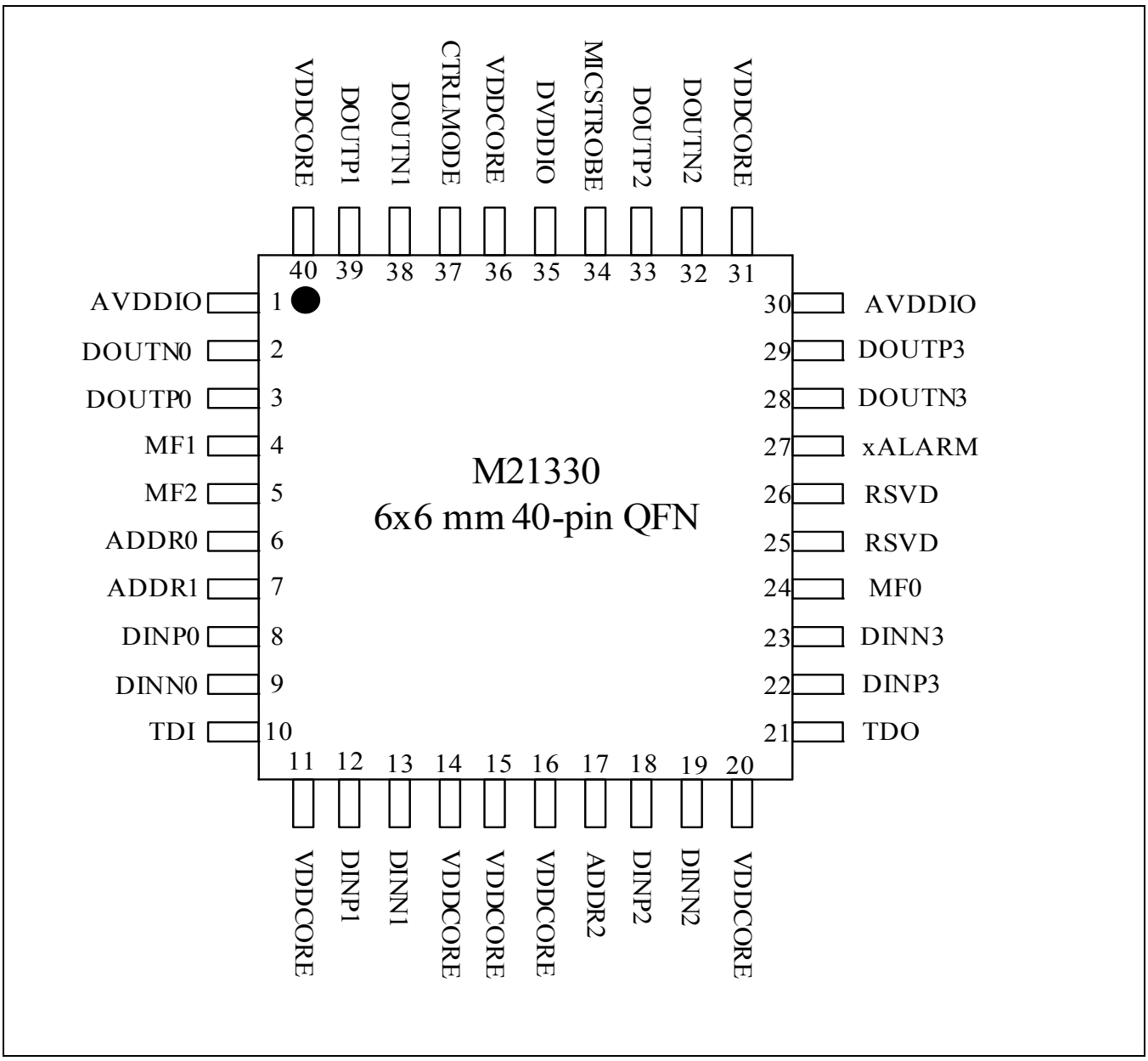


Table 3-1. M21330 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
AV_{DDIO}	1, 30	Power	Analog positive supply
DV_{DDIO}	35	Power	Digital positive supply
V_{DDCORE}	11,14,15,16, 20, 31, 36, 40	Power	Core positive supply
Package Paddle	GND	Ground	Device ground connection
MF0	24	CMOS Input	Multifunction Pin
MF1	4	CMOS Input	Multifunction Pin
MF2	5	CMOS Input	Multifunction Pin
ADDR0	6	CMOS Input	Two-wire interface address pin
ADDR1	7	CMOS Input	Two-wire interface address pin
ADDR2	17	CMOS Input	Two-wire interface address pin
TDI	10	CMOS Input	TDI for JTAG port
TDO	21	CMOS Output	TDO for JTAG port
MICSTROBE	34	CMOS Output	Strobe pin for MIC programming
CTRLMODE	37	CMOS Input	Control Mode Select
xALARM (1)	27	CMOS Output	Alarm Output Pin (1)
NC (2)	25, 26	No connect	Do not connect for M21330
DINP0	8	PCML Input	Channel 0 Input P
DINN0	9	PCML Input	Channel 0 Input N
DINP1	12	PCML Input	Channel 1 Input P
DINN1	13	PCML Input	Channel 1 Input N
DINP2	18	PCML Input	Channel 2 Input P
DINN2	19	PCML Input	Channel 2 Input N
DINP3	22	PCML Input	Channel 3 Input P
DINN3	23	PCML Input	Channel 3 Input N
DOUTP0	3	PCML Output	Channel 0 Output P
DOUTN0	2	PCML Output	Channel 0 Output N
DOUTP1	39	PCML Output	Channel 1 Output P
DOUTN1	38	PCML Output	Channel 1 Output N
DOUTP2	33	PCML Output	Channel 2 Output P
DOUTN2	32	PCML Output	Channel 2 Output N
DOUTP3	29	PCML Output	Channel 3 Output P
DOUTN3	28	PCML Output	Channel 3 Output N

NOTES:

1. xALARM is an open drain output and should be connected to an external 10 kΩ pull-up resistor in system designs.
2. Pins 25 and 26 are reserved for use as REFCLK connections on the M21330. MSPD recommends that a REFCLK circuit is designed into the system PCB if feasible to enable future use of the M21340 on the same PCB if necessary.

4.0 Control Registers Map and Descriptions

Table 4-1. M21330 Register Summary Table

Address	Register Name	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	Default	R/W
00h	devctrl0	MSPD							bpen0	00h	R/W
01h	devctrl1	standby	MSPD			ei_enable	MSPD			00h	R/W
02h	eqconfig	eqen		pd_dcoff	MSPD	pol_invert3	pol_invert2	pol_invert1	pol_invert0	C0h	R/W
03h	inctrl	in3pwr		in2pwr		in1pwr		in0pwr		FFh	R/W
04h	maneqlvl10	eqlvl1				eqlvl0				77h	R/W
05h	maneqlvl32	eqlvl3				eqlvl2				77h	R/W
06h	outctrl0	outlvl			MSPD	delvl		de_freq	MSPD	60h	R/W
07h	outctrl1	outlvl			MSPD	delvl		de_freq	MSPD	60h	R/W
08h	outctrl2	outlvl			MSPD	delvl		de_freq	MSPD	60h	R/W
09h	outctrl3	outlvl			MSPD	delvl		de_freq	MSPD	60h	R/W
0Ah	Alarm Configuration	MSPD		xLOS_en	MSPD				clear_alarm	CAh	R/W
0Bh	squelch	sqlevel		squelch	sqtime	MSPD			MSPD	C0h	R/W
0Ch	micreg	micdev					MSPD			00h	R/W
0Dh	xpointctrl	xstate3		xstate2		xstate1		xstate0		E4h	R/W
1Fh	Checksum	Seed value for MIC checksum								55h	R/W
24h	SDI Video_A 0	SDI Gain Channel 0				MSPD				00h	R/W
25h	SDI Video_A 1	SDI Gain Channel 1				MSPD				00h	R/W
26h	SDI Video_A 2	SDI Gain Channel 2				MSPD				00h	R/W
27h	SDI Video_A 3	SDI Gain Channel 3				MSPD				00h	R/W
28h	SDI Video_B 0	MSPD	SDI_en 0	MSPD						00h	R/W
29h	SDI Video_B 1	MSPD	SDI_en 1	MSPD						00h	R/W
2Ah	SDI Video_B 2	MSPD	SDI_en 2	MSPD						00h	R/W
2Bh	SDI Video_B 3	MSPD	SDI_en 3	MSPD						00h	R/W
80h	reset	reset								00h	R/W
81h	chip_id	chip_id								30h	R
82h	chip_rev	chip_rev								---*	R
83h	alarm	chan3 LOS	chan2 LOS	chan1 LOS	chan0 LOS	MSPD				N/A	R

Table 4-1. M21330 Register Summary Table

Address	Register Name	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	Default	R/W
87h	alarm_int	MSPD				alarm_mode	MSPD			04h	R/W
FCh	MIC Checksum	Computed Checksum Value								00h	R
* See register description for details on contents of the chip revision register (address 82h).											

Address 00h—Device Control 0

Bits	Type	Default	Label	Description
[7:1]	RSVD	0000000	MSPD	Reserved, set to '0000000'
0	R/W	0	bpen0	0: Equalizer optimized for standard cable. 1: Equalizer optimized for dispersion compensated cable and backplane traces.

Address 01h—Device Control 1

Bits	Type	Default	Label	Description
7	R/W	0	standby	0: Power Up—Normal operation. 1: Power Down—Standby operation.
[6:4]	R/W	000	MSPD	Reserved, set to 000b
3	R/W	0	ebi_enable	0: Disable electrical idle pass through mode. 1: Enable electrical idle pass through mode.
[2:0]	RSVD	000	MSPD	Reserved, set to 000

Address 02h—Equalizer Configuration

Bits	Type	Default	Label	Description
[7:6]	R/W	11	eqen	00: Disable input equalization. 01: Enable manual equalization mode. 10: Invalid setting—Do not use. 11: Enable adaptive equalization mode.
5	R/W	0	pd_dcoff	0: DC offset correction loop enabled. 1: DC offset correction loop disabled.
4	RSVD	0	MSPD	Reserved, set to 0.
3	R/W	0	pol_invert3	0: Normal polarity for input 3. 1: Invert polarity for input 3 (reverse INP and INN connections).
2	R/W	0	pol_invert2	0: Normal polarity for input 2. 1: Invert polarity for input 2 (reverse INP and INN connections).
1	R/W	0	pol_invert1	0: Normal polarity for input 1. 1: Invert polarity for input 1 (reverse INP and INN connections).
0	R/W	0	pol_invert0	0: Normal polarity for input 0. 1: Invert polarity for input 0 (reverse INP and INN connections).

Address 03h—Input Buffer Control

Bits	Type	Default	Label	Description
[7:6]	R/W	11	in3pwr	00: Power down input 3 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 01: Power down input 3 with 50Ω single-ended (100Ω differential) termination. 10: Enable input 3 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 11: Enable input 3 with 50Ω single-ended (100Ω differential) termination.
[5:4]	R/W	11	in2pwr	00: Power down input 2 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 01: Power down input 2 with 50Ω single-ended (100Ω differential) termination. 10: Enable input 2 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 11: Enable input 2 with 50Ω single-ended (100Ω differential) termination.
[3:2]	R/W	11	in1pwr	00: Power down input 1 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 01: Power down input 1 with 50Ω single-ended (100Ω differential) termination. 10: Enable input 1 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 11: Enable input 1 with 50Ω single-ended (100Ω differential) termination.
[1:0]	R/W	11	in0pwr	00: Power down input 0 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 01: Power down input 0 with 50Ω single-ended (100Ω differential) termination. 10: Enable input 0 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 11: Enable input 0 with 50Ω single-ended (100Ω differential) termination.

Address 04h—Input 1-0 Manual Equalization Setting

Bits	Type	Default	Label	Description
[7:4]	R/W	0111	eqlvl1	1111: Minimum equalization 1110: Low equalization .... 1000: Medium equalization 0000: Medium equalization .... 0110: High equalization 0111: Maximum equalization Input equalization is programmed using 2's complement encoding, with 1111 being the lowest eq setting and 0111 being the highest eq setting.
[3:0]	R/W	0111	eqlvl0	1111: Minimum equalization 1110: Low equalization .... 1000: Medium equalization 0000: Medium equalization .... 0110: High equalization 0111: Maximum equalization Input equalization is programmed using 2's complement encoding, with 1111 being the lowest eq setting and 0111 being the highest eq setting.

Address 05h—Input 3-2 Manual Equalization Setting

Bits	Type	Default	Label	Description
[7:4]	R/W	0111	eqlvl3	1111: Minimum equalization 1110: Low equalization .... 1000: Medium equalization 0000: Medium equalization .... 0110: High equalization 0111: Maximum equalization Input equalization is programmed using 2's complement encoding, with 1111 being the lowest eq setting and 0111 being the highest eq setting.
[3:0]	R/W	0111	eqlvl2	1111: Minimum equalization 1110: Low equalization .... 1000: Medium equalization 0000: Medium equalization .... 0110: High equalization 0111: Maximum equalization Input equalization is programmed using 2's complement encoding, with 1111 being the lowest eq setting and 0111 being the highest eq setting.

Address 06h, 07h, 08h, 09h—Output Buffer Control (add 06h = output 0, add 07h = output 1, add 08h = output 2, add 09h = output 3)

Bits	Type	Default	Label	Description
[7:5]	R/W	011	outlvl	Sets the swing level for the output buffer. 00x: Power Down ... 010: Minimum Output Swing ... 111: Maximum Output Swing
4	RSVD	0	MSPD	Reserved, set to 0
[3:2]	R/W	00	delvl	Controls output de-emphasis. 00: Output de-emphasis disabled. 01: Approximately 2 dB de-emphasis. 10: Approximately 4 dB de-emphasis. 11: Approximately 6 dB de-emphasis.
1	R/W	0	de_freq	0: Nominal time constant for output de-emphasis. 1: High time constant for output de-emphasis.
0	RSVD	0	MSPD	Reserved, set to 0.

Address 0Ah—Alarm Configuration

Bits	Type	Default	Label	Description
[7:6]	RSVD	11	MSPD	Reserved, set to 11.
5	R/W	0	xLOS_en	0: Enable LOS circuit 1: Disable and power down LOS circuit
[4:1]	RSVD	0101	MSPD	Reserved, set to 0101.
0	R/W	0	clear_alarm	0: Normal operation. 1: Clear alarm registers. (Note: To clear alarms, set this bit to '1', then set back to '0' for normal operation)

Address 0Bh—Squelch Control

Bits	Type	Default	Label	Description
[7:6]	R/W	11	sqlevel	00: Never squelch output. 01: Output H on LOS (recommended for DC coupled outputs). 10: Output L on LOS (recommended for DC coupled outputs). 11: Output electrical idle level on LOS (recommended for AC coupled outputs).
5	R/W	0	squelch	0: Normal operation. 1: Force squelch to level determined by sqlevel setting (bits [7:6]).
4	R/W	0	sqtime	Squelch enable time. 0: Declare LOS after approx 5 µs of no input data. 1: Declare LOS after approx 1 µs of no input data.
[3:0]	RSVD	0000	MSPD	Reserved, set to 0000.

Address 0Ch—Memory Interface Control Mode Registers

Bits	Type	Default	Label	Description
[7:3]	R/W	00000	micdev	Identifies the number of M21330 devices on the bus for Memory Interface Control mode. 00000: No additional M21330 devices on serial buss ... 11010: Maximum number(26) of additional M21330 devices on serial buss
[2:0]	RSVD	000	MSPD	Reserved, set to 000.

Address 0Dh—Crosspoint Switch Control

Bits	Type	Default	Label	Description
[7:6]	R/W	11	xstate3	00: Route input 0 to output 3. 01: Route input 1 to output 3. 10: Route input 2 to output 3. 11: Route input 3 to output 3.
[5:4]	R/W	10	xstate2	00: Route input 0 to output 2. 01: Route input 1 to output 2. 10: Route input 2 to output 2. 11: Route input 3 to output 2.
[3:2]	R/W	01	xstate1	00: Route input 0 to output 1. 01: Route input 1 to output 1. 10: Route input 2 to output 1. 11: Route input 3 to output 1.
[1:0]	R/W	00	xstate0	00: Route input 0 to output 0. 01: Route input 1 to output 0. 10: Route input 2 to output 0. 11: Route input 3 to output 0.

Address 1Fh—Checksum

Bits	Type	Default	Label	Description
[7:0]	R/W	55h	Checksum	Used with MIC mode. Adjust the value of register 1Fh so that the sum of the value of registers from 00h-2Fh is equal to 2Eh in order to compute a valid checksum after the EEPROM download.

Address 24h, 25h, 26h, 27h—SDI Video configuration A (add 24h = channel 0, add 25h = channel 1, add 26h = channel 2, add 27h = channel 3)

Bits	Type	Default	Label	Description
[7:4]	R/W	0000	SDI Gain	Sets the amount of low frequency gain when bit 6 of register 28h/29h/2Ah2Bh is set to 1. If bit 6 of register 28h/29h/2Ah/2Bh is set to 0, the low frequency gain is automatically determined by the device. (For applications that use 8B/10B and PRBS data patterns, this register should be left at it's default value.) 0111: minimum low frequency gain .... 0000: nominal low frequency gain 1000: nominal low frequency gain .... 1111: highest low frequency gain (recommended setting for SDI video to enable best performance with pathological data patterns)
[3:0]	R/W	0000	MSPD	Reserved, set to 0000.

Address 28h, 29h, 2Ah, 2Bh—SDI Video Configuration B
(add 28h = channel 0, add 29h = channel 1, add 2Ah = channel 2, add 2Bh = channel 3)

Bits	Type	Default	Label	Description
7	R/W	0	MSPD	Reserved, set to 0.
6	R/W	0	SDI_en	0: disable manual low frequency gain setting using SDI video configuration A register (recommended for non-SDI video applications) 1: enable manual low frequency gain setting using SDI video configuration A register (recommended for SDI video applications)
[5:0]	R/W	0	MSPD	Reserved, set to 00000.

Address 80h—Reset

Bits	Type	Default	Label	Description
[7:0]	R/W	00h	reset	00: Normal operation. AA: Reset mode. (Note, to reset the device, write AAh followed by a second write of 00h)

Address 81h—Chip Identification

Bits	Type	Default	Label	Description
[7:0]	R	30h	chip_id	Device identification register.

Address 82h—Chip Revision

Bits	Type	Default	Label	Description
[7:0]	R	---	chip_rev	Device revision register. M21330G-14 = 05h

Address 83h—Alarm Status

Bits	Type	Default	Label	Description
7	R	N/A	chan3 LOS	0: No alarm for input channel 3. 1: LOS alarm for input channel 3.
6	R	N/A	chan2 LOS	0: No alarm for input channel 2. 1: LOS alarm for input channel 2.
5	R	N/A	chan1 LOS	0: No alarm for input channel 1. 1: LOS alarm for input channel 1.
4	R	N/A	chan0 LOS	0: No alarm for input channel 0. 1: LOS alarm for input channel 0.
[3:0]	RSVD	N/A	MSPD	Reserved, may contain undefined values when read.

Address 87h—Alarm Interrupt Mode Control

Bits	Type	Default	Label	Description
[7:4]	RSVD	0000	MSPD	Reserved, set to 0000.
3	R/W	0	alarm_mode	0: Interrupt mode for xALARM output pin. 1: Status mode for xALARM output pin.
[2:0]	RSVD	100	MSPD	Reserved, set to 100.

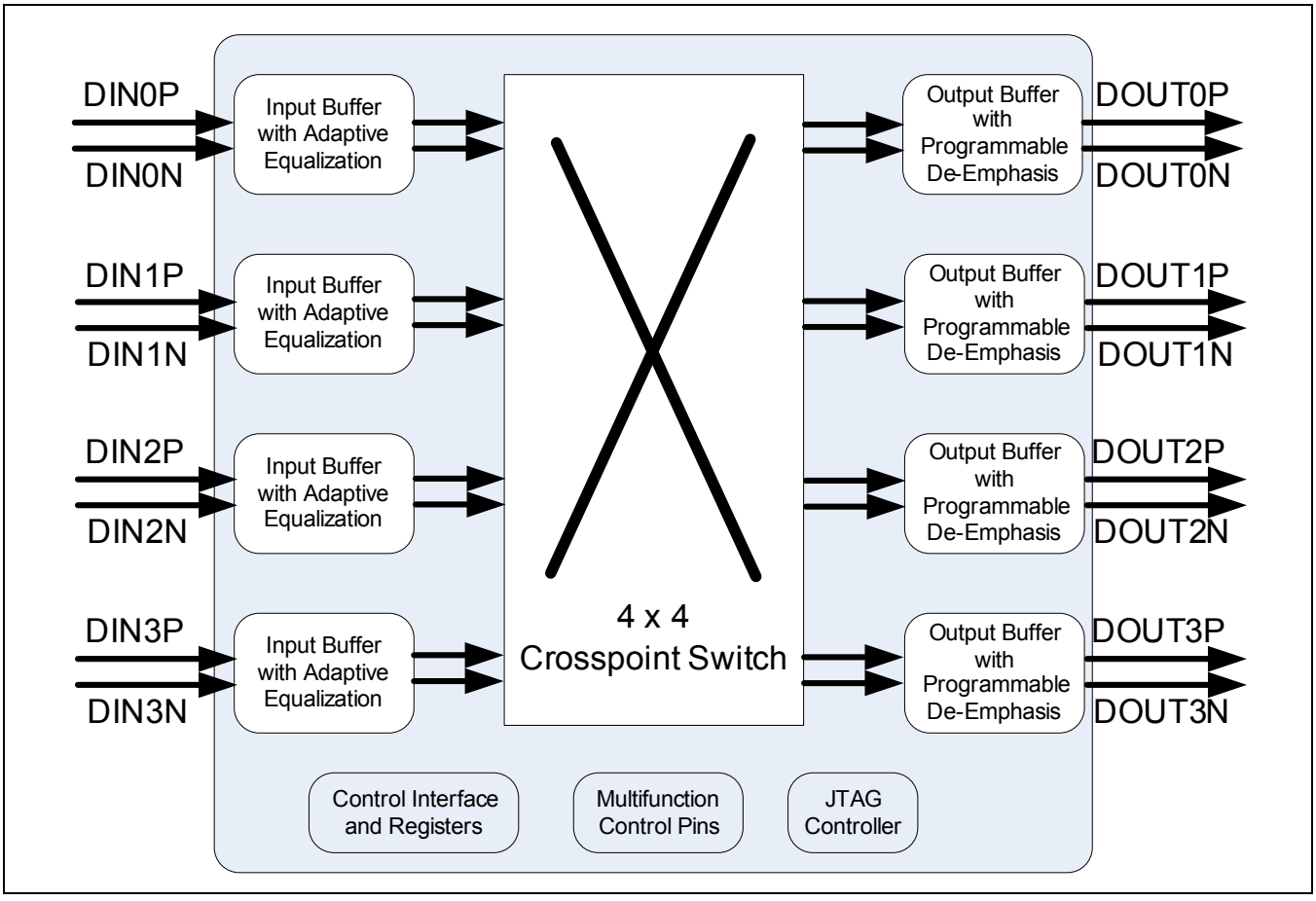
Address FCh—MIC Checksum

Bits	Type	Default	Label	Description
[7:0]	R	00h	MIC Checksum Calculated Value	After an EEPROM download, this register contains the checksum calculated value. If this value is not equal to 2Eh after an MIC download, there was either an issue with the download or the checksum seed value in register 1Fh is not correct.

5.0 Functional Description

The M21330 is a quad channel device with adaptive input equalization, programmable output de-emphasis, and an embedded 4x4 crosspoint switch matrix. Details on various functionality and features are described in the following sections.

Figure 5-1. Functional Block Diagram



5.1 Power Supply

The M21330 includes three distinct power supply domains: V_{DDCORE}, AV_{DDIO}, and DV_{DDIO}.

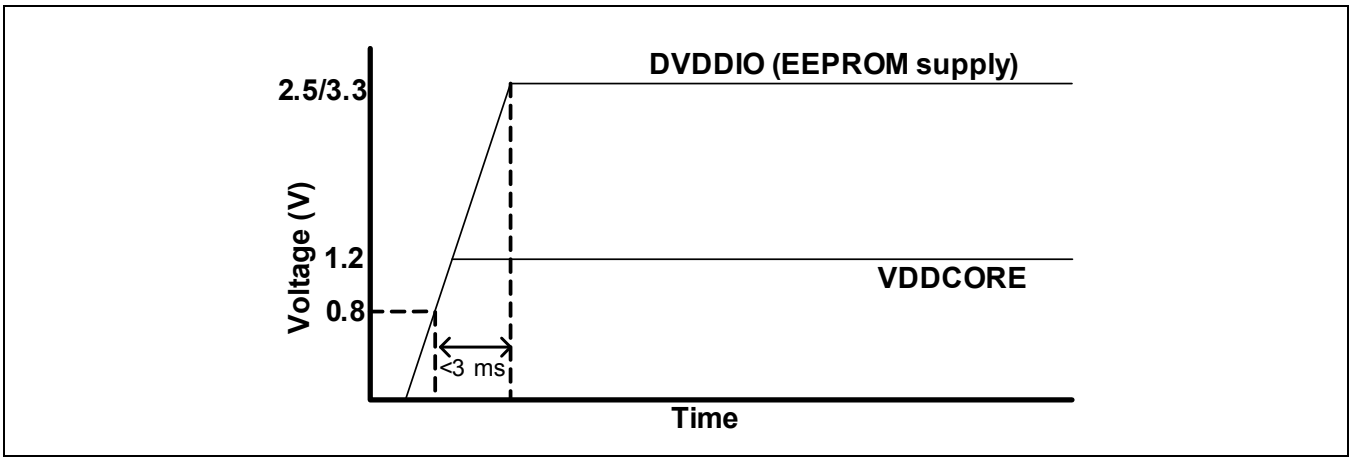
V_{DDCORE} powers the analog and digital core circuitry in the device, and must be set to 1.2V.

AV_{DDIO} powers the input/output circuits in the device, and can be set to either 1.2V or 1.8V. Note that to achieve output swing levels higher than 800 mV_{PPD}, AV_{DDIO} must be set to 1.8V.

DV_{DDIO} powers the digital circuitry within the device, and can be set to 1.2V, 1.8V, 2.5V, or 3.3V to allow for interface with various external digital devices. It is recommended that DV_{DDIO} is connected to the same voltage level as any digital devices that are used to control the M21330.

There are no power supply sequencing requirements for V_{DDCORE}, AV_{DDIO}, or DV_{DDIO} in the M21330. When the M21330 is operated in memory interface control (MIC) mode, the external EEPROM must be powered up and stable before the M21330 is powered up to ensure that the automatic register download occurs without errors. When the M21330 is operated in memory interface control (MIC) mode, the EEPROM must be powered up and stable within 3 ms of V_{DDCORE} reaching approximately 0.8V to ensure that the register download from the EEPROM is robust. Note that in MIC mode, the startup current on DV_{DDIO} could be as high as 50 mA until V_{DDCORE} is powered up. The device will issue a power on reset (POR) when V_{DDCORE} reaches approximately 0.8V during the power supply ramp. After the POR is complete, the device will poll the ADDR pins to determine which control mode the device is configured for. If the device is configured for MIC operation, it will attempt to communicate with the on-board EEPROM for register download immediately after the POR is complete. If the EEPROM does not respond within approximately 3 ms after the POR, the M21330 will stop trying to communicate with the EEPROM and the MIC download will fail. See below for the recommended power supply ramp up timing in MIC mode.

Figure 5-2. Recommended Power Supply Ramp up in MIC Mode



5.2 Multifunction Pins

The M21330 contains a series of multifunction pins, whose functionality changes depending on the control mode configuration of the device. Each multifunction pin is designed to support three different logic levels, high, low, and floating state. The floating state logic level is achieved by floating the pin, connecting it to a high impedance source, or driving to a voltage equal to $DV_{DDIO}/2$. The table below summarizes the functionality of the multifunction pins (MF[2:0]) for each control mode. More details on the functionality of the MF pins are included in the description sections for each control mode.

Table 5-1. Multifunction Pins

Pin	Functionality in Software/Memory Interface Control Mode	Functionality in JTAG/Boundary Scan Mode
MF0	Memory Interface Control enable	F
MF1	SDA	TMS
MF2	SCL	TCLK

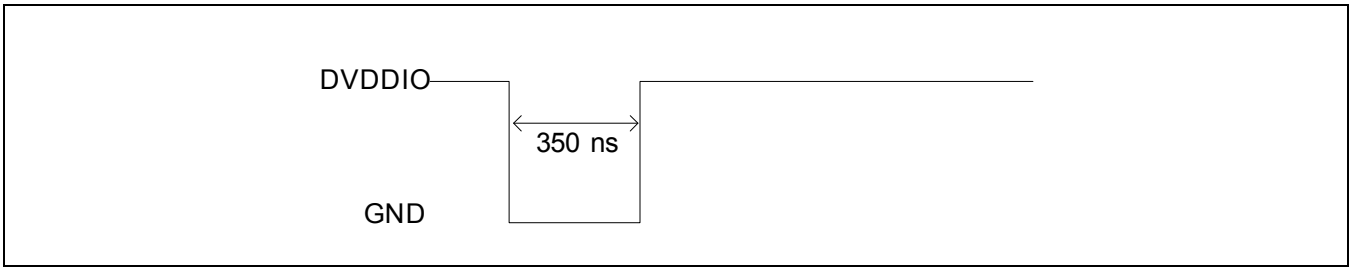
5.3 Input and Output Buffers

The input buffers in the M21330 are designed to work with AC coupled input signals, and support operation with a wide range of AC coupling capacitor values. Applications that use PRBS and/or 8b/10b encoded data will typically use AC coupling capacitors with a value of 0.1 µF. SDI video applications will typically use AC coupling capacitors with a value of 4.7 µF or larger. The output buffers are designed with PCML logic, and can operate with either AC coupled or DC coupled systems. Register 03h can be used to enable/power-down the input buffers and also select the desired input termination for each channel. The input buffer should not be configured in a high-impedance state when data needs to be passed through the M21330. For typical operation, the input buffer should be enabled with a 50Ω single ended (100Ω differential) termination.

5.4 LOS Alarm

There is signal detect circuit that will assert an alarm if the signal level at the input of the device is lower than approximately 100 mV_{PPD}. Once asserted, the alarm will remain asserted until the signal is above approximately 200 mV_{PPD}. There is hysteresis between the assert and de-assert levels to prevent chattering of the LOS alarm. When the input voltage level is between 100 mV_{PPD} and 200 mV_{PPD}, the LOS alarm can be high or low. The LOS circuit should be disabled when used with strings of 1010 data that last for more than approximately 3 µs to avoid false LOS alarms. By default, the xALARM hardware pin operates as an interrupt signal and will generate an interrupt signal with a pulse width of approximately 350 ns when there is an alarm on any input channel. See Figure 5-3 below for an example of the timing for the xALARM interrupt signal. To configure the device so that the xALARM pin acts as a status indicator rather than an interrupt signal, register address 87h[3] can be used.

Figure 5-3. Timing of xAlarm Interrupt Signal



5.5 Input Equalization

Each input channel of the M21330 includes an input equalizer, designed to compensate for bandwidth limitations of 50Ω twinaxial cables. The equalizer can operate in the adaptive mode or in a manual mode, where a fixed equalization setting is selected. In the adaptive equalization mode, the equalizer will select the optimal equalization

setting for the cable/backplane type and length connected to the input. The input equalization is configured through register addresses 00h, 02h, 04h, and 05h.

5.6 Output De-emphasis

Each output buffer of the M21330 includes a de-emphasis circuit that is manually configured by the user. There is approximately 6 dB of de-emphasis available, and the de-emphasis levels are selectable. The output de-emphasis is controlled through register addresses 06h, 07h, 08h, and 09h.

5.7 Electrical Idle Pass-through

Some protocols, such as SATA/SAS and PCIe, define a third logic state at the common mode for transmission of an electrical idle level. In SAS/SATA systems, OOB signals such as COMRESET, COMWAKE, and COMSAS utilize burst and idle levels for communication. The M21330 is designed to pass the electrical idle (EI) through the device to support SATA/SAS and PCIe protocol requirements. When the EI feature of the M21330 is enabled, the device will detect and pass EI signals with minimal distortion of the signal. LOS should be set to "never squelch" when the EI circuit is enabled to allow the device to detect data bursts quickly after electrical idle periods that last longer than approximately 5 µs. The EI feature is enabled/disabled through register address 01h, and is disabled by default.

Note: If the M21330 is used in a PCIe application that requires support of the L0s power management state, contact your Mindspeed representative for details on using the device in this application.

5.8 Squelch

To avoid random chattering of the output due to noise when there is no signal present at the inputs, the M21330 includes a squelch feature to automatically inhibit the output when there is a LOS alarm. This feature can be disabled if desired, and there is an option to inhibit to either logic H, logic L, or the EI common mode level on squelch. In addition to the automatic squelch feature, a manual squelch can be forced using register 0Bh. LOS should be set to "never squelch" when the EI circuit is enabled to allow the device to detect data bursts quickly after electrical idle periods that last longer than approximately 5 µs.

5.9 Operation in SDI Video Applications

Pathological data patterns found in SDI digital video applications stress the control circuitry in the adaptive equalization loops of the M21330 and limit the equalization performance of the device. For this reason, the adaptive equalization of the M21330 should be disabled and the manual equalization mode of the device should be used in SDI video applications. With the M21330 in manual equalization mode, the device can pass pathological video data error-free for SD-SDI, HD-SDI, and 3G-SDI data rates. In addition to putting the device into manual equalization mode, the following register settings should be set in applications when the device is used with pathological video data patterns.

Table 5-2. Recommended Register Settings for SDI Video Applications

Register Name	Register Address	Default Value	Recommended Value	Description
Equalizer Configuration	02h	C0h	40h	Disable adaptive equalization
Input 1/0 Manual Equalization Setting	04h	77h	Determined by the system channel	Set manual equalization level
Input 3/2 Manual Equalization Setting	05h	77h	Determined by the system channel	Set manual equalization level
SDI Video Configuration A, Input 0	24h	00h	F0h	Increase low frequency gain
SDI Video Configuration A, Input 1	25h	00h	F0h	Increase low frequency gain
SDI Video Configuration A, Input 2	26h	00h	F0h	Increase low frequency gain
SDI Video Configuration A, Input 3	27h	00h	F0h	Increase low frequency gain
SDI Video Configuration B, Input 0	28h	00h	40h	Enable manual setting of low frequency gain
SDI Video Configuration A, Input 1	29h	00h	40h	Enable manual setting of low frequency gain
SDI Video Configuration B, Input 2	2Ah	00h	40h	Enable manual setting of low frequency gain
SDI Video Configuration B, Input 3	2Bh	00h	40h	Enable manual setting of low frequency gain

For optimum performance with long strings of consecutive bits found in pathological patterns, 4.7 µF or larger value AC coupling capacitors should be used on the inputs and outputs of the M21330.

5.10 Control Options

There are two control modes available for the M21330. To control using a two wire, I^2C compatible programming interface, the device can be configured for Software Interface Control (SIC). The M21330 can also self configure from an external EEPROM when the Memory Interface Control (MIC) mode is selected. In addition to the three control modes, the M21330 also supports boundary scan through a JTAG port.

To select the control mode, configure the CTRLMODE and MF0 pins as shown:

Table 5-3. Control Mode

Operating Mode	CTRLMODE Pin	MF0 Pin
Software Interface Control	H	L
Memory Interface Control (EEPROM)	H	H
Boundary Scan	F	F

5.11 Boundary Scan Operation

In order to test external connections to and from the M21330, the device includes support for boundary scan through a JTAG port when configured for boundary scan mode. The device is put in this mode by setting MF0 = F and CTRLMODE = F. When the device is in boundary scan mode, the following pins are used for the JTAG port.

Table 5-4. Boundary Scan Mode Functionality

Pin Name	Pin Number	Functionality in Boundary Scan Mode
MF1	4	TMS
MF2	5	TCLK
TDI	10	TDI
TDO	21	TDO

For the input pins, the M21330 supports AC-coupled interconnects with edge rates faster than 20 ns. The clock rate should be less than 10 MHz. The input scan cells are built as single-ended, self-referenced edge detectors, such that for a differential input two signals are created (allowing for independent testing of p/n connections). For the output pins, the scan signal is injected into the main signal path and will be driven out differentially (one digital signal is used per differential output). The scan signal is muxed in before the 4x4 crosspoint core, so if a particular crosspoint switch state is being used during the scan test, the scan signal will be switched as well.

5.12 Software Interface Control Mode Operation

With the M21330 configured for Software Interface Control (SIC) operation, the functionality of the M21330 is controlled through register settings. Refer to Table 4-1 for a full description of the registers available within the M21330. To access the registers, an I^2C compatible, two-wire programming interface is available in the device. SDA is used for data transfer and is mapped to MF1 when the M21330 is configured for SIC operation. SCL is used for the clock signal and is mapped to the pin MF2 when the M21330 is configured for SIC operation. The two-wire device address is determined by the status of the pins ADDR[2:0]. The table below shows the address for each combination of settings for ADDR[2:0].

Table 5-5. Two Wire Serial Device Address List

ADDR[2:0] Setting	7-bit Device address
LLL	0100000
LLH	0100001
LHL	0100010
LHH	0100011
HLL	0100100
HLH	0100101
HHL	0100110
HHH	0100111
LLF	0101000
LHF	0101001

Table 5-5. Two Wire Serial Device Address List

ADDR[2:0] Setting	7-bit Device address
HLF	0101010
HHF	0101011
LFL	0101100
LFH	0101101
HFL	0101110
HFH	0101111
FLL	0110000
FLH	0110001
FHL	0110010
FHH	0110011
LFF	0110100
HFF	0110101
FLF	0110110
FHF	0110111
FFL	0111000
FFH	0111001
FFF	0111010

The two wire programming interface is designed to drive 400 pF @ 100 kHz and 100 pF @ 400 kHz operation. During a write operation, data is latched into the M21330 registers on the rising edge of SCL during the acknowledge phase (ACK) of communication. Refer to the I^2C bus specification standard for timing information that is applicable to the two-wire programming interface.

5.13 Memory Interface Control Mode Operation

With the M21330 configured for Memory Interface Control (MIC) operation, a single M21330 device or an array of M21330 devices can self configure from a single EEPROM with a two wire serial programming interface upon device power up. After the M21330 has self configured, the device reverts to SIC operation to allow an optional host controller to modify the register settings of the M21330.

If the M21330 is configured for MIC operation at power up, the lead M21330 interface operates as a temporary two wire quasi-master operating at 100 kHz when downloading from external memory and 400 kHz when configuring other M21330 devices. In an array of M21330 devices, only one device should be configured for MIC operation, and subsequent devices in the array should be configured for SIC operation. All devices in an array will receive the same configuration. As a quasi-master, the M21330 will drive pin MICSTROBE low during power up to indicate that the self configuration is in process. When the M21330 device begins to self configure, it will read the contents of an external EEPROM and configure its registers accordingly. The expected EEPROM device address is 1010000b, and the M21330 quasi master device address should be set to 0100000b. The EEPROM should be powered up and stable before the M21330 is powered up in MIC mode to ensure that the automatic register download occurs without errors. Please refer to Figure 5-2 for the recommended power supply ramp up timing in MIC mode.

Register 1Fh is used to load the checksum seed value. The checksum seed value should be selected such that the 8 LSB of the sum of the register values from address 00h through 2Fh is equal to 2Eh. After the download from the EEPROM, the checksum value is computed and written into register address FCh. If the checksum value is equal to 2Eh, then this is recognized as a valid checksum and the quasi-master device will continue to program other device on the interface buss. If the checksum value is not equal to 2Eh, the quasi master device will repeat the download process and look for the correct checksum value up to 512 times before timing out. If the correct checksum value is not detected, the quasi-master device will not configure any additional devices on the interface bus, but the quasi-master will be programed with the contents of the EEPROM.

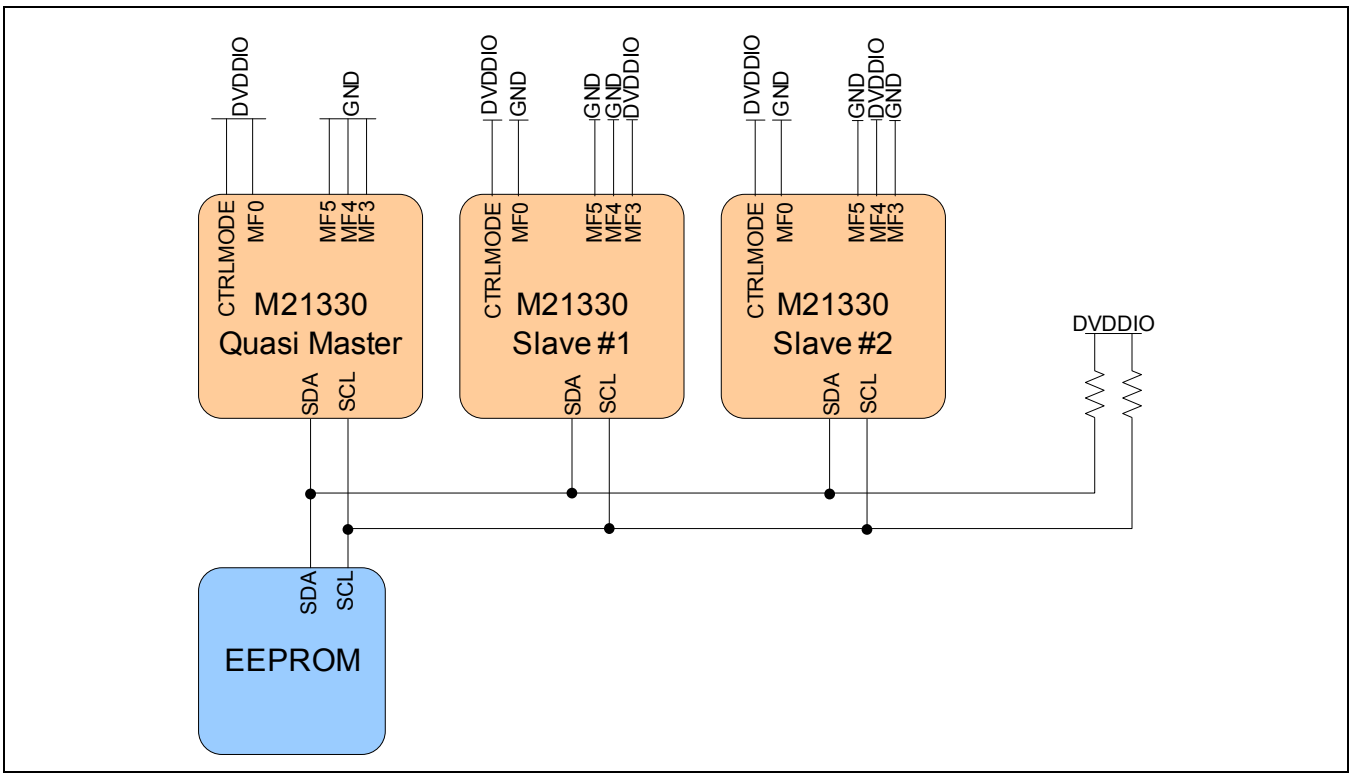
Register address 0Ch is used to identify the number of M21330 that will be self configured by the quasi master in MIC mode. When multiple M21330 devices are self configured in an array, the quasi master M21330 device will copy its register contents into other devices in the array sequentially using a 400 kHz interface bus. The devices in the array must have sequential programming addresses, starting with 0100000b for the quasi master device. After the last device in the M21330 has been configured, the pin MICSTROBE on the quasi master M21330 will be driven high, and the device will revert to SIC operation.

If the MIC mode is used in conjunction with an external host controller, the two wire interface on the host controller must not interrupt the programming buss while self configuration is taking place. This can be ensured by timing out the host controller for N x 0.8 seconds (N= number of M21330 devices in the self configure array), by monitoring the SDA/SCL buss for activity, or by monitoring the MICSTROBE pin on the quasi master device.

The device will issue a power on reset (POR) when V_{DDCORE} reaches approximately 0.8V during the power supply ramp. After the POR is complete, the device will poll the ADDR pins to determine which control mode the device is configured for. If the device is configured for MIC operation, it will attempt to communicate with the onboard EEPROM for register download immediately after the POR is complete. If there is no response from the EEPROM within approximately 3 ms after the POR is complete, the M21330 will stop trying to communicate with the EEPROM and the register download will fail. Please refer to Figure 5-2 for the recommended power supply ramp up timing in MIC mode.

Figure 5-4 below illustrates the connections necessary to self-configure three M21330 devices using MIC mode. The first M21330 device (quasi master) is configured for operation in MIC mode, and the other two devices (Slave #1 and Slave #2) are configured for SIC operation with consecutive programming addresses..

Figure 5-4. M21330 MIC System Diagram



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