MSW3103-310 & MSW3104-301

SP3T PIN Diode Switch

Rev. V1

Features

- Wide Frequency Range: 50 MHz to 3 GHz, in 2 bands
- Surface Mount SP3T Switch in Compact Outline:
  - 8 mm L x 5 mm W x 2.5 mm H
- Higher Average Power Handling than Plastic Packaged
  - MMIC Switches: 100 W CW
- High RF Peak Power: 500 W
- Low Insertion Loss: 0.5 dB
- High IIP3: 65 dBm
- Operates From Positive Voltage Only: 5 V & -28 V to -125 V
- RoHS Compliant

Case Style CS310

Applications

- High Power Transmit/Receive (TR) Switching
- Active Receiver Protection

Description

The MSW3103-310 and MSW3104-310 series of surface mount silicon PIN diode SP3T switches can be used for high power transmit/receive (TR) symmetrical switching or active receiver protection from 50 MHz to 1 GHz (MSW3103-310) or from 400 MHz to 3 GHz (MSW3104-310). These switches are manufactured using Aeroflex/ Metelics proven hybrid manufacturing process incorporating high voltage PIN diodes and passive devices integrated on a ceramic substrate. These low profiles, compact, surface mount components (8 mm L x 8 mm W x 2.5 mm H) offer superior small and large signal performance compared to that of MMIC devices in QFN packages. The SP3T switches are designed in a symmetrical topology to enable switched RF port to be used as the high-input-power-handling port, to minimize insertion loss and to maximize isolation performance. The very low thermal resistance (< 25 ºC/W) of the NIP diodes in these devices enables them to reliably handle RF incident power levels of 50 dBm CW and RF peak incident power levels of 53 dBm in cold switching applications. The thick I layers of the NIP diodes (> 40 µm), coupled with their long minority carrier lifetime (> 0.3 µs), produces input third order intercept point (IIP3) greater than 65 dBm.

These MSW3103-310, MSW3104-310 SP3T switches are designed to be used in high average and peak power switch applications, operating from 50 MHz to 3 GHz in two bands, which utilize high volume, surface mount, solder re-flow manufacturing. These products are durable and capable of reliably operating in military, commercial, and industrial environments. The devices are RoHS compliant.

DS-xxxxxxx

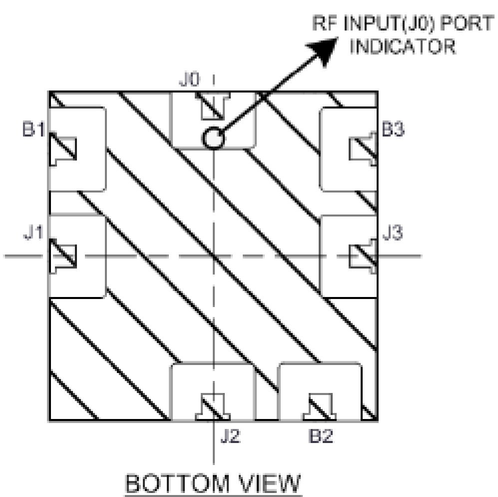
Environmental Capabilities

The MSW3103-310 and MSW3104-310 SP3T switches are capable of meeting the environmental requirements of MIL-STD-202 and MIL-STD-750.

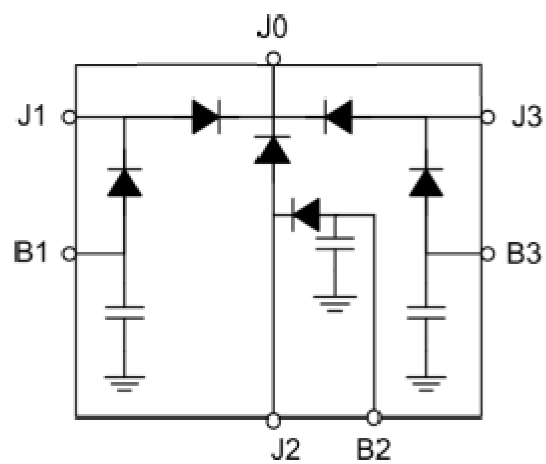
ESD and Moisture Sensitivity Level Rating

PIN Diode Switches are susceptible to ESD conditions as with all semiconductors. The ESD rating for this device is Class 1C, HBM. The moisture sensitivity level rating for this device is MSL 1.

Pin Out



Schematic



Truth Table

$+V_{CC1}$ = 5 V and $+V_{CC2}$ = 28 V (Unless otherwise noted)

Path J0 – J1	Path J0 – J2	Path J0 – J3	J1 Bias V1A	J2 Bias V2A	J3 Bias V3A	B1 Bias V1B	B2 Bias V2B	B3 Bias V3B	J0 Bias V3B
Low Loss (Bias State 1)	High Isolation	High Isolation	5 V 100 mA	-28 V -25 mA	-28 V -25 mA	-28V 0 mA	0 V 25 mA	0 V 25 mA	0 V -100 mA
High Isolation	Low Loss (Bias State 2)	High Isolation	-28 V -25 mA	5 V 100 mA	-28 V -25 mA	0 V 25 mA	-28 V 0 mA	0 V 25 mA	0 V -100 mA
High Isolation	High Isolation	Low Loss (Bias State 3)	-28 V -25 mA	-28 V -25 mA	5 V 100 mA	0 V 25 mA	0 V 25 mA	-28 V 0 mA	0 V -100 mA

MSW3103-310Electrical Specifications

Z_0 = 50 Ω, P_{IN}= 0 dBm, T_A= 25 ºC (Unless Otherwise Defined)

Parameter	Symbol	Test Conditions	Min. Value	Typ. Value	Max. Value	Units
Frequency	F		50	-	1000	MHz
Insertion Loss (Note 1)	IL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2 Bias state 3: port J0 to J3	-	0.4	0.6	dB
Return Loss (Note 1)	RL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2 Bias state 3: port J0 to J3	18	20	-	dB
Isolation (Note 1)	Isol	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2 Bias state 3: port J0 to J3	34	36	-	dB
CW Incident Power (Note 2)	P_{inc}(CW)	source & load VSWR = 1.5:1	-	-	50	dBm
Peak Incident Power (Note 2)	P_{inc}(Pk)	source & load VSWR = 1.5:1, pulse width = 10 µs, duty cycle = 1 %	-	-	53	dBm
Switching Time (Note 3)	t_{sw}	10 % - 90 % RF voltage, TTL rep rate = 100 kHz	-	2	3	µs
Input 3rd Order Intercept Point	IIP3	F_1 = 500 MHz, F_2 = 510 MHz, P_1 = P_2 = 10 dBm, measured on path biased to low loss state	60	64	-	dBm

MSW3104-310 Electrical Specifications

Z_0 = 50 Ω, P_{IN}= 0 dBm, T_A= 25 ºC (Unless Otherwise Defined)

Parameter	Symbol	Test Conditions	Min. Value	Typ. Value	Max. Value	Units
Frequency	F		400	-	3000	MHz
Insertion Loss (Note 1)	IL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2 Bias state 3: port J0 to J3	-	0.6	0.8	dB
Return Loss (Note 1)	RL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2 Bias state 3: port J0 to J3	14	15	-	dB
Isolation (Note 1)	Isol	Bias state 1: port J0 to J2, J0 to J3 Bias state 2: port J0 to J1, J0 to J3 Bias state 3: port J0 to J1, J0 to J2	32	34	-	dB
CW Incident Power (Note 2)	P_{inc}(CW)	source & load VSWR = 1.5:1	-	-	50	dBm
Peak Incident Power (Note 2)	P_{inc}(Pk)	source & load VSWR = 1.5:1, pulse width = 10 µs, duty cycle = 1 %	-	-	53	dBm
Switching Time (Note 3)	t_{sw}	10 % - 90 % RF voltage, TTL rep rate = 100 kHz	-	1.5	2	µs
Input 3rd Order Intercept Point	IIP3	F_1 = 2.00 GHz, F_2 = 2.01 GHz, P_1 = P_2 = 10 dBm, measured on path biased to low loss state	60	64	-	dBm

Notes:

1 Switching Speed (50 % TTL – 10/90 % RF Voltage) is a function of the PIN diode driver performance as well as the characteristics of the diode. An RC "current spiking network" is used on the driver output to provide a transient current to rapidly remove stored charge from the PIN diode. Typical component values are: R = 50 to 220 Ω and C = 470 to 1,000 pF. MACOMs MPD3T28125-700 is the recommended PIN diode driver to interface with the MSW3103-310, MSW3104-310 SP3T switches. Its data sheet may be found at

2 PIN diode DC reverse voltage to maintain high resistance in the OFF PIN diode is determined by RF frequency, incident power, and VSWR as well as by the characteristics of the diode. The minimum reverse bias voltage values are provided in this datasheet. The input signal level applied for small signal testing is approximately 0 dBm.

RF Bias Network Component Values

P/N	F (MHz)	DC Blocking Capacitors	Inductors	RF Bypass Capacitors	Secondary Bypass Capacitors	Current Limiting Resistor R1	Current Limiting Resistors R2, R3, R4
MSW3103-310	50 – 1,000	0.1 µF	4.7 µH	0.1 µF	0.1 µF	39 Ω	Selection based on the reverse bias voltage
MSW3104-310	400 – 3,000	27 pF	82 nH	270 pF	270 pF	39 Ω	Selection based on the reverse bias voltage

Bias States and Biasing Conditions

Bias State	Path J0 – J1	Path J0 – J2	Path J0 – J3	J1 Bias V1A	J2 Bias V2A	J3 Bias V3A	B1 Bias V1B	B2 Bias V2B	B3 Bias V3B	J0 Bias V3B
Bias State 1	Low Loss	High Isolation	High Isolation	5 V 100 mA	-28 V -25 mA	-28 V -25 mA	-28V 0 mA	0 V 25 mA	0 V 25 mA	0 V -100 mA
Bias State 2	High Isolation	Low Loss	High Isolation	-28 V -25 mA	5 V 100 mA	-28 V -25 mA	0 V 25 mA	-28 V 0 mA	0 V 25 mA	0 V -100 mA
Bias State 3	High Isolation	High Isolation	Low Loss	-28 V -25 mA	-28 V -25 mA	5 V 100 mA	0 V 25 mA	0 V 25 mA	-28 V 0 mA	0 V -100 mA

Minimum Reverse Bias Voltage at TX, RX, DC Ports vs. Signal Frequency

P_{INC} = 100 W CW, Z_0 = 50Ω with 1.5:1 VSWR

Part Number	F = 20 MHz	F = 100 MHz	F = 200 MHz	F = 400 MHz	F = 1 GHz	F = 3 GHz
MSW3103-310	-125 V	-125 V	-125 V	100 V	-85 V	NA
MSW3104-310	NA	NA	NA	-85 V	-65 V	-28 V

Note: "NA" denotes the switch is not recommended for use in that frequency band.

Absolute Maximum Ratings

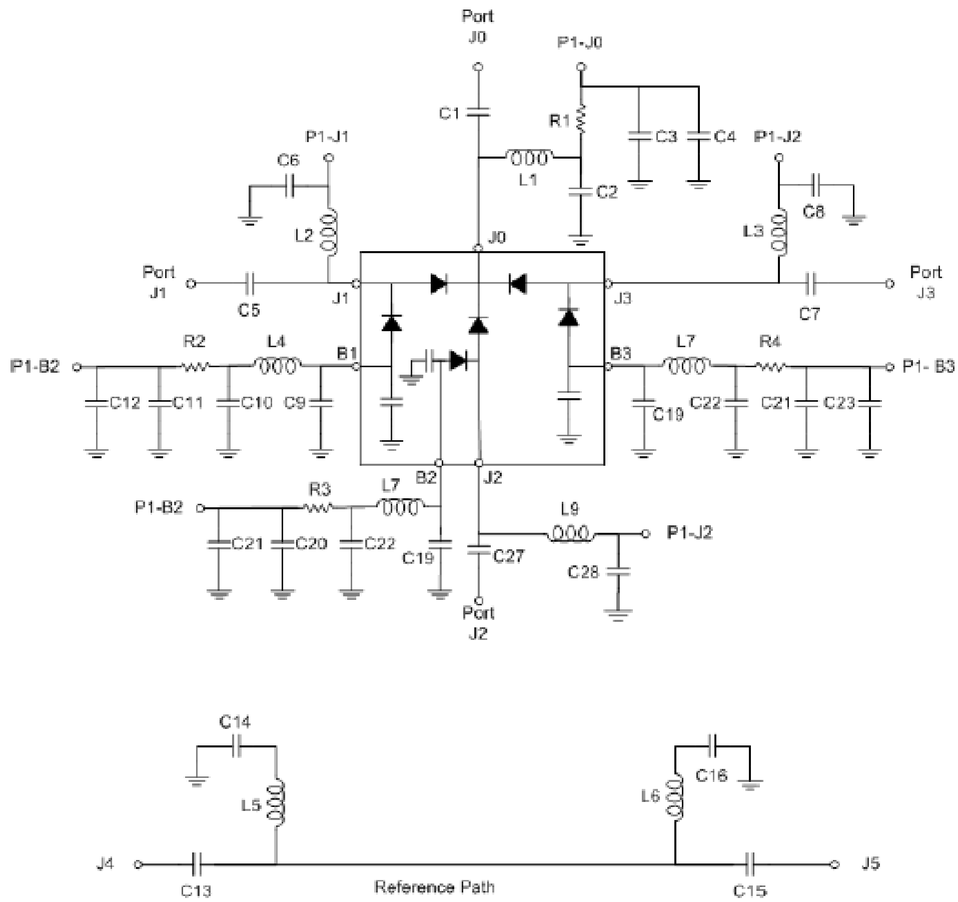
Z_0 = 50 Ω, T_A = +25 ºC (Unless Otherwise Defined)

Parameter	Conditions	Absolute Maximum Value
Forward Current - J1, J2, J3 Port		250 mA
Forward Current - B1, B2, B3 Port		150 mA
Reverse Voltage - J1, J2, J3 Port		125 V
Reverse Voltage - B1, B2, B3 Port		125 V
Forward Diode Voltage	I_F = 250 mA	1.2 V
Operating Temperature		-65 ºC to 125 ºC
Storage Temperature		-65 ºC to 150 ºC
Junction Temperature		175 ºC
Assembly Temperature		260 ºC for 10 s
CW Incident Power Handling – J0 or J1, J2, J3 Port (Note	Source & load VSWR = 1.5 :1, T_{CASE} = 85 ºC, cold switching	50 dBm
Peak Incident Power Handling – J0 or J1, J2, J3 Port (Note 1)	Source & load VSWR = 1.5 :1, T_{CASE} = 85 ºC, cold switching, pulse width = 10 µs, duty cycle = 1 %	53 dBm
Total Dissipated RF & DC Power (Note 1)	T_{CASE} = 85 ºC, cold switching	8.5 W

Notes:

1 Backside RF and DC grounding area of device must be completely solder-attached to RF circuit board vias for proper electrical and thermal circuit grounding.

SP3T Switch Evaluation Board Schematic



Evaluation Board Description

Below is the description of MSW310x-310 SP3T series shunt switch module control using MPD3T28125-701 three channel pin diode driver. The switch module can also be controlled by using external voltage sources accordingly.

The MSW310x-310 series shunt three throw switch can be fully controlled using external power sources. Each power source is connected to bias the series diode and the shunt diode of the switch arms. A typical symmetric switch with a power source interface is shown below. The switch is controlled to operate in one of three oper-ational states, which are called State 1, State 2 and State 3. In the descriptions of States 1, 2 and 3 (below), it is assumed that +VCC1 = 5 V and VCC2 = -28 V.

State 1

In State 1, the path from port J0 to J1 is in its low insertion loss condition. The paths from port J0 to port J2, and port J0 to port J3, are in their high isolation states. In state 1 the series PIN diode between the J0 and J1 is forward biased by applying +5 V to the J1 bias input port. J0 port is held at 0 V/ Ground thru a 39 Ω resistor R1. The magni-tude of the resultant bias current through the forward-biased diode is primarily determined by the voltage ap-plied to the J1 bias port (5 V nominal), the magnitude of the forward voltage across the PIN diode and the resistance of R1 at J0 port. This current is nominally 100 mA. Port B1 is connected to –28 V bias to reverse bias the shunt diode between the J1 and B1 ports. At the same time, the shunt PIN diodes connected between port J2 and B2 and between port J3 and B3 are also forward biased by applying a 0 V bias voltage at port B2 and B3, The magnitudes of the bias currents through these diodes are primarily determined by the voltage applied (-28 V) to the J2 and J3 bias ports, the magnitudes of the forward voltage across each of the PIN diodes and the current limiting resistances R3 and R4 (nominally 1.1 kΩ). These currents are nominally 25 mA each. Under this condition, the series PIN diodes connected between the J0 and J2 ports, between the J0 and J3 ports and the shunt diode between J1 and B1 are each reverse biased.

The reverse bias voltage applied to non-conducting diodes must be sufficiently large to maintain each diode in its non- conducting, high impedance state when a large RF signal voltage may be present. For example, assume a large RF signal is present in the J0- to-J1 path. The reverse bias voltage across each of the series diodes in the other paths is the arithmetic difference of the bias voltage applied to the J2 bias port or J3 bias port and the DC forward voltage of the forward-biased J0-to-J1 series PIN diode. The minimum voltage required to maintain the series diode between ports J0 and J2 and the series diode between ports J0 and J3 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the series diode's anode, the frequency of the RF signal and the characteristics of the series diode, among other factors. The minimum reverse bias voltage may be calculated as described in the "Minimum Reverse Bias Voltage" section.

Truth table for SP3T switch operation with PIN diode driver (MPD3T28125-701) Interface

Note 1 : V_{HIGH} = +5V , V_{LOW} = 0 V

RF State	Path J0 – J1	Path J0 – J2	Path J0 – J3	J1 Bias V1A	J2 Bias V2A	J3 Bias V3A	B1 Bias V1B	B2 Bias V2B	B3 Bias V3B	J0 Bias V3B
State 1	Low Loss	High Isolation	High Isolation	5 V 100 mA	-28 V -25 mA	-28 V -25 mA	-28V 0 mA	0 V 25 mA	0 V 25 mA	0 V -100 mA
State 2	High Isolation	Low Loss	High Isolation	-28 V -25 mA	5 V 100 mA	-28 V -25 mA	0 V 25 mA	-28 V 0 mA	0 V 25 mA	0 V -100 mA
State 3	High Isolation	High Isolation	Low Loss	-28 V -25 mA	-28 V -25 mA	5 V 100 mA	0 V 25 mA	0 V 25 mA	-28 V 0 mA	0 V -100 mA

State 2

In State 2, the path from port J0 to J2 is in its low insertion loss condition. The path from port J0 to port J1, and the path from port J0 to port J3, are in their high isolation states.

In State 2, the series PIN diode between the J0 and J2 is forward biased by applying +5 V to the J2 bias input port and 0 v to J0 port, while reverse-biasing the series diodes connected from port J0 to port J1, and from port J0 to port J3. The magnitude of the resultant bias current through the forward-biased diode is primarily determined by the voltage applied to the J2 bias port (5 V nominal), the magnitude of the forward voltage across the PIN diode and the resistance of R1 (39 Ω). This current is nominally 100 mA.

At the same time, the shunt PIN diodes connected between port J1 and B1 and between port J3 and B3 are also forward biased by applying a high bias voltage, nominally -28 V, to the J1 and J3 bias ports and 0 V to the B1 and B3 bias ports. The magnitudes of the bias currents through these diodes are primarily determined by the voltage applied to the J1 and J3 bias ports, the magnitudes of the forward voltage across each of the PIN diodes and the resistances of R2 and R4 (nominally1.1 kΩ). These currents are nominally 25 mA each. Under this condition, the series PIN diodes connected between the J0 and J1 ports, between the J0 and J3 ports and the shunt diode between J2 and B2 are each reverse biased.

The reverse bias voltage applied to non-conducting diodes must be sufficiently large to maintain each diode in its non-conducting, high impedance state when a large RF signal voltage may be present. For example, assume a large RF signal is present in the J0-to-J2 path. The reverse bias voltage across each of the series diodes in the other paths is the arithmetic difference of the bias voltage applied to the J1 bias port or J3 bias port and the DC forward voltage of the forward-biased J0-to-J2 series PIN diode.

State 3

In State 3, the path from port J0 to J3 is in its low insertion loss condition. The path from port J0 to port J1, and the path from port J0 to port J2, is in their high isolation states.

In State 3, the series PIN diode between the J0 and J3 ports is forward biased by applying 5 V to the J3 bias input port, while reverse-biasing the series diodes connected from port J0 to port J1, and from port J0 to port J2. The magnitude of the resultant bias current through the forward-biased diode is primarily determined by the voltage applied to the J3 bias port (5 V nominal), the magnitude of the forward voltage across the PIN diode and the resistance of R1 (39 Ω). This current is nominally 100 mA.

At the same time, the shunt PIN diodes connected between port J1 and B1 and between port J3 and B2 are also forward biased by applying a high bias voltage, nominally -28 V, to the J1 and J2 bias ports (P1-J1, P1-J2) and 0 V to the B1 and B2 bias ports (P1-B2, P1-B2). The magnitudes of the bias currents through these diodes are primarily determined by the voltage applied to the J1 and J2 bias ports, the magnitudes of the forward voltage across each of the PIN diodes and the resis-tances of R2 and R3 (nominally 1.1 kΩ). These currents are nominally 25 mA each. Under this condition, the series PIN diodes connected between the J0 and J1 ports, between the J0 and J2 ports and the shunt diode between J3 and B3 are each reverse biased.

The reverse bias voltage applied to non-conducting diodes must be sufficiently large to maintain each diode in its non-conducting, high impedance state when a large RF signal voltage may be present. For example, assume a large RF signal is present in the J0-to-J3 path. The reverse bias voltage across each of the series diodes in the other paths is the arithmetic difference of the bias voltage applied to the J1 bias port or J2 bias port and the DC forward voltage of the forward-biased J0-to-J3 series PIN diode.

Calculation of Resistor Values

The magnitude of the forward bias current applied to the series diode is set by the magnitude of the supply voltage $+V_{CC1}$, which is nominally 5 V, the value of resistor R1 and the forward voltage of the series diode, V_{DIODE}, among other factors. Given the desired current value, the resistance is given by the formula:

$$R_1 = \frac{(+V_{CC1} - V_{DIODE})}{I_{BIAS}}$$

The magnitude of the current through the shunt diode is set by the magnitude of the supply voltage $+V_{CC2}$, the value of resistor in series with the shunt diode (R_2 or R_4 or R_5)and the forward voltage of the shunt diode, VDIODE, among other factors. Given the desired current value, this resistance is given by the formula:

$$R_{SHUNT} = \frac{(+V_{CC2} - 0.3 - V_{DIODE})}{I_{BIAS}}$$

It is important to note that the switch module evaluation board, as supplied from the factory, is not capable of handling RF input signals larger than 45 dBm. If per-formance of the switch under larger input signals is to be evaluated, an adequate heat sink must be properly attached to the evaluation board, and several of the passive components on the board must be changed in order to safely handle the dissipated power as well as the high bias voltage necessary for proper performance. Contact the factory for recommended components and heat sink.

Minimum Reverse Bias Voltage

The minimum reverse bias voltage required to maintain a PIN diode out of conduction in the presence of a large RF signal is given by:

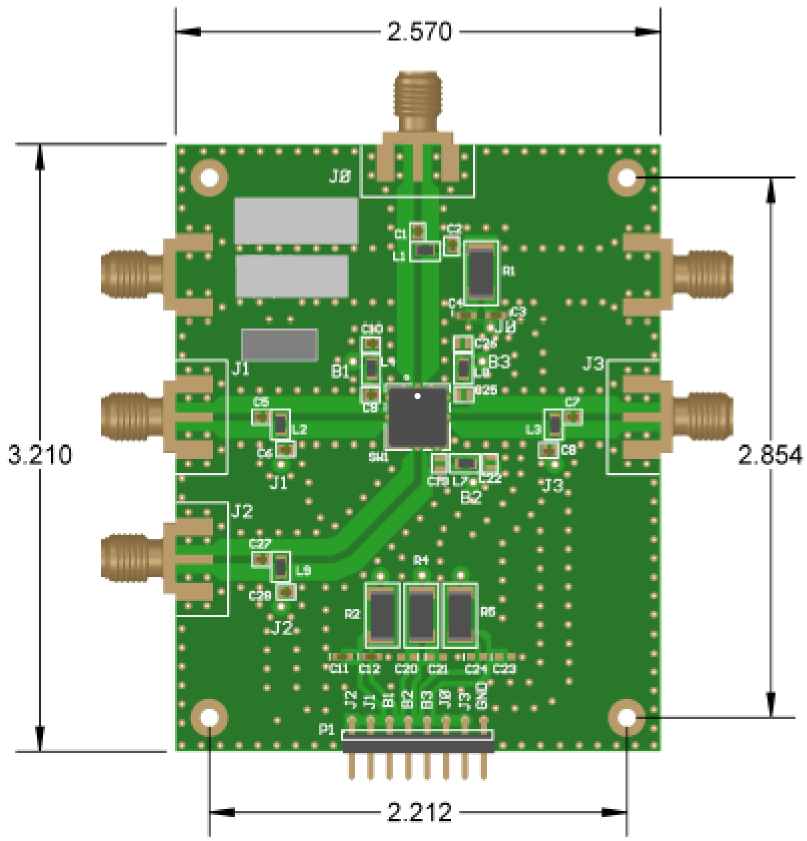
$$|V_{DC}| = \frac{|V_{RF}|}{\sqrt{1 + \left[\left(\frac{0.0142 \times f_{MHz} \times W_{mils}^2}{V_{RF} \times \sqrt{D}}\right) \times \left(1 + \sqrt{1 + \left(\frac{0.056 \times V_{RF} \times \sqrt{D}}{W_{mils}}\right)^2}\right)\right]^2}}$$

where

$\lvert V_{DC}\rvert$	=	magnitude of the minimum DC reverse bias voltage
$\lvert V_{RF}\rvert$	=	magnitude of the peak RF voltage (including the effects of VSWR)
f_{MHz}	=	lowest RF signal frequency expressed in MHz
D	=	duty factor of the RF signal
W_{mils}	=	thickness of the diode I layer, expressed in mils (thousandths of an inch)

(Caverly, R. H. & Hiller, G., "Establishing the Minimum Reverse Bias for a p-i-n Diode in a High-Power Switch", IEEE Transactions on Microwave Theory and Techniques, Vol. 38, No. 12, December 1990)

SP3T Switch Evaluation Board Layout



APPLIES TO THE FOLLOWING EVAL BOARDS:
CS310 - BAND 1 / BAND 2 / BAND 3

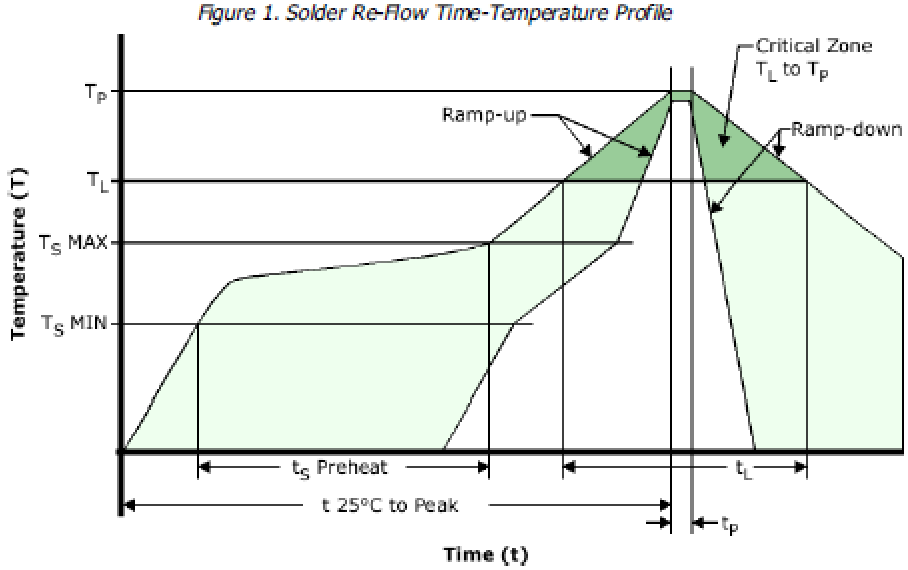
Assembly Instructions

The MSW3103-301 and MSW3104-301 switches are capable of being placed onto circuit boards with pick and place manu-facturing equipment from tube or tape-reel dispensing. The devices are attached to the circuit board using conventional solder re-flow or wave soldering procedures with RoHS type or Sn60/Pb40-type solders per Table I and Figure I.

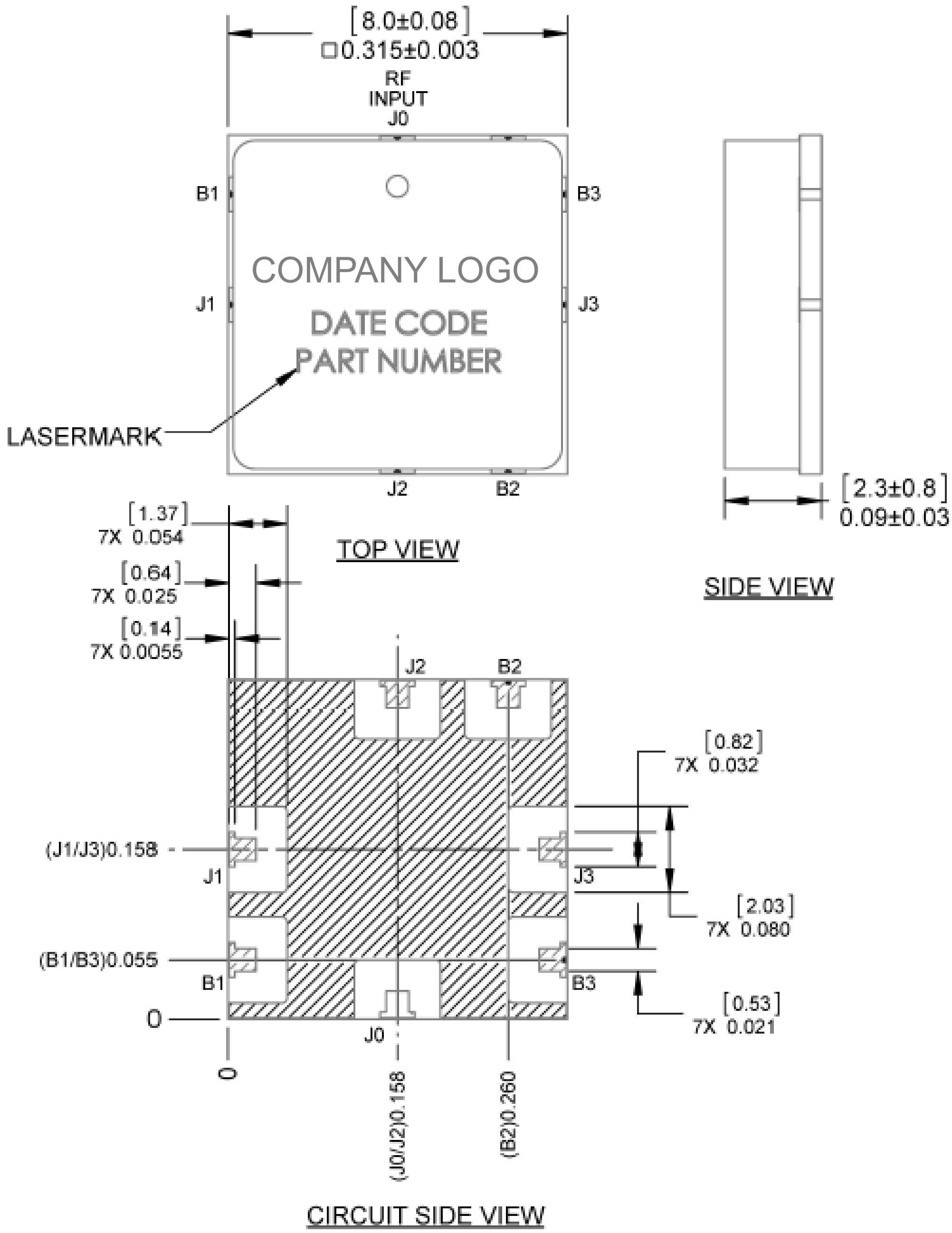
Table 1. Time-Temperature Profile for Sn60/Pb40 or RoHS Type Solders

Profile Feature	SnPb Solder Assembly	Pb-Free Solder Assembly
Average Ramp-Up Rate (T_L to T_P)	3 °C /second maximum	3 °C /second maximum
Preheat: - Temperature Min (T_{SMIN}) - Temperature Max (T_{SMAX}) - Time (min to max)(t_s)	 100 °C 150 °C 60-120 s	 150 °C 200 °C 60-180 s
T_{SMAX} to T_L - Ramp-Up Rate		3 °C/s maximum
Time Maintained Above: - Temperature (T_L) - Time (t_L)	183 °C 60-150 s	217 °C 60-150 s
Peak temperature (T_P)	225 +0/-5 °C	260 +0/-5 °C
Time Within 5 °C of Actual Peak Temperature (t_p)	10 – 30 s	20 – 40 s
Ramp-Down Rate	6 °C /s maximum	6 °C /s maximum
Time 25 °C to Peak Temperature	6 minutes maximum	8 minutes maximum

Figure 1. Solder Re-Flow Time-Temperature Profile



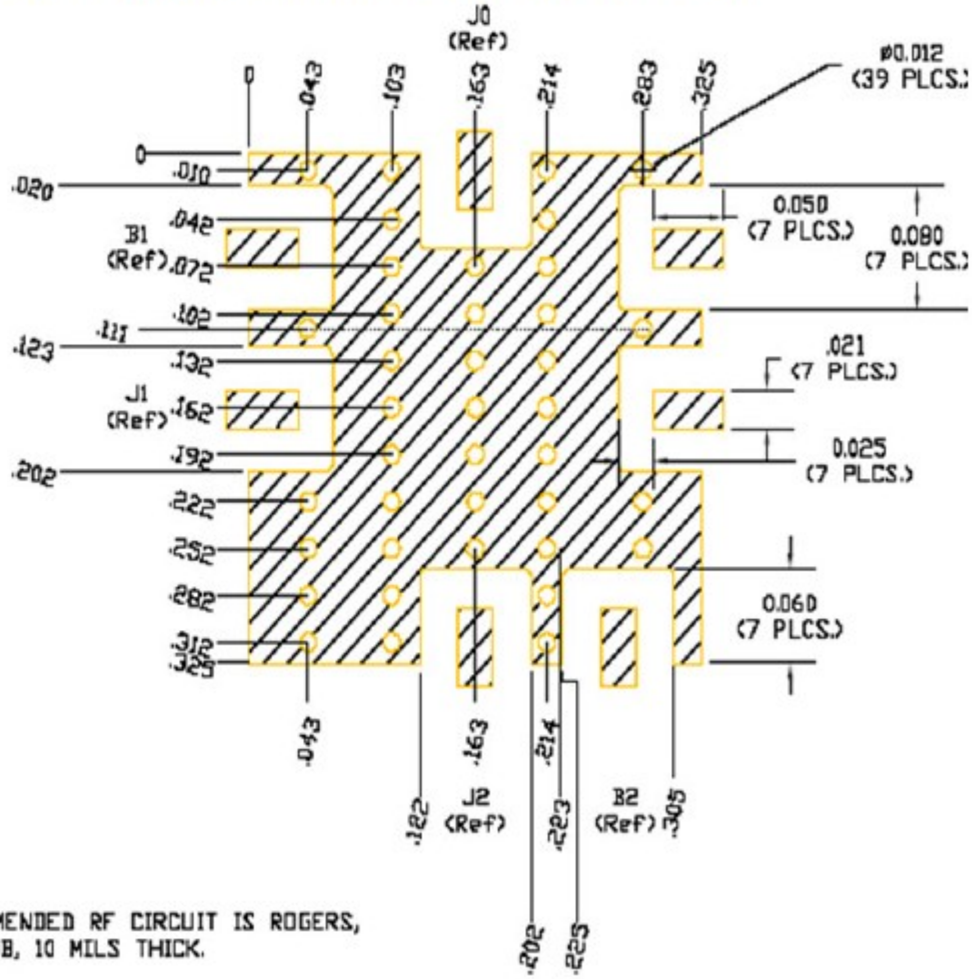
SP3T Switch Outline for Case Style 310 (CS310)



Notes:

1. Hatched Metal Area on Circuit Side of Device is RF, D.C., and Thermal Ground.

RF Circuit Solder Footprint for Case Style 310 (CS310)



NOTES:
1. RECOMMENDED RF CIRCUIT IS ROGERS, RO4350B, 10 MILS THICK.

Hatched area is RF, DC, and thermal Ground. Vias should be solid copper fill and gold plated for optimum heat transfer from backside of switch module through Circuit Vias to metal thermal ground.

Part Number Ordering Information

Part Number	Description	Packaging
MSW3103-310-T		Tube
MSW3103-310-R		Tape-Reel (Quantities of 250 or 500)
MSW3103-310-W		Waffle Pack
MSW3104-310-T		Tube
MSW3104-310-R		Tape-Reel (Quantities of 250 or 500)
MSW3104-310-W		Waffle Pack
MSW3103-310-E		RF Evaluation Board
MSW3104-310-E		RF Evaluation Board

* RF Evaluation boards are rated at + 45 dBm C.W. or Peak Incident Power due to the RF power rating values of the Passive L, C Bias Elements.