MICRO
Advanced Process Control, Defect Reduction, and Yield Enhancement for Semiconductor Manufacturing

MATERIALS INTEGRATION

Using an ICP-based strip system to perform resist and barrier-layer removal in copper low-k processes

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A resist strip and barrier-layer-removal system that can control the ion current and ion energy of the plasma species minimizes sputtering and the contact resistance of copper surfaces.

The successful integration of copper interconnects and low-k dielectrics in dual-damascene processes has been a critical, but difficult, step in the development of IC technology. The new materials used in interconnect layers are essential for achieving the higher-speed operations that are required for advanced computing and communications applications. Because copper is a better conductor than aluminum and the interline capacitance of low-k materials is lower than that of silicon dioxide, copper/low-k technology reduces resistance-capacitance (RC) delay for signals and accelerates the switching of logic gates in the circuit.[1–3]

One part of the copper/low-k integration process, stripping photoresist and cleaning wafers without damaging the low-k materials, has been a significant challenge.[4,5] Advanced semiconductor fabs have met this challenge in production, and work is proceeding on the development of next-generation ultra-low-k dielectrics—particularly nanoporous materials—to further reduce the dielectric constant.

In the integration process, three main problems result from photoresist stripping and the removal of residues and the barrier layer covering the copper:

- *Low-k film damage.* The low-k film can be damaged through oxidation

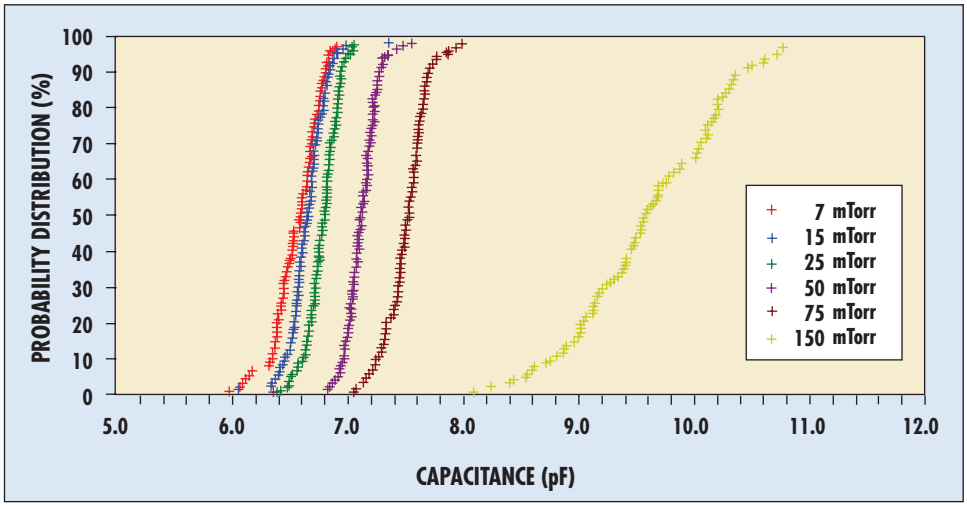

Figure 1: The 0.25/0.30-µm comb capacitance test results from MSQ films showing dependence of RC product on process pressure.

or other types of chemical attacks. Such attacks can potentially cause material shrinkage, increasing the dielectric constant or roughening the via sidewalls. Those effects make the subsequent formation of an impermeable metal barrier difficult.[4]

- *Increased copper contact resistance.* The surface properties of copper can be altered as a result of contamination, oxidation, or improper residue removal.[5]
- *Backsputter of copper onto via sidewalls.* Process schemes with less-than-adequate control of the plasma potential or high bias voltage can cause copper to sputter from the bottoms of the vias onto the sidewalls of the dielectric, which can contaminate transistors.[6]

Methods for Integrating Copper/Low-k Steps

Various methods have been developed for integrating the many steps involved in patterning low-k dielectric while preserving low-k properties and avoiding or reducing copper interconnect contamination. Regardless of the approach, the cost of each layer must be kept as low as possible because of the increasing number of interconnect layers. Two copper/low-k integration routines are commonly performed:

- *All-in-one process.* Some etch systems perform what is referred to as an all-in-one process, where all steps take place in one tool. Steps include low-k etching of vias and trenches, photoresist stripping, and barrier-layer removal. The all-in-one approach is usually conducted in a single etch chamber, which reduces the throughput of a tool that is expensive to operate.
- *Dual-tool process.* In this approach, etch and barrier-layer-removal steps are performed in the etch tool, and photoresist strips are performed in a separate ashing system. However, if the strip step is conducted before the removal of the barrier layer, the wafers must be returned to the etcher after ashing, increasing cycle times. If barrier-layer removal is performed in the etch tool before the strip step is performed in the ashing tool, copper is exposed during the strip step. The use of either oxidizing or reducing strip chemistries leaves a chemically altered layer on the copper surface, increasing contact resistance. Although the use of hydrogen-based chemistries can reduce copper oxidation, they often leave a copper hydride layer that is hard to eliminate.[7]

This article demonstrates the use of an electrostatic-shielded inductively coupled plasma (ICP) and radio-frequency (RF)-biased stripping system that was installed at Freescale Semiconductor's Austin, TX, facility to strip photoresist and remove the barrier layer covering the copper lines. In this two-in-one scheme, dielectric etch is performed in an etch tool, after which resist strip and residue removal steps followed by barrier-layer removal are performed in an Aspen III Highlands ICP-based strip tool from Mattson (Fremont, CA). The two-in-one approach was compared with the process of record (POR), in which low-k etch and barrier-layer-removal steps were performed in the etch tool.

The Highlands reactor design can control the ion current and ion energy of the plasma species independently. To demonstrate that capacity, the article presents Langmuir-probe and ion energy analyzer measurements. Furthermore, the article shows that lower gas pressures, lower pedestal temperatures, and better control over ion properties contribute to improved electrical test results. On-wafer results, including CD loss and via-chain resistance, are presented to demonstrate the benefits of the process. Finally, parametric yield results confirm the capabilities of the two-in-one system.

Resist Strip, Residue Removal, and Barrier-Layer Removal

To effectively integrate the two-in-one process, a stripping system must meet stringent requirements for avoiding contamination and low-k damage. The process removes resist and residues before removing the barrier layer beneath each low-k layer. Thus, the copper surface is protected while resist and residues are removed, avoiding copper oxidation during oxygen-based plasma stripping.

Following resist stripping and cleaning, the barrier layer can be removed with a soft ion-based process, opening the path to the copper underneath for all vias. This process requires ion bombardment to provide the anisotropy required to complete proper formation of the vias down to the copper underlayer.[8] However, control of ion energy and the proper

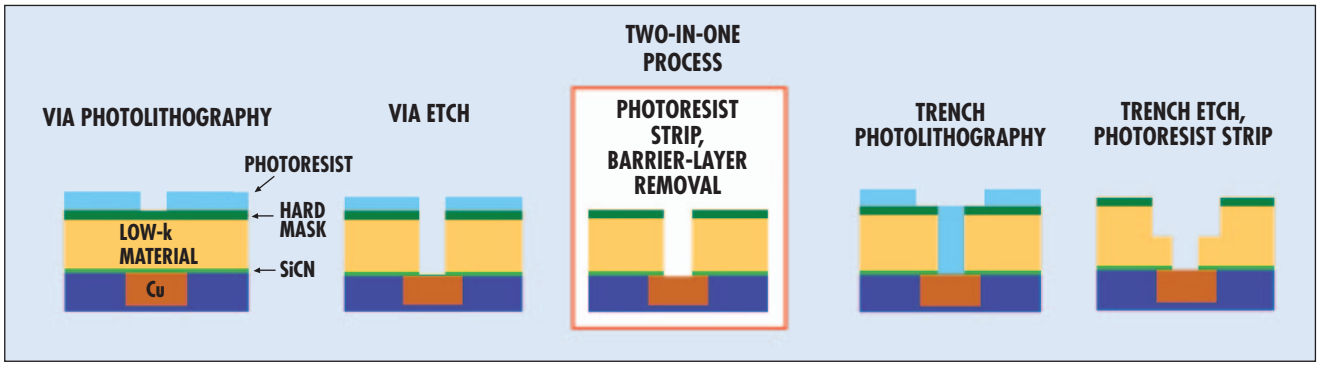

Figure 2: Schematic diagram showing system integration scheme of the two-in-one process.

process chemistry are vital for minimizing copper sputtering and polymer deposition onto the copper.

Resist Stripping. The dry resist strip step generally removes organic polymers by converting them into volatile products. Because of low temperature and low process pressure, the oxygen-based, ion-activated two-in-one process efficiently strips resist without removing or reacting significantly with the organic components of the low-k material. For low-k dielectric materials used at device geometries ≥90 nm, this method works. It works because it exposes sidewalls to a higher ratio of ion flux than oxygen radicals. Low oxygen flow and low gas pressure result in low atomic oxygen flux, while low temperature also contributes to reducing oxygen diffusion into the low-k material through the via sidewalls. At the same time, ion impact effectively seals the sidewalls, which also inhibits oxygen diffusion into the low-k material.

Another benefit of the two-in-one system is that it strips resist and removes residue while the barrier layer covers the copper. This feature prevents oxidation of the copper surface and sputtering of copper onto the via's low-k material sidewalls by the ions that activate the stripping process.

Figure 1 shows comb capacitance measurements from a methylsilsesquioxane (MSQ)-based dielectric material processed at different pressures in the two-in-one strip system (all other parameters remained constant). The figure demonstrates the preservation of low interline capacitance and shows that gas pressures at or above 25 mTorr adversely affect capacitance. Since the two-in-one process uses low pressures and temperatures, stripping rates for this ion-based oxygen process are somewhat lower than those in conventional high-temperature downstream systems. However, they are adequate for the thinner photoresist layers used in 90-nm production. Furthermore, because ion bombardment provides the activation for reactions, wafer temperatures above 100°C are not needed to achieve productive stripping.

Residue Removal. Residue removal, which usually occurs at the same time as resist ashing, requires sufficient reactive species to volatize or convert the polymer on the sidewalls and bottoms of the vias to a soluble form. These polymers typically contain carbon and fluorine, as well as some silicon, oxygen, and hydrogen.[9] It has been observed that the primarily carbon-based polymers at the bottoms of the vias can be eliminated effectively by the use of oxygen in the stripping process.

Barrier-Layer Removal. The barrier layer at the bottoms of the vias is best removed after stripping. Barrier-layer removal should be performed over the entire via area without undercutting or damaging the low-k dielectric. While optimal removal in vertical via profiles virtually requires ion bombardment, that process can cause wafer problems if it is not properly controlled. Ion energies above 20 eV cause copper to sputter onto via walls, resulting in contamination and loss of reliability.

Capacitively coupled parallel-plate etchers cannot maintain low ion energy because in such systems, electrode potentials must be hundreds of volts. In contrast, very low and controllable ion energies, which result in less contamination from copper sputtering, can be achieved using an inductively coupled, electrostatically shielded plasma source operating under low pressure. The electrostatic shielding isolates plasma from induction coil voltage, which can greatly reduce the plasma potential, thereby reducing the energy of the ions arriving at the wafer.

Cleaning Carbon-Containing Residues on the Copper Surface. Following the barrier-layer-removal endpoint, the final step in the two-in-one process is the removal of residues and the reduction of oxidation on the copper surface. In this step, it is difficult to clean carbon-containing residues on the copper surface adequately without causing via sidewall damage to the low-k dielectric or forming a copper hydride layer on the copper surface. To remove carbon-containing residues, ion bombardment in a reducing chemistry is used, which is effective at activating reactions with the residues on the copper surface while avoiding excessive surface exposure to hydrogen. Furthermore, unless ion energies are well controlled, copper sputtering from via bottoms can occur.

System Integration and Plasma Source

Integration Scheme. Before the introduction of the two-in-one process, via etching and the opening of the barrier layer were performed in a capacitively coupled dielectric etcher. Following the etch process, photoresist was stripped in a separate ICP-based tool. Figure 2 displays the two-in-one process integration scheme used at Freescale to perform the

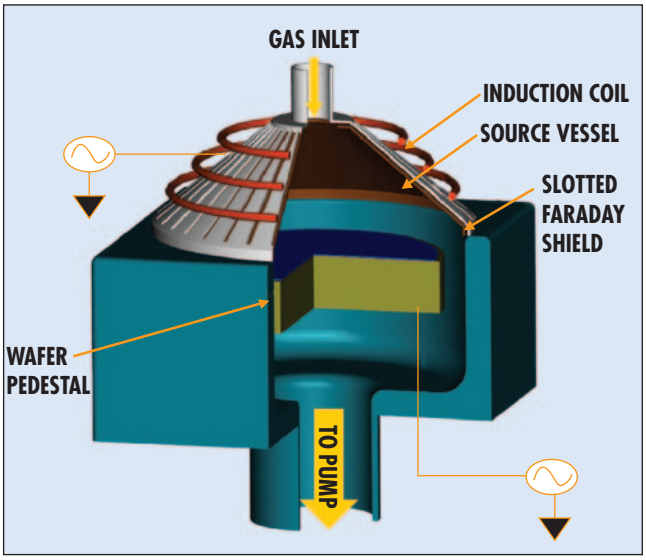

Figure 3: Plasma source and stripping station of the two-in-one system.

experiments discussed in this article. As illustrated in the figure, the vias were first patterned using a 193-nm resist. During the etch step, the vias were etched and the barrier layer was partially opened in the etcher. After the etch step, the two-in-one process was conducted, during which photoresist was stripped and the remainder of the barrier layer was opened. Then 248-nm resist was used to pattern the trenches. Finally, trench etch and photoresist strip were performed in a capacitively coupled dielectric etcher.

Plasma Source. A cross-sectional view of the two-in-one processing reactor used in the experiments at Freescale is shown in Figure 3. The vacuum chamber has two stations (not shown) in which two wafers can be processed simultaneously. Each station has an electrostatically shielded ICP source and a wafer pedestal. The ICP source and the wafer pedestal are powered independently at the same radio frequency.

A slotted electrostatic Faraday shield is situated between the induction coil and the vacuum vessel. This aluminum shield closely covers the dielectric vacuum vessel, electrostatically isolating the plasma from the induction coil. The slots are very narrow, permitting only negligible penetration of the electrostatic field. The shield is attached directly to the aluminum top wall of the processing chamber so that it is very well grounded and thereby shorts out any RF electrostatic fields that might otherwise couple from the coil to the plasma. The coil can carry thousands of volts, which, at radio frequencies and without the Faraday shield, could capacitively couple amperes of current to the plasma, significantly increasing the plasma potential.

Inductive plasma sources are well known for their ability to operate in the lowest pressure regimes, enabling increased ion flux relative to neutral radical flux. However, such sources may experience problems arising from varying wall conditions in the source, which may influence processes adversely and cause contamination. Coupling in nonshielded sources increases the sheath potential adjacent to the coil, causing ion bombardment at that part of the wall to have high energies. The resulting sputtering and etching leads to nonuniform wall conditions and vessel erosion. Furthermore, unshielded RF power from the coil influences the plasma potential and, therefore, the energy of ions bombarding the wafer. In an unshielded source, increasing RF power to the coil increases the ion current density to the wafer, but it also increases the plasma potential and the sheath potential above the wafer. As a result, the minimum controllable ion energy at the wafer is considerably higher than when an electrostatic shield is used.

In a plasma source containing an electrostatic shield, the shield, rather than the plasma, provides the grounding path for capacitively coupled currents from the coil. The shield prevents the coil voltage from affecting the local wall sheath potential, preventing sputtering of the wall and vessel-wall erosion. It also stops the coil voltage from affecting the plasma potential because it prevents RF currents from the coil from passing through the plasma. The shield thus enables independent control of ion current density and ion energy because varying the source power does not increase the plasma potential and the sheath potential above the wafer. This results in enhanced control over the physical mechanisms of the process. Consequently, the electrostatic shield is an important feature that permits an inductively coupled source to succeed in wafer fabrication.

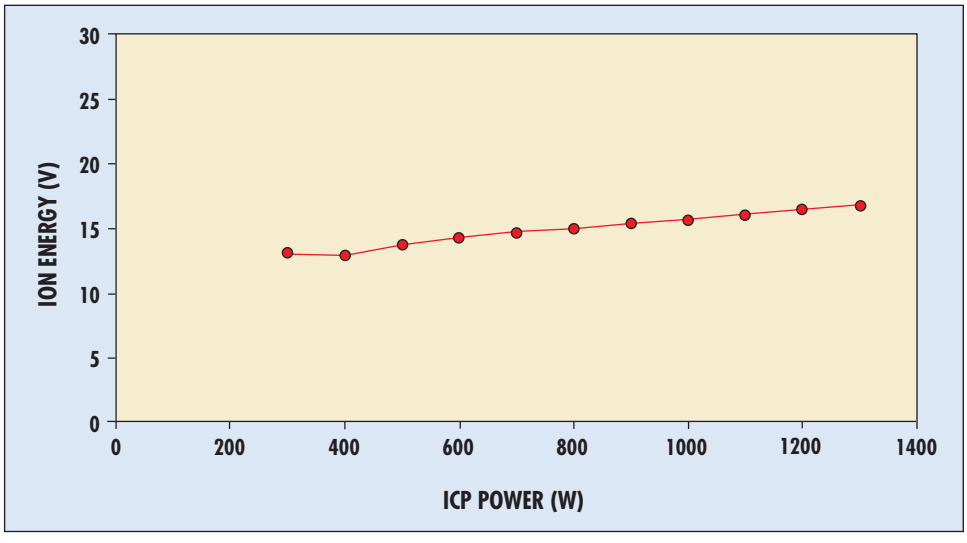

Figure 4: Dependence of plasma potential on ICP power.

Figure 4 shows the plasma potential for a range of RF power levels provided to the

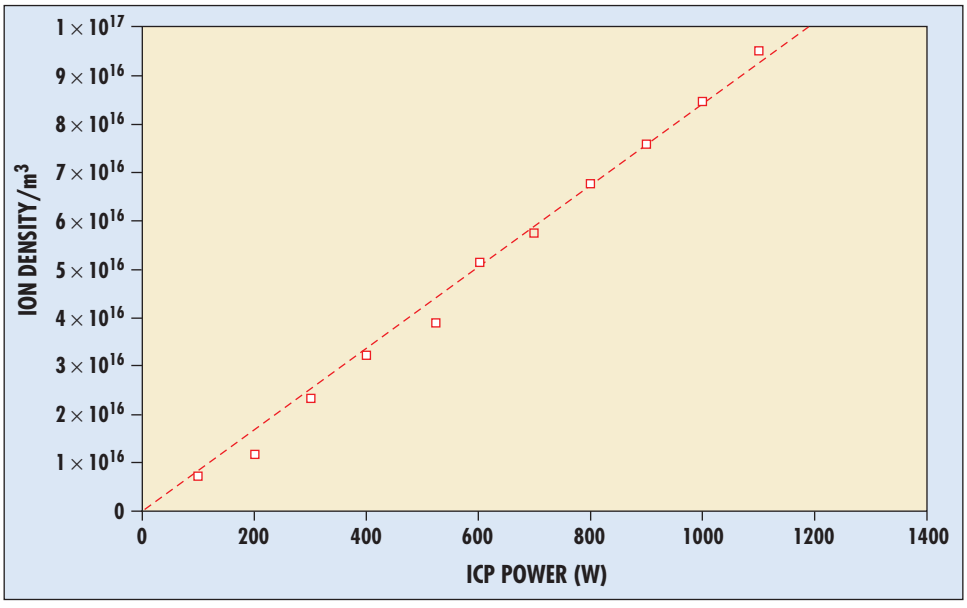

Figure 5: Linearity between ion density and inductively coupled power.

plasma induction coil. In this test, an EQP field energy analyzer from Hiden Analytical (Warrington, UK) was used to make the plasma potential measurements. It is evident that increasing RF power to the coil, which increases both the ion current density and the voltage on the coil, raises the plasma potential only slightly. This small increase may result from the slightly increased electron temperature.

Ion density is strongly dependent on the induction power provided to the coil. Figure 5, based on ion-density measurements made using an ESP Langmuir probe from Hiden, shows this relationship to be linear. The fact that electron temperature increases only very slightly with ICP power suggests that ion current density also increases roughly linearly with ICP power. This phenomenon is important because it enables the two-in-one system to provide more ion current to the wafer to increase process rates without increasing the plasma potential. Furthermore, since bias power is roughly the product of the ion current and ion energy, the ability to increase the ion current at a fixed bias power results in reduced ion energies. Other systems, in which increased ion current results in increased ion energy, cannot do this. Limiting ion energies is an important capability, since it eliminates sputtering of copper interconnects when barrier-layer removal is completed.

While ion density in this electrostatically shielded plasma source is dependent on inductively coupled power, data indicate that ion density and ion current density show almost no dependence on bias power. Figure 6 illustrates the measured dependence of ion density on bias power. Because increased bias power does not increase ion density, the power is used almost entirely to increase the bombardment energy of the ions, as intended. In such a high-density inductive plasma with a moderate RF potential used for biasing, the normal (nonlinear sheath dynamic) mechanism for electron heating resulting from capacitively coupled bias power has a minimal heating effect on the plasma electron population. Thus, bias power has only a minimal effect on ion density.

The copper sputtering rate at low ion energies is strongly dependent on energy. Measurements indicate that the sputter yield of argon ions bombarding copper below an energy level of approximately 20 eV is virtually 0. Consequently, the threshold energy is 20 eV. However, as ion energies rise to about 50 eV, the yield increases to more than 0.01 atoms of copper per incident ion. According to the Transport of Ions in Matter (TRIM) code, which is widely used to model ion impact and the penetration of solids, the sputter yields for atomic oxygen or fluorine ions are roughly equal to those of argon ions striking copper. Hence, since substantial overetch is likely during the barrier-layer-removal process, ion energies >50 eV would produce a sputtered yield of approximately an atomic monolayer or more of copper, a significant amount that would likely result in poisoning and reliability problems.

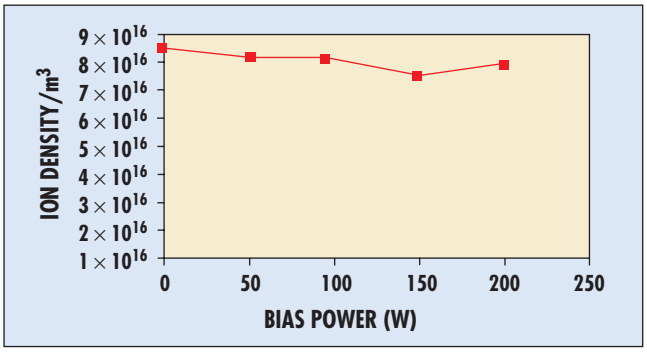

Figure 6: Measured ion density versus bias power in the two-in-one system.

System Performance and Results

Following stripping and residue removal, which are performed simultaneously using the oxygen-based process chemistry, the barrier layer is anisotropically removed. Since the amount of the barrier layer remaining after dielectric etch can vary significantly because of within-wafer variation in the dielectric etch, it is inevitable that substantial overetch will occur in those vias where the barrier layer is initially much thinner. In these areas, the copper at the bottoms of the vias is exposed to the barrier-layer-removal process. Therefore, barrier-layer-removal uniformity is less important than the requirement that the process not sputter the copper. Barrier-layer-removal uniformity has been measured in this system to be <2% 1σ, which, given the small thickness of the layer, is well within acceptable limits.

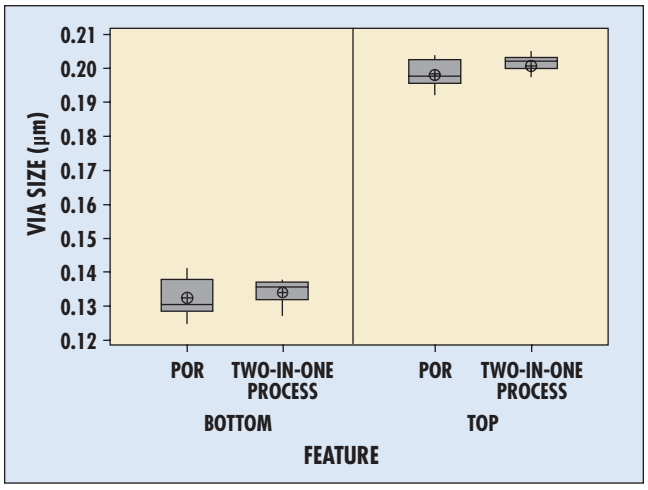

Figure 7: Electrical test results for via bottom and top CD.

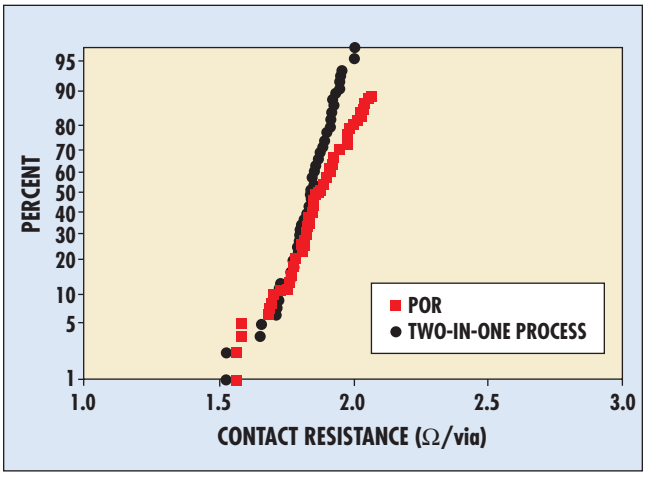

Figure 8: Normalized probability chart showing via-chain resistance.

A risk associated with using the two-in-one method to remove the barrier layer is the rounding of the edges of the vias or trenches. Rounding increases the critical dimension (CD) of the vias and is undesirable. It occurs because ion-based processes tend to have high sputtering rates for sloping surfaces, such as the edges of vias or trenches, which increases etch rates. Figure 7 compares POR and two-in-one measurements for the bottom and top CDs of dense and isolated vias after barrier-layer removal. For the two-in-one process, a barely measurable increase in CD near the via tops was observed. This widening, which was on the order of only a few nanometers, was well within acceptable limits because of ion-energy control (which is also helpful in avoiding copper sputtering) and the consequent reduction in sputtering or enhanced etching of exposed edges. This CD control helps to avoid metal-to-metal leakage, which can occur if the tops of the vias are widened. In addition, Figure 7 shows that the two-in-one process achieved equivalent or better via bottom CDs than the POR and caused less within-wafer variation.

The barrier-layer-removal process must leave the copper surface free of oxidation or residue, thus minimizing the resistance of the plug to the underlying line. Characterizing resistance across the wafer for a given process is done using a test structure with many vias in series with copper lines, so that the contact resistances add together. Variations in the distribution of via resistances to underlying lines in a given structure are expressed in the value of the average resistance per contact. Figure 8 presents cumulative plots of the via chains' average resistances for both the POR and the two-in-one process. The latter produced lower via-chain resistance, resulting in better via-chain yield than the POR. The greater consistency of low contact resistance resulting from the two-in-one process is apparent—clear evidence that there are far fewer high-resistance contacts in that process than in the POR. This phenomenon results in devices that are faster, on average, than those fabricated using the POR, improving the value of functional devices.

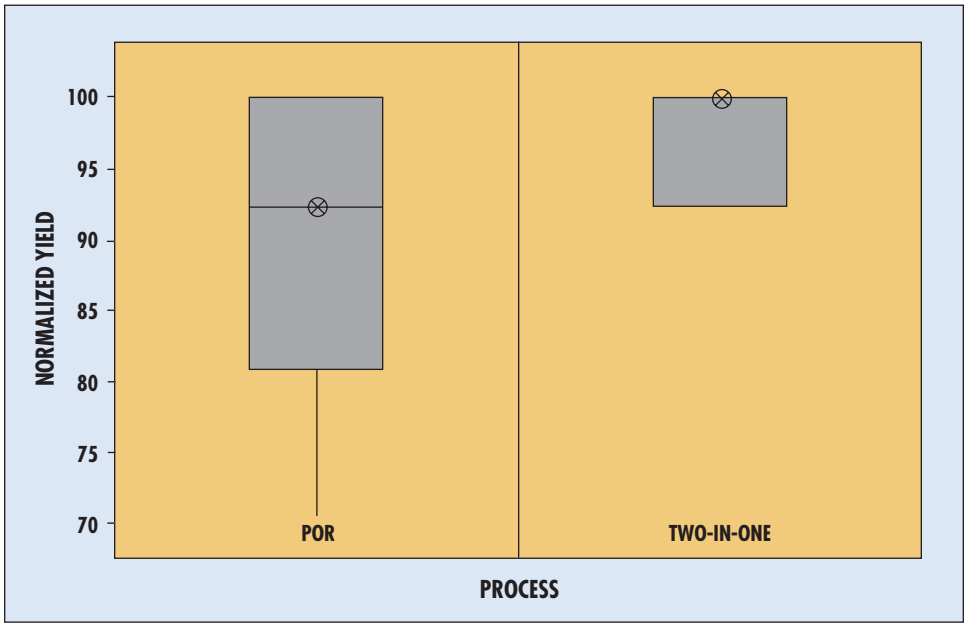

Figure 9: Normalized probability chart showing via-chain yield.

The potential impact of contact resistance distribution on actual device yield is illustrated in Figure 9. The two-in-one process resulted in a substantial 8% improvement in via-chain yield over the POR. The narrower width of the distribution of via-chain resistance for the two-in-one method also reduced within-wafer or lot-to-lot yield uncertainty.

Figure 10 presents a cross-section scanning electron microscope (SEM) image of a copper/low-k interconnect structure manufactured using the two-in-one process. The figure shows that the process maintained the profile of

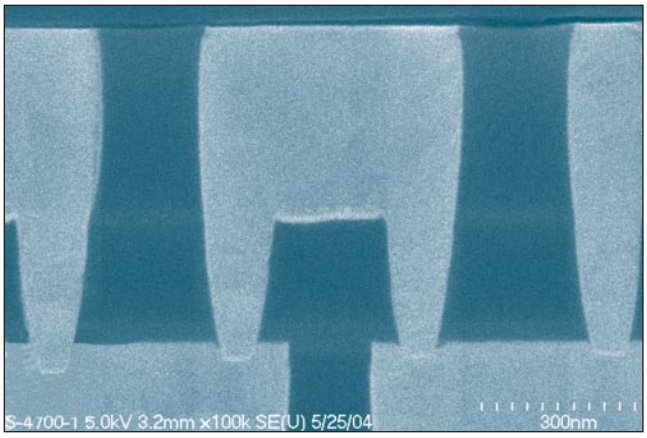

Figure 10: Cross-section SEM image of a copper/low-k interconnect structure manufactured using the two-in-one process.

vias and trenches and that the barrier was successfully removed.

Conclusion

To meet the strict requirements of two-in-one processing, a strip/residue removal tool should have the following properties:

- The ability to process wafers at low temperatures to control the reactivity of gas-phase species with the dielectric through via sidewalls.
- Great flexibility in its use of process chemistries and the ability to shift process steps continuously across substantial pressure and chemistry ranges.
- Well-controlled ion energy that is stable and highly controllable at low values so that copper sputtering can be lessened.
- The ability to vary ion energy or ion current density without affecting the other significantly.
- Ion-current density that is repeatable and uniform over a range of pressures and gas chemistries.
- Stable reactor-wall conditions that do not vary widely or rapidly over the interior surface of the reactor.

It has been shown that an alternative integration scheme for dual-damascene low-k copper integration, in which stripping and barrier-layer removal are performed in a separate low-pressure ion-based tool, is successful. Data have demonstrated that the two-in-one tool provides a high ion current and can independently control the ion energy and ion current that the wafer is exposed to. These process control capabilities are critical for the success of back-end-of line dual-damascene integration.

Data have also demonstrated that the two-in-one system preserves the dielectric constant of the low-k material and achieves lower via resistance than the POR. In addition, performing barrier-layer removal using the system causes negligible widening of the via tops and minimal increase in CD. Finally, the system results in better via-chain resistances and yields than the POR.

Acknowledgments

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