Resist strip and Cu diffusion barrier etch in Cu BEOL integration schemes in a Mattson Highlands™ chamber

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Introduction:

The work described below deals with the process development for stripping the resist and etching the SiC barrier layer from oxide and low-k damascene structures. In the damascene patterning, SiC is used as a barrier layer that prevents Cu to diffuse into the dielectric stacks. The requirements for this barrier etch and strip process are numerous: no chemical modification (k-value), good post etch Cu cleaning properties, good selectivity towards hard masks and good profile control. All experiments were performed in a Mattson Aspen III – Highlands chamber; a low-pressure reactor with biased bottom electrode.

Experimental:

Three potential candidates for plasma etch of SiC: H_2/CF_4 – N_2/CF_4 – O_2/CF_4 and two candidates for resist strip N_2/O_2 and N_2/H_2 were selected. A DOE to screen the optimal process parameters was set up on blanket CVD SiC, CVD oxide and resist wafers. Afterwards the etch and strip plasmas were characterized on single damascene wafers to check the performance for resist strip efficiency, profile control, hard mask erosion and post etch residue removal. In a third phase interline capacitance measurements were done to investigate possible modification of the dielectrics low-k value. Finally XPS analyses were performed to get an idea about the chemical composition of the low-k sidewalls, the Cu surface and the top hard mask after barrier etch.

Results and discussion:

As can be seen from fig.1 the CF_4/O_2 plasma shows the highest SiC etch rate as compared to the CF_4/H_2 and CF_4/N_2 plasma. Looking at fig. 2, the SiC:SiO_2 selectivity is the highest for the CF_4/O_2 plasma with a maximum of 2:1. However, since O_2 free plasma might be preferable for low- k compatibility, also the other chemistries are of interest. For the CF_4/H_2 and CF_4/N_2 plasma, typical SiC:SiO_2 selectivity of 1:1 and 1.5:1 are measured. High strip rates, > 600 nm/min, are obtained in conventional N_2/O_2 plasmas. The strip rates of a N_2/H_2 plasma are shown in fig 3. The maximum strip rate is only 200 nm/min for this plasma but could be used as a valuable alternative for an oxygen free resist strip.

These findings were a good starting point for doing further process development on patterned wafers. Some applications only require the etching of the SiC Cu-diffusion barrier, i.e. when all the resist is consumed during the previous patterning step(s). An example is shown in Fig 4. It shows a cross section SEM picture from a dual damascene stack (without Cu underneath) after the SiC etch using a high CF_4/H_2 plasma followed by a solvent clean to remove (Cu) residues.
For applications that require both resist strip and SiC etch, there are two possible alternatives: a resist strip first or a SiC etch first approach. Fig. 5 and 6 show a comparison between "SiC etch first followed by resist strip" and "resist strip first followed by SiC etch" from a single damascene trench in LKD-5109™. These wafers did not receive an additional wet clean. As can be seen from the pictures, the profile control and the residue removal are worse when the resist strip is done before the SiC etch.

In a third phase, interline capacitance measurements (ILC's) were performed on SD test structures. The goal of these tests was to study the impact of different etch chemistries on the effective k- value. The results of an ILC experiment on SD SiLK™ are shown in fig. 7. It compares the as measured ILC values of a reference wafer which did not get a SiC removal nor a wet solvent clean and other wafers which got different SiC etch plasma's. As a general conclusion it can be stated that the measured ILC data for the H_2/CF_4 SiC etch plasma are somewhat lower than for the other splits. These differences could be explained by the larger contribution of the low k layer in the dielectric stack because of the HM erosion. The CF_4/O_2 plasma shows the highest ILC values, which points towards low-k degradation.

Finally, XPS analyses were made on SD SiLK™ trenches at three different X- ray angles. A comparison was made between a reference wafer, which did not get a barrier etch and 2 wafers, which got a 50 % and 100 % barrier overetch. Some general conclusions could be drawn from fig. 8: if the barrier etch is done with a CF4/H2 plasma, C-F_x, CuO, $Cu(OH)_2$ residues can be found in the trench and against the side walls. No Cu could be found on top of the trench and even with longer overetch the relative Cu percentage that could be found, was not significant.

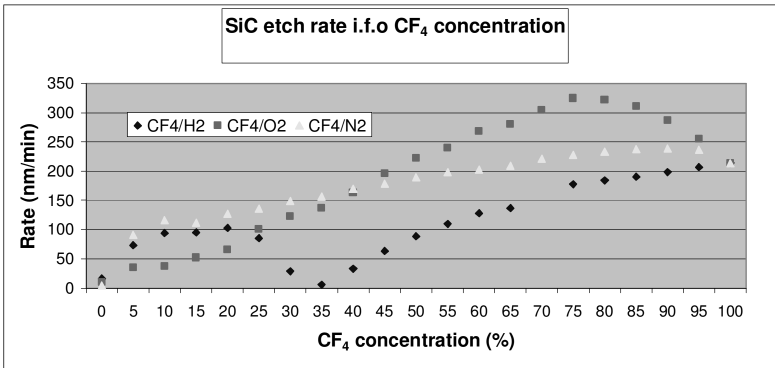

Fig. 1: SiC etchrate i.f.o. CF_4 concentration

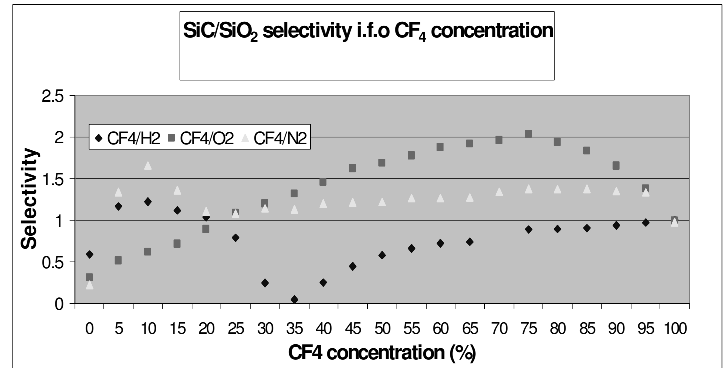

Fig. 2: SiC/SiO_2 selectivity i.f.o. CF_4 concentration

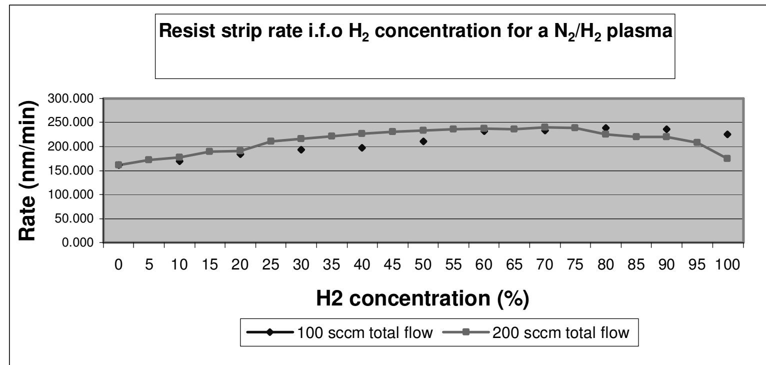

Fig. 3: Resist strip rate i.f.o. H_2 concentration for a N_2/H_2 plasma

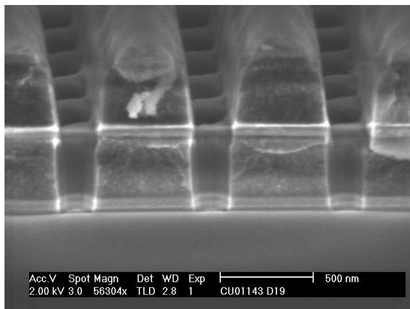

Fig. 4: dual damascene (no Cu)

Fig 5: single damascene on Cu

Fig 6: single damascene on Cu

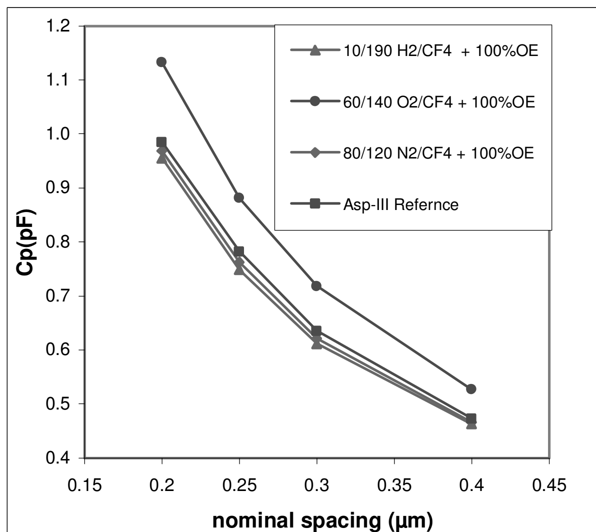

Fig. 7: Interline capacitance

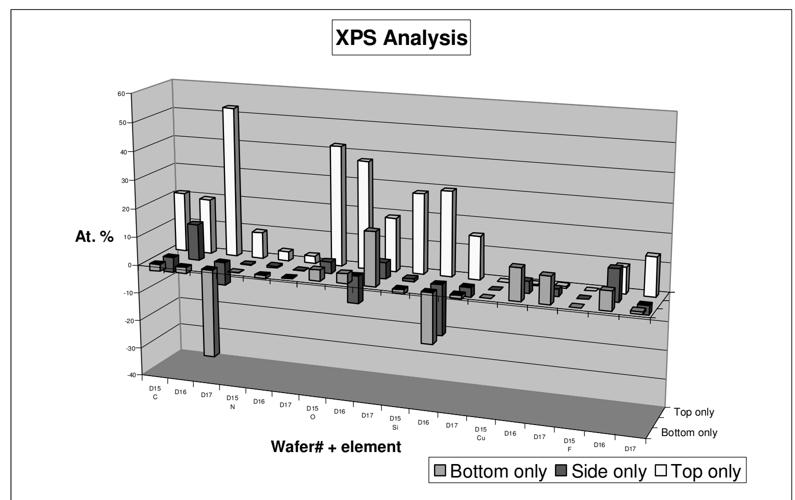

Fig. 8: XPS analyses