RTP APPLICATIONS AND TECHNOLOGY OPTIONS FOR THE SUB-45 NM NODES

R. B. MacKnight[1], P. J. Timans[1], S.-P. Tay[1], and Z. Nenyei[2]

[1]Mattson Technology
47131 Bayside Parkway
Fremont, CA 94538
U. S. A.

[2]Mattson Thermal Products GmbH
D-89160 Dornstadt
Germany

As device dimensions have reduced to nanometer length scales, rapid thermal processing (RTP) has emerged as the key approach for providing the low thermal budget and ultra-pure process conditions that are essential in advanced fabrication schemes. As further progress in electronic technology becomes increasingly dependent on success in rapid development cycles that include both materials innovations and changes in CMOS device architecture, RTP will play a major role in the story. RTP will contribute in gate-stack engineering, oxidation processes, ultra-shallow junctions, silicide formation, low-k dielectric annealing and in fundamental improvement of thin film properties.

As device dimensions are controlled at the atomic scale, the concepts of thermal budget reduction will continue to drive the technology, with reductions in both process times and process temperatures combined with control of a very high purity process gas ambient. The thermal and ambient flexibility of RTP will become even more important as processes are developed and optimized for new gate dielectrics, high-mobility channel designs and metal gates combined with device architecture changes such as multiple-gate transistor designs.

As the transistor channel length scales towards the ultimate limit imposed by atomic-scale fluctuations and quantum effects, the need for minimization of parasitic resistance and capacitance will become increasingly dominant in device performance. Here, the most critical requirements are to increase the concentrations of electrically active dopants without inducing excessive diffusion and to reduce contact resistances. These challenges will be met through innovation in RTP that addresses opportunities in materials engineering and in thermal cycle design.

Further advances in silicon device technology will ultimately be limited by manufacturing costs. Pressure for manufacturing cycle-time reductions will mean that single-wafer processing technologies, including RTP, will continue to displace batch processing approaches. The final blow for the batch furnace will come from the transition to even larger wafer sizes, where the planar heating geometry inherent in RTP provides a natural fit to the wafer.

INTRODUCTION

The reduction in the feature size of MOS devices continues to be the dominant trend that propels the semiconductor industry. Despite extraordinary technical challenges, this trend has continued to provide consistent benefits both in circuit performance and cost. Although the technical and financial obstacles to further progress continue to be the subject of debate, there are no fundamental physical barriers to the creation of MOS devices with 5 nm gate lengths [1]. Fig. 1 shows predictions from the International Technology Roadmap for Semiconductors (ITRS) that show key device feature sizes rapidly reducing towards the limits set by interatomic spacings [2]. However, the issues for scaling are becoming increasingly technically difficult, and although a plethora of potential solutions has emerged, the pace of progress in CMOS device scaling is likely to slow significantly over the next decade [3,4]. The continuing escalation of the investment needed for volume production of leading-edge CMOS devices also poses a formidable economic challenge that may moderate the pace of technical progress.

A survey of the recent history of device scaling shows that CMOS technology is rapidly ceasing to be a "power-friendly" electronic technology [4,5]. Fig. 2 illustrates the nature of the problem. The off-state current in CMOS devices has been rising extremely fast, as device designers have used scaling approaches that improved performance at the expense of power consumption. This trend is inherently incompatible with the low-power mobile electronics applications that have become increasingly important to the electronics industry. Further progress in scaling at the 45 nm device node and beyond will have to answer this challenge. Traditional scaling approaches will need to be augmented by major innovations in materials and device architecture in order to keep the benefits of scaling alive [4-8].

RTP: A KEY TECHNOLOGY IN SCALING BEYOND THE 45 nm NODE

The most important challenge in scaling of advanced devices arises from how to suppress the off-state current of the transistor while maximizing the on-state current. Advances in the engineering of ultra-thin gate insulators, high-mobility channels, ultra-shallow junctions and low-resistance contacts are the keys for this progress. RTP provides essential capabilities for both process and materials development on this path. Table I indicates the range of applications in silicon device technology where RTP will be critical for progress in device scaling. Figs. 3, 4 and 5 illustrate how RTP processing provides key capabilities in doping, gate stacks, contacts and interconnects. Fig. 6 shows examples of how RTP will be essential in future multi-gate device technologies. In these advanced devices, RTP will find new applications in conditioning the surfaces, interfaces and topography of 3-D structures, while continuing to be crucial in activation of dopants and in contact formation.

Fig. 7 shows the trends in the "temperature-time" domain where RTP finds its most important applications. The recent trends have included "hotter and faster" processing that is needed for advanced ion-implant activation processes for the formation of ultra-shallow junctions (USJ), and the increasing use of RTP at relatively low process temperatures ($< \sim 500°C$). Although the focus in this paper is on the use of RTP for silicon device manufacturing, Table II shows that the methods and benefits of RTP will continue to extend to a wide range of high-technology applications.

In advanced CMOS devices, the problem with off-state current arises from two major components. The first is the current that flows as a result of the finite potential barrier between the source and the drain and the second is the current that flows by tunneling through the gate insulator. There are also several other leakage currents of lesser significance, such as the leakage current at the source/drain (s/d) junctions. Control of the flow of current from

source to the drain in the off state requires minimization of short-channel effects such as drain-induced barrier lowering and degradation of the sub-threshold slope. Increased doping of the channel, combined with innovations such as super-steep retrograde channel doping profiles, halo implants and ultra-shallow s/d extensions have all helped in management of the issue [5,9-11]. However, further improvement may require the use of fully-depleted silicon-on-insulator (FD-SOI) approaches or even multi-gate transistor designs [6,7]. Although there are many research reports that show that a change from the traditional planar configuration to "three-dimensional" structures with multiple gates improves CMOS scalability, the extensive changes needed in fabrication approach mean that such configurations are unlikely to be adopted before the 32 nm node [7]. As a result, there is still a strong interest in using bulk silicon at least down to the 45 nm node, and maybe beyond [9,11,12]. However, this will only be possible with further development of doping and activation technologies that allow the creation of extremely precisely defined abrupt doping profiles with high concentrations of electrically active dopants. Conventional ion-implantation annealing and RTP technologies are unlikely to meet this need beyond the 45 nm node. However, novel forms of RTP, such as millisecond annealing tools, can provide much higher concentrations of electrically active dopants while introducing minimal diffusion.

The reduction of the equivalent oxide thickness (EOT) of the gate dielectric is essential in order to increase the “on”-current, but it leads to the severe challenge of how to minimize gate leakage current [13]. Fig. 8 uses the predictions of the ITRS to illustrate the nature of the challenge [2]. Scaling has led to gate "oxides" with an EOT of only 0.9 nm for high-performance CMOS at the 65 nm node, and gate leakage currents are becoming a major concern for power consumption. The strict limits on the gate dielectric leakage currents that are acceptable in low-operating power and low-stand-by power devices have made the limitations of oxynitride films a significant problem even before the 65 nm node. For each type of device, there is an EOT limit where a transition to a higher dielectric constant (high-k) gate dielectric is mandatory [2]. However, despite a huge international effort to develop new high-k materials that could replace the silicon dioxide gate dielectric, there are still serious doubts that this technology will be available by the 45 nm node. Although encouraging results are described in the literature, formidable issues of process integration and reliability will require far more work [13,14]. In these extremely thin structures, interface properties dominate the electrical performance. RTP will need to provide new approaches for surface treatment and for film annealing that are consistent with the need for atomic level interface control [15].

The need to maximize the capacitance of the gate stack has also put great emphasis on reduction of polysilicon depletion effects [6,10,16]. This means increasing the activation of the dopants in the polysilicon or poly-SiGe electrode, or even replacing the polysilicon gate electrode with a metal. RTP processing plays a key part in activating the dopants in the gate, and in the future it will also help in the challenging task of integrating metal gates and in work-function tuning processes.

Progress in scaling has continued through innovations such as the creation of strain in the channel, which can help increase the mobility of charge carriers and provide higher drive currents [8,17]. Since it seems that high-k gate dielectrics tend to degrade channel mobility, such improvements become all the more important in future devices. Alternative approaches for improving mobility include the use of new orientations of the silicon crystal (e.g. (110) for the PMOS channel) and even the examination of alternative materials such as Ge [17].

Further improvements in channel mobility have the tendency to reduce the device resistance and increase the significance of the parasitic resistances of the source and drain regions. Fig. 9 shows the trend in the ratio of the parasitic s/d resistance (R_{SD}) to the channel resistance in CMOS devices down to the 90 nm node [8]. At the 90 nm node, the ratio is ~ 0.8,

and it is clear that with further scaling and further advances in mobility enhancement, R_{SD} will become the dominant issue in limiting the on-state current. Progress in scaling requires the adoption of new technologies that can significantly reduce these resistances. Here, the leading challenges are in the formation of highly-activated, yet very abrupt, s/d doping profiles and low resistance contacts. This re-emphasizes the importance of improvements in USJ engineering, but it is also essential to reduce the contact resistance at the silicide contact. Indeed, it has been suggested that the contact resistance issue may be even more important than the s/d doping issue because it rises with the square of the linear scaling factor [14]. Silicide formation and annealing requires RTP processes, and new materials are bringing a need for very tight control of low-temperature RTP heating cycles for silicide processing.

From this brief survey, it is evident that innovation in the materials engineering will be essential for the continuation of progress in the semiconductor industry. However, innovative approaches are of little value if they cannot transition to volume manufacturing with high yield and acceptable cost-of-ownership. Process control, including repeatability and uniformity control, is of paramount importance for success. This challenge is just as fundamental as those posed by the device physics or the process technology. RTP will play a critical part in the progress of materials and process development, but it must also meet the challenges of providing robust manufacturing solutions.

THERMAL PROCESSES OF THE FUTURE: A DELICATE BALANCE OF REQUIREMENTS

RTP has become the leading approach for thermal processing in the fabrication of advanced semiconductor devices. The advantages of reduced thermal budget, an ultra-clean processing environment and an inherently short cycle time for both development and manufacturing have all played a part in the move from batch processing to RTP [18]. The capability for creation of sophisticated cycles of heating and cooling with a wide range of ramp-rates, process temperatures and gas ambient conditions provides an extraordinary degree of flexibility for optimization of thermal processes.

In many ways, the device manufacturing process can be considered as a delicate balance between achieving desired process objectives while limiting undesired effects. The undesired processes can be considered in three main categories: Firstly, thermal diffusion extends device dimensions and reduces the abruptness of doping profiles and interfaces. Secondly, defect structures can form and degrade device characteristics. Thirdly, contamination leads to the incorporation of impurities, interface layers and particles. The essence of RTP is to limit diffusion and defect formation through minimization of thermal budget, while simultaneously providing a highly controlled ambient that minimizes contamination effects.

The most fundamental trend in thermal processing requirements is the need for continuous reduction in thermal budget. The concept of thermal budget very much depends on the physical state of the device at any given point in the fabrication process, as well as the kinetics of an undesired process that is activated by the thermal exposure [19-21]. The upper limit on thermal budget is usually set by the extent to which a given thermal cycle induces diffusion, chemical reaction, defect formation or phase-change phenomena that are not desired.

As an example, it is instructive to consider the degree of diffusion induced by various heat treatments in comparison to the size of device features. Fig. 10 shows the temperature and times associated with various diffusion lengths of B atoms. The curves were calculated using $[4D(T)t]^{1/2}$, where D(T) is the intrinsic diffusion coefficient for B at the process temperature T and t is the process time [22]. In real device processing applications the diffusion length could be significantly larger, because of various mechanisms that can accelerate the diffusion, but these curves serve as a guide to the absolute maximum in thermal exposure. The multi-gate device contemplated by the ITRS 2003 at the 32 nm node has a physical gate length of only

13 nm and a channel thickness of ~ 10 nm [2]. In such a device, diffusion by more than 1 or 2 nm will have a strong impact on the properties. Fig. 10 shows that in this case, thermal processes above 750°C will all have to be performed in the RTP regime if B doping is present. In reality, the thermal budget after formation of s/d regions and gate activation will have to be much lower because otherwise the metastable doping levels will tend to deactivate [16,23].

Thermal budget reduction will also be essential after formation of NiSi contact regions because these structures would rapidly degrade when exposed to temperatures >600°C [24,25]. This aspect will be discussed further below.

The issue of controlling contamination is also becoming increasingly relevant, and it is especially evident in the processing of ultra-thin dielectrics, where sub-monolayer interface layers can have a major impact on device performance [13]. Ultra-pure ambients, and controlled fluxes of gaseous species at the wafer surface play an essential part in production of highly-scaled devices. Issues of chemical and particle contamination are also subject to severe scaling requirements, and design of advanced tools must consider these aspects. RTP has an inherent advantage as compared to furnace or other hot-wall heating technologies because the wafer is always hotter than the process gas that surrounds it. In this situation, the large thermal gradient in the gas next to the wafer induces thermophoresis, where particles are repelled from the wafer surface [26].

THE CHALLENGES OF DOPING: ACTIVATION vs DIFFUSION vs DEFECTS

The discussion above shows that one of the key challenges as CMOS scales beyond the 45 nm node arises from how to introduce the doping profiles that are needed to control the carrier flow in the transistor. There are three challenges that are intimately linked by the materials science of doping in silicon. The first challenge is the definition and control of the three-dimensional concentration profiles of the dopant species that are introduced during the doping process. The second challenge is in the related issue of what fraction of these impurities contribute charge carriers, i.e. the process of incorporating electrically active dopants and maintaining their activation throughout the entire fabrication process. The third challenge arises from the need to ensure that any crystal defects that are created during doping and activation processes do not create mischief, e.g. by inducing leakage currents in p-n junctions.

Currently, ultra-shallow junctions are formed through the combination of low-energy ion implantation and RTP cycles at high temperatures that activate ion-implanted dopants with minimal diffusion. As devices have scaled down, the general trend has been to adjust the RTP process by increasing the annealing temperature while simultaneously reducing the time at temperature, e.g. by moving from soak anneals to spike anneals. This trend is driven by the difference between the thermal activation energy for dopant diffusion and that for electrical activation [19,27,28]. Fig. 10 illustrates the origins of the trend. The activation energy for intrinsic B diffusion is 3.46 eV. The dashed curve represents the time taken to activate 50% of the carriers that can be introduced by an implant of 10^{15} B/cm^2 at 250 eV [28]. The activation energy for the latter process was deduced to be ~ 4.7 eV. Since this process has a higher activation energy than that for diffusion, it is kinetically favoured at higher temperatures. Hence, we can reach the 50% activation point with less diffusion by annealing for a shorter time at a higher temperature. Various researchers have found that this trend holds for activation of B species implanted in silicon. Fig. 10 suggests that annealing this implant with only ~ 1-2 nm of diffusion would require an annealing cycle of ~ 1 ms duration at a temperature just below the melting point of silicon.

However, the optimization of doping profiles in advanced device technologies is a complex matter that requires the very delicate balance of requirements discussed above. In recent years, some device manufacturers have even chosen to reduce the temperature of the

spike anneal, favouring improved control of doping abruptness over electrical activation [29]. The struggle with the science of doping is well reflected in the evolution of the doping requirements of the ITRS and the industry's attempts to meet them. Fig. 11 shows how the ITRS roadmap for PMOS s/d doping requirements evolved between 2000 and 2003 [2,30]. The trend-lines show the desired trade-off between junction depth (X_J) and sheet resistance (R_S), and the figure includes values that were deemed appropriate for devices at various technology nodes. The technology node is defined through the half-pitch for DRAM technology, but since the precise definitions of technology nodes changed slightly over time, the points for each "node" were taken for devices with similar physical gate lengths. The ITRS 2000 update still emphasized the desire for simultaneous improvements in junction depth and sheet resistance, but later editions in 2001 and 2003 accepted the reality that this would not be easily available from existing techniques that could be accepted in manufacturing.

These compromises are unacceptable in the sub-45 nm nodes, as the need for reduced R_{SD} becomes essential [8,31]. R_{SD} arises from a number of components, and there has been some debate about which elements are most important, but it is clear that two aspects are critical: (a) The formation of ultra-abrupt heavily-doped s/d extension junctions, and (b) the formation of silicide contacts with very low contact resistivity [14,32,33].

A wide variety of processing techniques is being explored to attempt to meet the X_J / R_S challenge for USJ formation. Relatively conventional approaches include reduction of the ion implant energy, co-doping, spacer optimization and RTP spike anneals [34-37]. These efforts have benefited from the strong existing infrastructure of ion implantation and RTP annealing technologies. At the opposite extreme, exotic methods that can provide activation levels well in excess of the solid-solubility limit are being explored. For example, pulsed laser melting of doped surface layers can incorporate very large concentrations of electrically active dopants [35,38]. RTCVD of heavily B-doped SiGe films also can provide extremely high concentrations of active dopants [39].

Recent developments in RTP technology have included a strong emphasis on further reductions in the time at temperature, for example by reducing the "peak width" of spike anneals, as reflected in the time spent at temperatures greater than 50°C below the peak temperature [37,40]. However, the peak width for conventional RTP systems is usually limited by the maximum cooling rate of the wafer and by the time taken to switch off the heating energy sources, which are usually tungsten-halogen lamps. These factors typically limit the peak-width in conventional RTP systems to $> \sim 1$ s. More aggressive spike-width reduction is possible through the use of CW arc-lamp energy sources, which can be switched off very fast and can provide spike anneals with peak widths of ~ 0.3 s [41]. Such reductions in peak-width may be useful for activation of certain dopants and for further reductions in the thermal budget of RTP processes in the near term. However, for USJ formation, it has long been recognized that the trade-off between defect annealing and dopant diffusion illustrated in Fig. 10 ultimately leads to a need for millisecond-duration heating cycles with peak temperatures somewhat below the melting point of silicon [19]. Early studies used CW laser or electron beams swept across the surface of the wafer to induce millisecond annealing, but such methods were not cost-effective for manufacturing and research was largely abandoned because in this era there was no commercial need for extreme reduction in dopant diffusion [42-44]. In recent years, the imminent crisis in R_{SD} has led to a renaissance in millisecond annealing and several alternative techniques have emerged [45-53]. Although these approaches require a radical departure from conventional RTP heating technology, millisecond annealing is attractive because it appears to offer a solution for forming advanced junctions that does not require extensive changes in the process integration scheme.

Fig. 12 compares results achieved using conventional RTP spike anneal technology to

those from millisecond annealing with the flash-assisted RTP™ (fRTP™) approach [46]. fRTP™ combines a fast ramp to an intermediate temperature with a pulse of energy from an array of powerful water-wall flash-lamps that produces a temperature jump at the surface of the wafer [45-48]. The study included a comparison of the results from samples doped by conventional beam-line implantation with BF_2 and samples implanted by a plasma doping approach with a BF_3 source gas. The results from the fRTP™ results show a significant improvement in the X_J / R_S performance relative to those from conventional RTP spike annealing. In fRTP™, the ability to adjust the intermediate temperature and the magnitude of the temperature jump induced by the pulse of lamp energy also provides flexibility in tuning the amount of diffusion relative to the amount of activation. This may prove to be useful in optimization of the very small degrees of diffusion that may be needed for tuning overlap with the channel and in reducing problems that may arise in completely diffusion-free anneals, which may exacerbate the effects of line edge-roughness at the gate electrode [54]. The use of an elevated intermediate temperature also reduces the pulse energy needed to reach the millisecond annealing temperature, and hence it reduces the magnitude of induced stresses and pattern effects [47].

Fig. 12 shows that the fRTP™ approach can clearly satisfy the ITRS X_J / R_S requirements down to at least the 45 nm node, and it is expected that the approach will be extended to the 32 nm node [48]. Fig. 12 includes a comparison of the process results with predictions of the X_J / R_S trends expected for box-shaped doping profiles with various concentrations of electrically active boron [36]. The concentrations for two of the curves were chosen so that the curves fell close to the X_J / R_S results from the spike anneals and the fRTP™ anneals. There is > 100% improvement in electrical activation with the fRTP™ approach. The curve shown for the concentration of $4x10^{20}$ B/cm^3 indicates the electrical activation needed to meet the needs of the 18 nm node. Further advances in millisecond annealing, such as the flash-solid-phase-epitaxy approach, may provide such high activation levels [55]. Millisecond heating approaches may also find applications beyond the USJ field, in other situations where thermal budget minimization is required [56].

The challenge of doping has stimulated R&D into many alternative schemes, with the main focus on the USJ for s/d extension regions. However, the issues involved in the engineering of the "deep" s/d region are also becoming increasingly challenging. The rapid reduction in the depth of these junctions has led to an additional problem which is that the formation of the silicide contact consumes too much of the doped region, potentially leading to leakage problems [2]. The change from the use of $CoSi_2$ to NiSi has helped to reduce the silicon consumption, but further progress requires the use of elevated s/d regions formed by CVD of Si or SiGe [3]. The need for this approach is especially evident in advanced SOI technologies, where the very thin SOI layers do not allow the conventional approach and an elevated contact is mandatory [57]. Elevated extension regions may also be required to reduce the parasitic resistance further [58,59].

Contact resistance reduction is possible through increased doping of the "deep" s/d region, although activation limits are also a major problem here. The use of SiGe allows new opportunities for contact resistance reduction because of the bandgap reduction combined with the ability to introduce extremely high concentrations of B [39]. The use of SiGe in the s/d contact regions has recently been exploited to also introduce strain in the channels of 90 nm CMOS devices, and further progress with this kind of approach can be expected [60,61]. Indeed it has been suggested that the ion-implantation process could be eliminated and that all the doping for the s/d structure, including the extension region, could be introduced during RTCVD of SiGe layers, but this approach poses major process control problems that have yet to be resolved [35].

The problems of doping are even more complex in multi-gate devices, where the non-planar geometry makes the use of conventional ion-implantation schemes more difficult. One of

the main challenges in these technologies arises from the need to reduce the parasitic resistance of the s/d regions and contacts [62]. If these resistances cannot be reduced, then the scaling benefits of the multi-gate approach may be negated. Clearly, the ability to produce very high activation levels and abrupt doping profiles can be very helpful for these technologies [63,64].

Doping approaches will be influenced by the introduction of new materials, especially high-k gate dielectrics and metal gates. For the conventional CMOS flow, where the gate stack is formed before the s/d doping and activation anneals, issues of thermal stability in the new materials may be very important. It has been argued that for low power electronics, where these materials are mandatory beyond the 45 nm node, low-temperature activation approaches, such as solid-phase epitaxial regrowth of heavily doped amorphous layers, may be required [47]. However, remarkably little is known about the thermal impact of high temperature millisecond anneals on structural transformations in these materials, and there is plenty of room for innovation in this area. Alternative process integration schemes, such as the gate-last approach, where the gate is formed after the s/d activation anneal, may also be considered [6]. Annealing schemes will also have to fit in with the widespread adoption of new materials and structures used for improving channel mobility, such as strained layers.

THIN DIELECTRICS, INTERFACE & TOPOGRAPHY ENGINEERING

In advanced devices, almost all the dielectric films are “thin” dielectrics that are conveniently formed through rapid thermal oxidation or through deposition approaches such as atomic-layer deposition (ALD). RTP has become widely adopted for oxidation, nitridation and annealing dielectric films. The ability to use higher process temperatures for short times leads to less stress in the films, as well as benefits in reduction of thermal budget and in reduction of stress-induced defects in the substrate [65-68]. RTP allows the use of a wide range of process gases, including steam. RTP oxidation with steam has expanded the range of RTP applications and can provide further benefits in thermal budget reduction. Steam can be used with either oxygen and hydrogen-rich ambients for a variety of advanced oxidation processes [69,70].

In some applications, it may also be useful for RTP to be clustered with other processes, such as precleaning, CVD, ALD or plasma nitridation. Clustering of process modules makes sense when there is a strong technical driving force for minimization and/or control of the delay between processes, or when the wafer must be kept in a very tightly controlled gas ambient between process steps [71]. In many applications, stand-alone RTP approaches can be equally successful, while providing greater flexibility in tool utilization.

In recent years, much of the focus in dielectric development has been on developing ultra-thin gate dielectrics for CMOS transistors [13]. Fig. 8 shows the evolution of the gate dielectric requirements for high-performance, low operating power and low standby power CMOS technologies [2]. At the 45 nm node, the requirement for the gate dielectric in the high-performance CMOS is an EOT of 0.7 nm, and by the 22 nm node, this has decreased to 0.5 nm. It has been suggested that the high-performance requirements can be met by silicon oxynitride films all the way to the 22 nm node but that for the low power technologies, a change to high-k dielectrics is mandatory in order to prevent excessive gate leakage currents [2,12]. However, the difficulties with introducing these new materials into the heart of the CMOS device has delayed the adoption of high-k materials, so further progress in oxynitride technology is critical, at least for the 45 nm node. Much of the progress in the SiON system has come from increasingly sophisticated approaches for raising the nitrogen content of the film, which tends to increase the dielectric constant, as well as being necessary to prevent the penetration of B from doped polysilicon into the channel during high-temperature processing [13,72]. Plasma nitridation approaches have been shown to be useful and an important aspect of the process is

the post-nitridation RTP anneal, which stabilizes the film [72,73].

Another approach for creating thin SiON films with very high N content involves RTP processing in NH_3 to grow a thin nitride by direct nitridation of the silicon surface, followed by a reoxidation step that improves the interface quality [74-76]. This process has yielded promising results for thin SiON films, and may even present advantages in terms of process uniformity.

Despite the challenges of high-k materials, it seems likely that high-k films will eventually be successfully incorporated in CMOS technology. Currently, the most promising film is based on the HfSiON combination, which has come the closest to meeting the formidable set of requirements, including a high-k value, appropriate band alignment, low leakage and thermal stability that is compatible with s/d activation anneals and polysilicon gates. Nitridation of the film improves thermal stability and reduces issues of boron penetration [77,78]. Various deposition processes have been pursued for high-k films, mainly based on MOCVD or ALD technologies, and RTP process steps are being incorporated for post-deposition annealing that improves film stoichiometry and purity and also for pre-deposition surface conditioning [15,56,79].

The surface preparation for high-k gate dielectric formation is especially challenging, since the nature of the interface between the high-k film and the channel is critical for device properties, especially the mobility and interface states [14]. As dielectric films have become extremely thin, the behaviour of the interfaces is becoming a dominant factor. This calls for progress in interface engineering technologies, and RTP will be a key contributor in the development of processes that can tailor these interface properties. When we consider that the EOT target for the 22 nm node of HP-CMOS is 0.5 nm, we can see that the entire film thickness lies within what was previously considered an interfacial layer! For high-k integration, these interface layers can greatly degrade the EOT of the gate dielectric "stack" because they add an undesired capacitance in series with the high-k layer [13,14]. Tailoring these processes will call for innovation in RTP processing, and that work will undoubtedly benefit related applications where the performance of thin dielectrics is critical, including the formation of tunnel oxides or nitrides and interpoly dielectrics in flash memory, as well as the processing of capacitor dielectrics in DRAM and other high-capacitance dielectric applications [80].

RTP processing will also continue to expand to applications for forming and annealing a wide variety of dielectric films. For example, the formation of shallow-trench isolation structures requires careful engineering of the trench geometry, especially with respect to the corner regions where stresses can generate defects in the silicon substrate [68]. In these regions, the trench liner oxide thickness also tends to vary as a consequence of the impact of stress and crystal orientation on the oxidation rate. RTP allows the use of high oxidation temperatures for short times, which leads to more uniform films and also allows less time for stress-induced defects to evolve in the silicon [66,67]. Applications where RTP processing enables optimization of stress and topography can be expected to expand in the era of three-dimensional CMOS devices, where engineering the corners and smoothing the surfaces of silicon fins and other multi-gate structures will be critical [81-83].

RTP will also continue to be used for applications such as gate contact and/or gate-sidewall oxidation, which is essential for repairing damage from gate etching processes, and for forming sidewall spacer structures. In gate stacks that contain metals such as tungsten, selective oxidation processes can be especially useful [70,84].

As we look out at the 22 nm node, we can see that the needs for gate dielectrics with EOT values of ~ 0.5 nm may not be compatible with any of the common processing techniques being considered today. In this era, the interface engineering is truly at the atomic scale. The complete elimination of an interface layer may become necessary, suggesting that lattice-matched epitaxial growth of the gate structures

may be necessary [13,85]. Monocrystalline dielectrics may also provide other advantages such as the absence of the dielectric relaxation phenomena that may limit the stability of amorphous high-k materials [86]. Possibly the use of molecular beam epitaxial growth in a UHV environment may provide a sufficiently stable processing technique, but clearly such fabrication methods will be very challenging for manufacturing costs. This may put renewed emphasis on methods of low-pressure vapour phase deposition approaches with sufficient ambient purity [87].

GATE METALS AND WORK-FUNCTION ENGINEERING

Depletion effects in polysilicon gate electrodes can cause a significant reduction in the capacitance of the MOS gate stack in inversion, typically introducing 0.4-0.5 nm of extra EOT [6]. The development of RTP technology for improved gate activation is being pursued, including methods based on millisecond annealing or even pulsed laser annealing [47,88]. SiGe gates may provide improved activation levels combined with reduced thermal budget [16]. The depletion problem can be completely eliminated by replacing the polysilicon with a metal or silicide, where the carrier density is far higher and depletion effects are negligible [6]. Metal gate structures may also be more compatible with new high-k materials, which often form undesirable interface structures when contacted by polysilicon [89,90]. There may also be further circuit performance advantages from reduced resistance of a metal gate, especially in mixed signal circuits. Control of metal gate work-functions will also be a critical factor in FD-SOI and multi-gate device technologies since in these devices, doping does not provide a convenient approach for threshold voltage control [91].

The importance of metal gates for future semiconductor devices has stimulated a resurgence of work on the materials science of the gate electrode and on fabrication approaches. It has even been suggested that metal gate technology may bring significant benefits, even without a change to a high-k dielectric. However, a change from polysilicon also brings severe challenges in materials science and for the process integration approach. The normal CMOS process flow, where s/d doping and activation is performed after gate formation, poses a serious difficulty with respect to thermal stability of the metal gate.

A basic problem with a switch to metal gates arises because for bulk CMOS, it is necessary to use gate electrodes with different work-functions for the NMOS and PMOS devices [6]. Hence the quest for suitable metals becomes a challenge of work-function engineering. The need to deposit and pattern two separate metals also adds process complexity, and there has been considerable emphasis on finding approaches that require fewer process steps. Several approaches rely on depositing one metal and then adjusting its work-function on one set of devices by a modification process, such as an ion implantation step or an alloying process [92].

One promising approach for forming metal gates is through the "full-silicidation" of a silicon gate ("FUSI" process) [93,94]. In this process, a metal layer is deposited over a polysilicon gate and completely converts it to a silicide layer, which acts as the gate electrode. The approach has been evaluated for $CoSi_2$ and NiSi electrodes, although the latter has received more emphasis. By performing the process on a doped polysilicon layer, it is possible to create a pile-up of dopants near the gate dielectric interface. The nature of the doping can be used to adjust the gate work-function [93,94]. This kind of capability may prove important for future metal-gate technologies.

This challenge of work-function engineering presents an opportunity where the excellent thermal and ambient process control of RTP can be very important. Process control will be crucial because the work-function of the gate electrode has a direct impact on the threshold voltage of the MOS device [95]. Processing of metals is also likely to require the same very tight ambient control capabilities that have been

typically associated with silicide processing requirements.

SILICIDES, CONTACTS AND INTERCONNECT

Thermal budget reduction is also taking place in the domain of silicides, contact and barrier layers and back-end-of-line (BEOL) processing. Here, the reduction in thermal budget is partly driven by the need to employ NiSi as the contact and gate silicide. Low-resistivity NiSi can be formed on very narrow lines, making it the material of choice for sub-90 nm-node CMOS [24,25]. It also has the benefit of consuming less silicon than $CoSi_2$ does. Various schemes for NiSi processing have been considered, but a consensus seems to be emerging on a two-stage process, where an initial anneal at at ~ 300°C is followed by etching and a second anneal at ~ 450°C [24]. RTP temperature measurement and control technology has evolved to allow reliable, repeatable processing in this low-temperature regime, combined with the traditional advantages of low thermal budget and an ultra-high purity gas ambient. The very fast diffusion of Ni in Si means that precise control of the thermal budget is important in NiSi processing.

Once the NiSi is formed, its thermal stability limits require that subsequent process temperatures do not exceed ~ 600°C [24,25]. Furthermore, the increasing use of SiGe materials in s/d regions means that the technology of NiSiGe materials is becoming more significant, and their thermal stability limits are even lower, and BEOL processes would have to be limited to < ~ 500°C [24,25]. Addition of other metals, such as Pt, may be necessary for improvement of the thermal stability.

Another motive for lowering BEOL process temperatures comes from the increasing significance of deactivation processes on the electrical activity. Since advanced doping processes produce metastable doping concentrations that are above the solid-solubility limit, thermal exposure can lead to deactivation, which undoes the good work of the activation anneal [23].

Further progress in contact technology will aim for continuing reductions in the contact resistivity. Reduction of the potential barrier is one possible direction, and it has been suggested that separate silicides may be formed for PMOS and NMOS for optimal performance. RTP processes for such materials (e.g. PtSi and $ErSi_2$) will need development [96,97].

The need for low thermal budget processing after doping and NiSi processes suggests that RTP applications may extend to BEOL applications such as Cu metal anneals and low-k film curing [98-100]. It has previously been shown that there are technological advantages to using RTP for these applications, and low-k curing may benefit from high ramp rates, ~ 100-150°C/s, that are only possible in RTP. However, cost-of-ownership factors previously favoured the use of batch furnaces. Despite this, the general trend for increasingly precise and short thermal cycles in a well-controlled gas ambient may ultimately favour the use of RTP even in these BEOL applications.

THERMAL PROCESSING TECHNOLOGY

We see that RTP needs to meet the requirements of a broad range of applications, but one common requirement is for highly repeatable and uniform processing on large diameter wafers. Currently, the leading edge technologies are manufactured on 300 mm diameter wafers, but we can expect a transition to the next wafer size to begin within a decade from now. The heating geometry in RTP tools exposes the wafer to essentially planar heat sources, which makes RTP rather easy to scale to larger wafer sizes without any compromise in ramp rate capability or process uniformity [101]. This is in marked contrast to the trend in batch furnaces, where increases in wafer size inevitably lead to poorer process uniformity, lower ramp rates and smaller batch sizes that compromise throughput [18].

One of the key benefits of RTP approaches for thermal processing is an inherently short cycle-time. This has clear benefits in product cycle-time reduction for the semiconductor device manufacturer [18,102,103]. However, it may have even greater benefit during development activity and yield ramps, where the rapid learning of how to optimize processes pays back dividends in minimization of development time. This aspect of RTP technology becomes crucial when new materials are being introduced and optimization of the process requires iteration in process conditions. An RTP tool can run a different process on every wafer in a cassette, allowing process temperatures, ramp rates and the choice of gas ambient conditions to be perfected very rapidly. Such flexibility is impossible in the batch furnace.

As device technology progresses, process control will continue to improve, and this is a central issue in RTP tool development. The primary process variable is the thermal history of the wafer, but close control of the ambient gas conditions is also essential in many applications. An ideal RTP system produces the same temperature-time cycle and the same ambient conditions at all positions on all wafers, regardless of the number of wafers processed or the nature of those wafers. In the modern manufacturing environment, this must be achieved at minimal cost, both in terms of expenditure of time but also in terms of expenditure of human intervention in the tool operation. Simplification and automation of tool set-up and operation are important objectives for continuing progress in RTP equipment technology.

Temperature control is the single most important technical issue in RTP equipment technology. Challenging specifications on temperature control are often driven by anxiety about the impact of temperature profile variations on the doping profiles present in devices. For example, the need for increasingly tight control on the extent of diffusion has stimulated demands for progressive improvements in temperature control during RTP spike anneals [104].

Since the adoption of RTP in the early 80s, there have been many steps forward in improving the control of wafer temperature [105]. Uniformity tuning approaches have evolved to allow temperature variations across a 300 mm wafer of ~+/-1°C. Emissivity-independent pyrometry provides temperature measurement that is independent from the nature of coatings on the back of the wafer, and allows closed-loop control throughout the heating cycle. This has been made possible through innovations such as Ripple Pyrometry™, which uses an in situ measurement of both the wafer emissivity and the stray-light intensity for dynamic compensation for the effects of these two variables [106,107]. This allows highly repeatable processing across different wafer types in applications such as spike-annealing. Another useful technique is the Hot Liner™ approach, where the combination of a dynamic thermal shield below the wafer and dual-sided lamp irradiation provides an extremely robust approach for compensation of wafer backside emissivity variations [108]. The choice of the best temperature measurement approach is application dependent.

Development in temperature measurement technology will undoubtedly continue as process control requirements continue to tighten and the range of RTP processes expands. One area where there has been great progress in recent years is in extending the temperature range covered by pyrometry to the low temperatures needed in NiSi processing, where it is useful to begin closed-loop control of the heating cycle at temperatures as low as 250°C. Fig. 13 illustrates temperature-time profiles for a range of low-temperature anneals performed using state-of-the-art RTP technology.

Within-wafer temperature uniformity control also continues to improve. One approach for improving RTP system performance is through model-based control (MBC), where sophisticated physical models of the chamber predict wafer temperature distributions and continuously optimize the electrical power sent to different lamp zones, thus enabling dynamic temperature uniformity

control. MBC approaches can give major improvements in process uniformity while keeping the system simple, reliable and economical. Fig. 14 illustrates the process uniformity achieved using an MBC control scheme for a rapid thermal oxidation process performed at 1100°C for 60 s. The wafer map illustrates results obtained from Mattson Technology's Helios™ RTP system. The oxide thickness measured at 121 points, with a 3 mm edge-exclusion, has a 1-σ uniformity of 0.18%, and the total temperature range across the 300 mm wafer is only 1.05°C. Such extraordinary results indicate the maturity of today's RTP technology.

The remaining challenge in temperature control is in management of the temperature non-uniformities induced by the presence of patterns in the thin film coatings on the front side of the wafer [108-113]. This issue probably already dominates the RTP process uniformity obtained in the production environment, although it may be difficult to identify this variation among a host of other manufacturing variations. Fig. 15 illustrates the impact of RTP heating configurations on the pattern effect during an ion implantation annealing process [109]. The simplest approach for reducing the pattern effect, while maintaining full flexibility in temperature cycles is through the use of dual-sided irradiation, which can reduce the pattern effect by 50%. Complete elimination of the pattern effect is possible through the use of the "Hot Shielding" approach, which retains most of the flexibility in thermal profiles [109,110]. This approach is practical for all conventional RTP processes except for fast spike-anneals [113].

The advent of millisecond annealing brings fundamental changes in heating technology. Millisecond processing requires selective heating of the wafer surface, generating a large vertical thermal gradient through the wafer thickness. The large thermal gradient is essential because it enables fast surface cooling immediately after the heating pulse, with the bulk of the wafer acting as a heat-sink [50]. Fig. 16 illustrates the principle and points out the important length-scales associated with the heat transfer. Rapid surface heating occurs when a pulse of radiant energy is absorbed in a surface region with a depth, d_{abs}, that is small compared to the thermal diffusion length, L_{diff}. Rapid cooling occurs if $L_{diff} << d_{waf}$, where d_{waf} is the wafer thickness, so that the bulk of the wafer remains much cooler than the surface during the pulse and can act as a heat-sink for fast conductive cooling. Surface heating can be induced by a broad-area pulse of radiant energy delivered uniformly across the wafer or from a focussed energy beam that is scanned over the wafer. Broad-area pulsed heating can be implemented with high-energy flash-lamps that can deliver the very large instantaneous power densities required [45-51]. As noted above, millisecond annealing can also be performed by scanning a high-power laser beam across the wafer surface [42,43,53]. Millisecond annealing technology will bring new challenges in process control. These techniques have to produce repeatable process results despite operating over much shorter time scales with much higher power densities than those employed in conventional RTP. USJ formation is still likely to require tight control of the thermal profile, although the definition of process windows for millisecond annealing requires further research.

Process uniformity control in millisecond annealing poses new problems. For broad-area heating, excellent uniformity of the energy density absorbed across the surface of the wafer is essential. For laser processing, special issues arise as a consequence of the 2-D heat transfer pattern associated with a scanned beam [51]. For example, if the energy source does not have sufficient power to produce a line beam that can cover the entire wafer, it may be necessary to overlap scans. This introduces a highly undesirable mode of processing, where the regions of overlap are not processed in the same way as the rest of the wafer [38,51].

One special challenge for process uniformity comes from the pattern effect, which may pose a significant problem in millisecond processing because it arises over a shorter length scale and could affect intra-die uniformity [114]. Fig. 17 illustrates the issue by showing the temperature non-uniformity that can be induced

by a stripe of a material with an absorptivity higher than that of its surroundings [115]. The calculations predict that even stripes as narrow as ~10 μm could induce significant temperature non-uniformity. This demonstrates the great reduction in the length scale of pattern effects in millisecond annealing as opposed to those in conventional RTP.

The usual concerns of repeatability are also relevant, and it remains to be seen whether closed-loop control is even necessary. If real-time control during the fast anneal is not used, it will be necessary to measure the surface temperature to assure a stable process, because an unmonitored open-loop process is clearly unacceptable in an advanced fab environment.

In millisecond annealing, the difficulties of temperature measurement are compounded by the need to measure the temperature rise over a very short period of time. For laser processing an additional problem arises from the very small area that is heated, which contains very steep lateral temperature gradients. Furthermore, all millisecond heating approaches inherently generate a large vertical temperature gradient through the thickness of the silicon wafer, and thermally emitted radiation does not all originate from the surface of the wafer. This problem, which is analogous to some of the issues in pyrometry of semi-transparent systems such as glass or hot gases, adds to the challenges in temperature measurement. Other problems, such as the effects of variation of the emissivity of the surface layers, will also require solutions.

Finally, it is worth considering whether thermal processing at even shorter time scales will ever be useful in device fabrication. Pulsed laser processing has been extensively evaluated as a means for ion-implant annealing, with the main focus on the melting mode, where extremely high concentrations of electrically active dopants can be obtained when the molten layer freezes [35]. Unfortunately, this approach has proved to be impractical because of the severe difficulties that arise from the effects of device patterns on laser power coupling combined with device distortion that can happen when silicon melts [35,38]. Various approaches have been explored for mitigating such problems, chiefly through the use of absorber layers and other thin film coatings that can help even out the energy absorption [38,116]. Despite progress in this area, the extra complications in process integration would make this path impractical for high-volume low-cost manufacturing.

THERMAL PROCESSING OF THE FUTURE: DO WE NEED IT AT ALL?

As we look beyond the 22 nm node, where device dimensions approach limits imposed by atomic spacing, it seems that a fundamental issue arises from the random nature of current doping schemes. This is becomes evident when one considers the very small number of dopant atoms present in the channel of current devices. This is already viewed as a problem for threshold voltage control, and the effect only becomes worse with device scaling. This is one of the arguments in favour of fully-depleted body devices, which have undoped channels, and where the threshold voltage is controlled by the work-functions of gate electrodes [117]. The limitations of the electrical carrier concentration available through doping also have fundamental impact on the gate electrode. The polysilicon depletion issue is one of the main driving forces for the introduction of metal gate technologies. Even in the s/d regions the limits from doping have stimulated interest in Schottky barrier s/d technologies, where the contact scheme does not require doping at the source and drain [97,118,119]. These trends show that a new science may be emerging, which aims to produce more controlled interfaces through innovation in materials engineering and in deposition technologies [87,120,121]. Processes of implantation and diffusion have a random nature that is not friendly to engineering at nm length scales. The trend is also visible in other parts of the transistor. For example, we already emphasized the need for near-atomic abruptness in the gate-dielectric/channel interface. The channel itself has become a thin film over an insulating substrate. At the 22 nm node, its thickness will be ~ 7 nm, even for a multi-gate

device, and its interfaces will dominate its capability for high-mobility transport.

These trends point towards evolution in the direction that has earlier been taken by III-V device technology, where growth of films, patterning and engineering of band-gap and strain distributions already dominate the technology. The future of device fabrication may lie in this direction, but there is a danger of a cost explosion, which would mean that the devices could not meet commercial objectives. This trend, far more than the limits of device physics or fabrication technology, threatens the end of Moore's law.

As we look at these extremely scaled devices, it is interesting to consider why we need heating processes at all. Heat provides the opportunity for statistical variation in atomic configurations. By selecting materials and process conditions, the application of heat allows the system to evolve towards a lower free energy state, hopefully one that is closer to the device we want to fabricate. However, in many cases, we are now trying to limit the process so that it does not evolve to the lowest energy state. This is the message behind thermal budget reduction – we want to "freeze" the device in a given state. Even advanced deposition processes need heat, whether it is to provide the activation energy for bond rearrangements, or to remove precursor species from a surface, or to allow defects to annihilate. As process technology advances, we will still need heat, but management of that thermal budget, and optimization with respect to the chemical/physical objectives, will become increasingly important. There is less room for statistical variation at the 1 nm length scale!

In addition to heat, we need to consider other methods for manipulating materials that may allow us new opportunities for innovation. Photonic effects are already a critical part of the semiconductor process flow – albeit in the field of lithography. There may be benefits in bringing photonic excitation into the world of materials processing [122-5]. Plasma exposure can also bring new species and energy distributions to the wafer [84,87]. Ion-implantation will have to evolve, and ion energies will reduce greatly, but new approaches, such as plasma immersion doping, have shown promise for the future [126]. Many of these processes may be combined with precisely controlled thermal treatments, where the heat serves its traditional role of enabling rearrangement and processing is terminated to "freeze" the desired structure. Processing will become more integrated, and RTP will often be clustered together with other processes. In many cases, an RTP chamber of the future may look more like a deposition, implantation or etching system, where processes are combined for optimal effect [79,120]. Despite this, the disciplines of RTP, temperature and ambient control, will still be the keys for success.

CONCLUSIONS

RTP technology has become the leading thermal processing approach for device manufacturing. As we look forward beyond the 45 nm node, the key applications for RTP will remain in the activation of dopants and annealing of defects, interface engineering, dielectric film formation and annealing, silicide and metal gate annealing, low-k film curing and interconnect metal and barrier layer annealing. New processing capabilities that provide ultra-high dopant activation with minimal dopant diffusion require millisecond annealing technologies, which will evolve rapidly as we move through the 45 nm era. As we head towards the 22 nm node, thermal processing will increasingly integrate itself within the arts of deposition, patterning and etching. In the volume manufacturing environment, process control across all points on all wafers will remain of paramount importance, while economic factors will demand simplification of operation and further strides in productivity. Finally, RTP will continue to expand its applications in non-traditional applications, such as those identified in Table II, where improved value is gained from uniform thermal processing of substrates for high-technology applications.

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[127] Magic Denuded Zone ® is a trademark of MEMC Electronic Materials Inc. (St. Peters, MO).

Node	**65 nm**	**45 nm**	**32 nm**	**22 nm**
Volume Prod.	**2005**	**2007**	**2010**	**2014**
Leading Tech.	Bulk Si	Bulk Si	FD-SOI	FD-SOI / Multigate
Dielectrics	SiON form/anneal	SiON form/anneal	SiON form/anneal	
	Surface nitridation	Surface nitridation	Surface nitridation	Surface nitridation
	Post-nitridation SiON anneal	Post-nitridation SiON anneal	Post-nitridation SiON anneal	Post-nitridation High-k anneal
	Sidewall oxide	Sidewall oxide	Sidewall oxide	Sidewall oxide
	Selective ox. (W-gate DRAM)	Selective ox. (W-gate DRAM)	Selective ox. (W-gate DRAM)	
	Sacrificial oxide	Sacrificial oxide	Sacrificial oxide	Sacrificial oxide
	Pad oxide	Pad oxide	Pad oxide	Pad oxide
	STI liner oxide	STI liner oxide	STI liner oxide	STI liner oxide
	Tunnel oxide	Tunnel ox./nitride	Tunnel ox./nitride	Tunnel dielectric
	Interpoly oxide	Interpoly oxide	Interpoly dielectric	Interpoly dielectric
	Deposited oxide densification	Deposited oxide densification	Deposited oxide densification	Deposited oxide densification
		High-k interface layer engineering	High-k interface layer engineering	High-k interface layer engineering
		High-k post-deposition anneal	High-k post-deposition anneal	High-k post-deposition anneal
				Multi-gate corner shape engineering
				Multi-gate channel surface smoothing
Doping Processes	Source/Drain extension anneal	Source/Drain extension anneal	Source/Drain extension anneal	Source/Drain anneal
	“Deep “ s/d anneal	“Deep “ s/d anneal	Raised s/d anneal	Raised s/d anneal
	Well & Channel implant anneal	Well & Channel implant anneal		
Gate Electr. Processes	Poly-Si/SiGe gate activation	Poly-Si/SiGe gate activation	Poly-SiGe gate activation	
		Metal gate work-function tuning	Metal gate work-function tuning	Metal gate work-function tuning
		Full silicidation of polysilicon (FUSI)	Full silicidation of polysilicon (FUSI)	Full silicidation of polysilicon (FUSI)
Contacts	$CoSi_2$ form/anneal			
	NiSi/Ni SiGe formation & anneal	NiSi/Ni(Pt) SiGe formation & anneal	NiSi/Ni(Pt) SiGe/NiGe formation & anneal	NiSi/Ni(Pt) SiGe/NiGe formation & anneal
			Dual silicide formation & anneal	Dual silicide formation & anneal
				Schottky S/D form
Interconnect	Barrier layer anneal	Barrier layer anneal	Barrier layer anneal	Barrier layer anneal
		Cu anneal	Cu anneal	Cu anneal
		Low-k curing	Low-k curing	Low-k curing

Table I: Applications for RTP in silicon device technology

Volume Prod.	2005	2007	2010	2013
Wafer Manuf.	Thermal donor annihilation	Thermal donor annihilation	Thermal donor annihilation	
	Magic Denuded Zone® [127]	Magic Denuded Zone® [127]	Magic Denuded Zone® [127]	
	COP Anneal	COP Anneal	COP Anneal	
	SOI surface smoothing	SOI surface smoothing	SOI surface smoothing	SOI surface smoothing
	Strained Si & SOI substrates	Strained Si & SOI substrates	Strained Si & SOI substrates	Strained Si & SOI substrates
Compound Semicond.	Contact annealing	Contact annealing	Contact annealing	Contact annealing
	Dopant activation: p-GaN	Dopant activation: p-GaN	Dopant activation: p-GaN	Dopant activation: p-GaN
	Implant anneal: GaAs	Implant anneal: SiC related	Implant anneal: SiC related	Implant anneal: SiC related
		Quantum well intermixing	Quantum well intermixing	Quantum well intermixing
		Selective oxidation for VCSEL	Selective oxidation for VCSEL	Selective oxidation for VCSEL
Si-based Optoelectron.		Waveguide engineering	Waveguide engineering	Waveguide engineering
			Nanoparticle formation	Nanoparticle formation
			CMOS integrated optoelectronics (incl on-chip comms)	CMOS integrated optoelectronics (incl on-chip comms)
Solar cell processes	Doping, oxidation, contacts	Doping, oxidation, contacts	Doping, oxidation, contacts	Doping, oxidation, contacts
Flat-Panel Displays	Crystallization, doping, oxidation, contacts	Crystallization, doping, oxidation, contacts	Crystallization, doping, oxidation, contacts	Crystallization, doping, oxidation, contacts
Data Storage	Magnetic film annealing	Magnetic film annealing	Magnetic film annealing	Magnetic film annealing
	FRAM anneal	FRAM anneal	FRAM anneal	FRAM anneal
		Ovonic memory processes	Ovonic memory processes	Ovonic memory processes
		MRAM processes	MRAM processes	MRAM processes
				Single-electron memory fabrication
Passive components	High-value capacitors	High-value capacitors	High-value capacitors	High-value capacitors
MEMS fabrication	Stress relief annealing	Stress relief annealing	Stress relief annealing	Stress relief annealing
				Doping, oxidation, contacts

Table II: Applications for RTP beyond conventional silicon technology

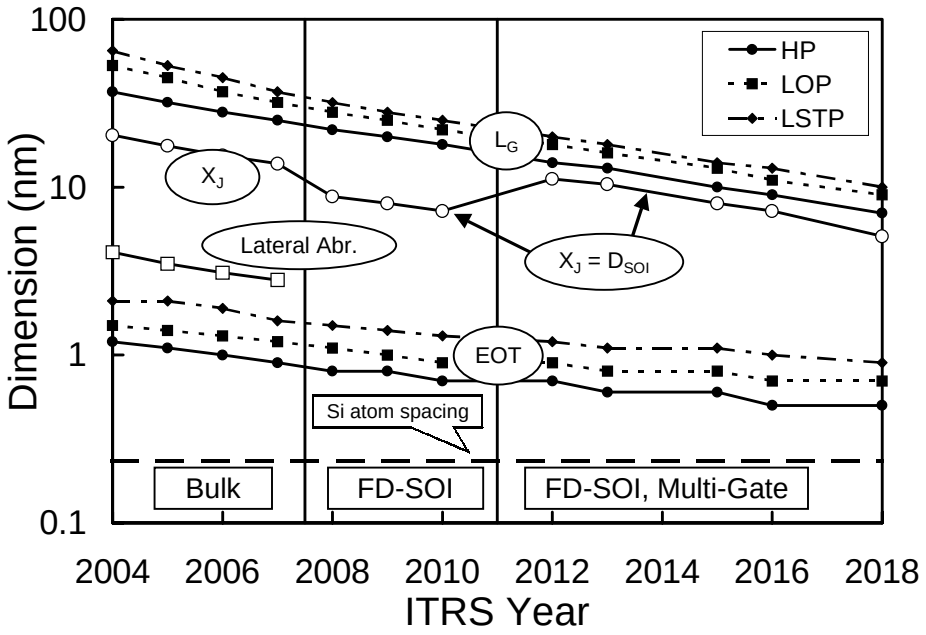

Fig. 1. The International Technology Roadmap for Semiconductors (ITRS) predictions for key device feature sizes from the 90 nm node (2004) through to the 18 nm node at the end of the current roadmap in 2018 [2]. Predictions are shown for the high performance (HP), low operating power (LOP) and low stand-by power (LSTP) families of CMOS devices. The ITRS contemplates an evolution of device architecture from bulk to fully-depleted SOI (FD-SOI) and then multi-gate devices. The trends include those for physical gate length (L_g), source/drain extension junction depth (X_J), lateral abruptness of the source/drain extensions and equivalent oxide thickness (EOT). Lateral abruptness specifications have yet to be developed for the FD-SOI & multi-gate devices [2]. Towards the end of the roadmap, critical device dimensions approach the limits of interatomic spacing.

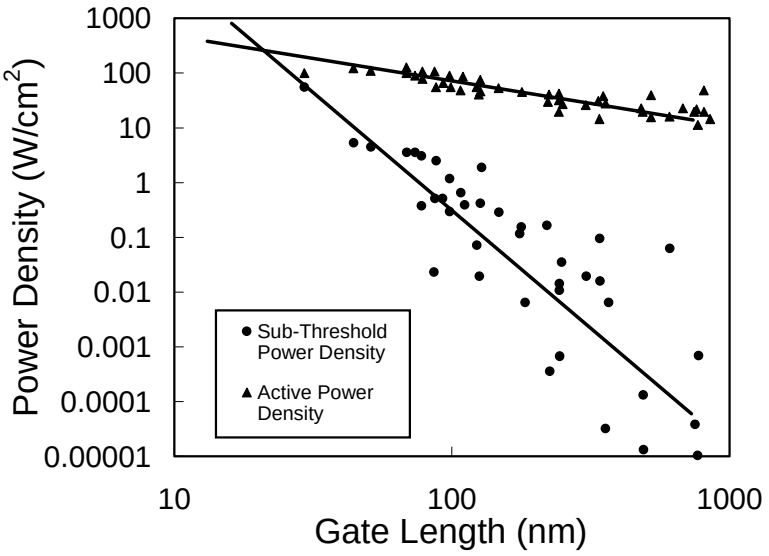

Fig. 2. MOS device power trends [4]. As devices have scaled below the 90 nm node, CMOS ceases to be a "power-friendly" technology, mainly because of the very rapid rise in the "off-state" leakage currents. Continued progress will require increasingly sophisticated approaches, including the use of new materials, device architectures and circuit designs optimized for power-management.

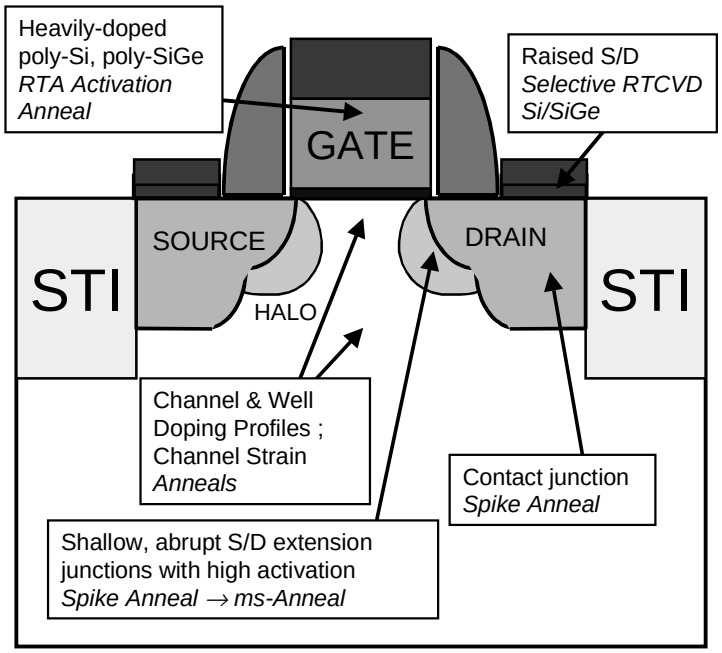

Fig. 3. The role of RTP in advanced doping and strain engineering.

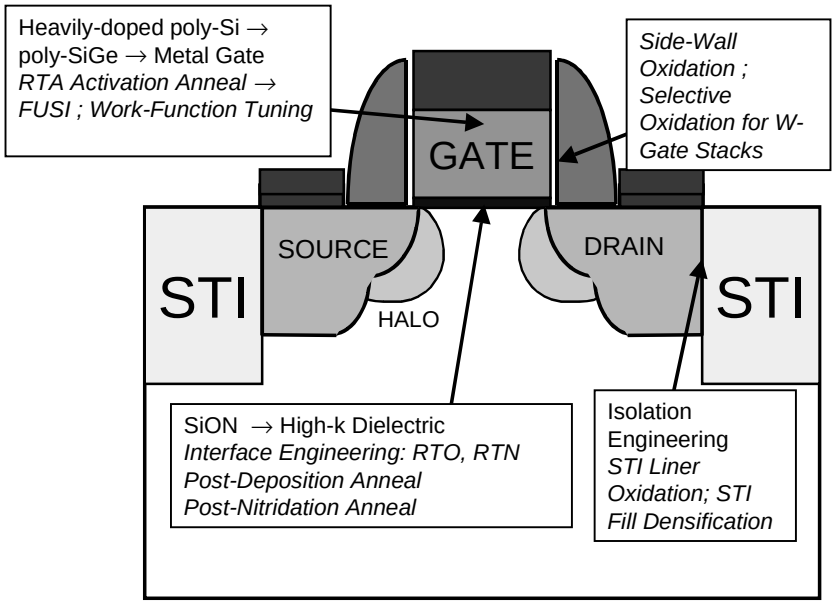

Fig. 4. Applications of RTP in gate stack and isolation engineering.

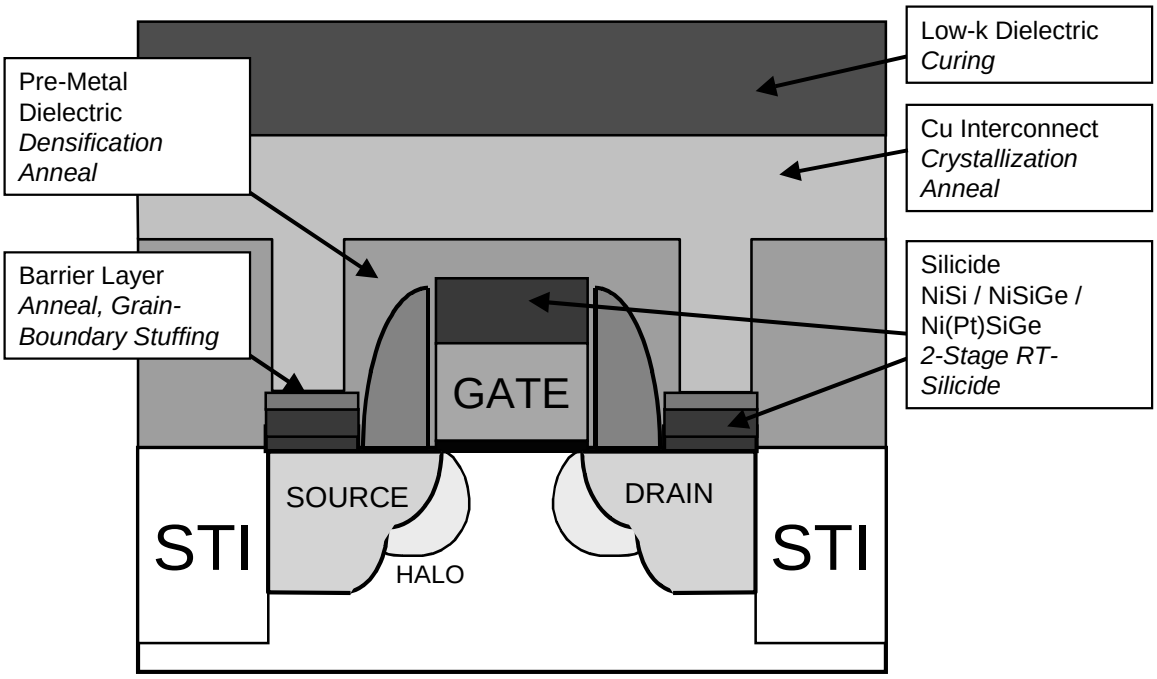

Fig. 5 RTP applications in contact and interconnect engineering.

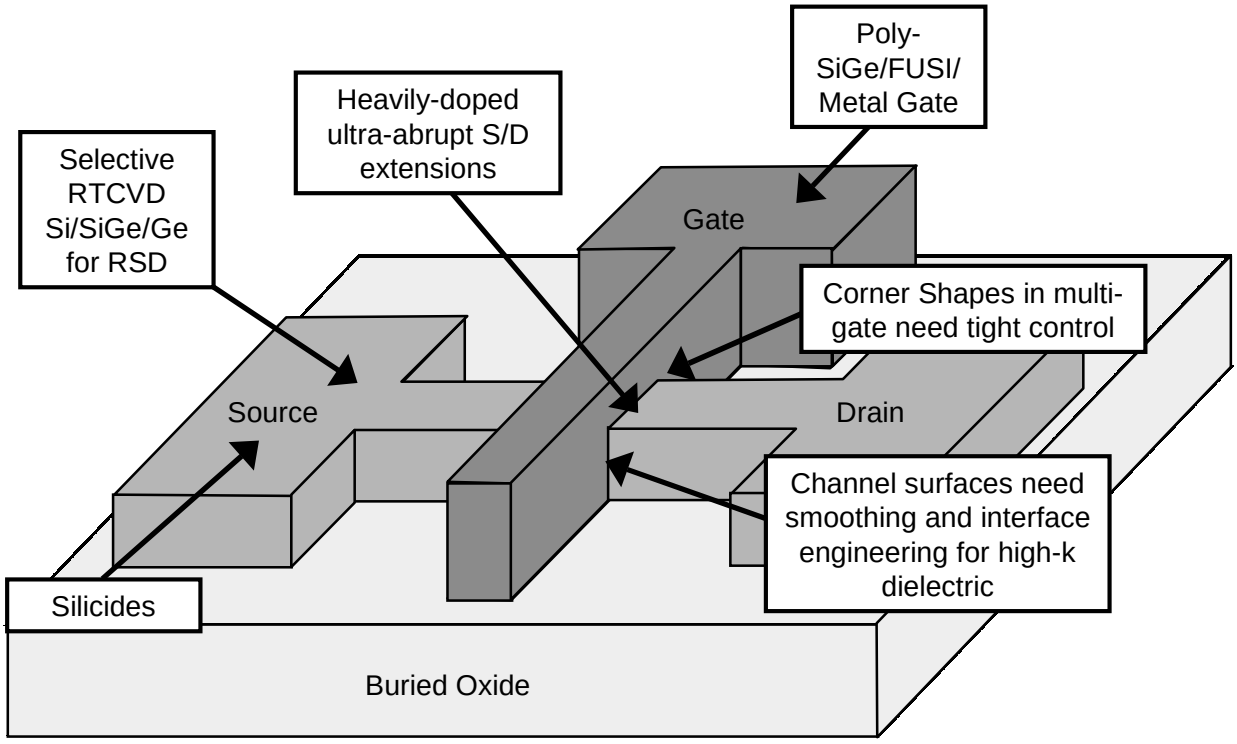

Fig. 6. RTP applications in processing of advanced multi-gate devices.

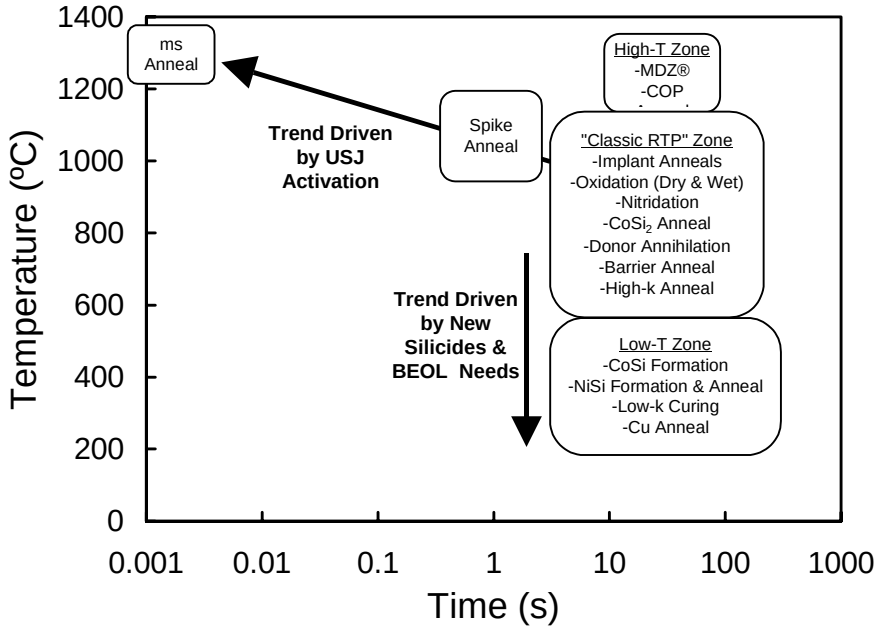

Fig. 7. The temperature-time domain of RTP continues to evolve. Recent trends include "hotter and faster" processes that enable the creation of advanced ultra-shallow junctions and low-temperature processing that is needed for NiSi formation and annealing.

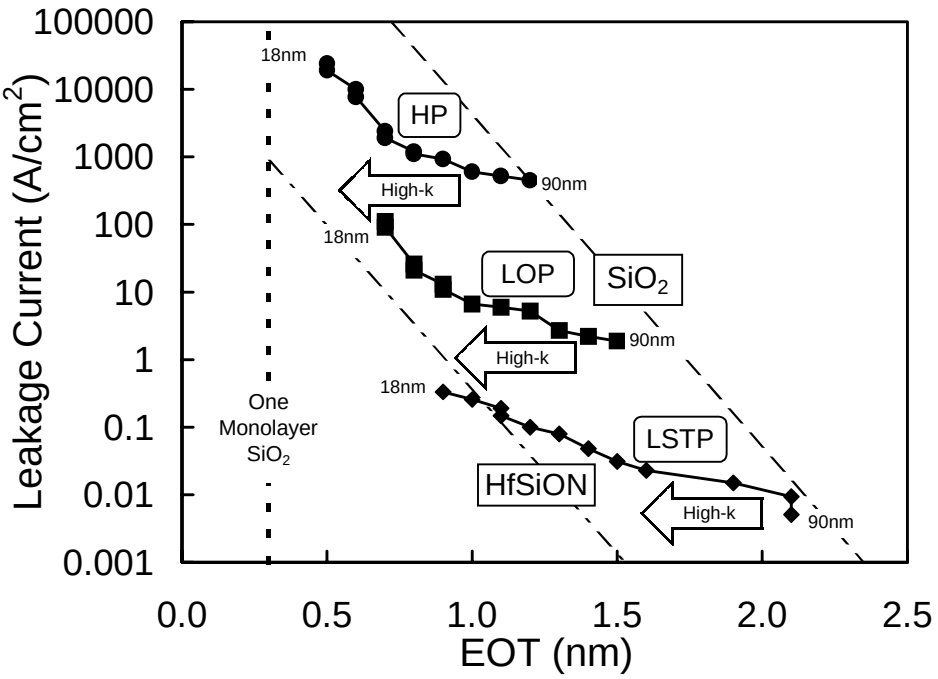

Fig. 8 Trends in the evolution of the requirements for gate dielectrics [2]. The figure shows the evolution from the 90 nm to the 18 nm node for the high performance (HP), low operating power (LOP) and low stand-by power (LSTP) families of CMOS devices. The arrows show the points where adoption of high-k becomes mandatory, according to the ITRS. The dashed lines marked SiO_2 and HfSiON indicate typical leakage-EOT trends expected for these materials [78].

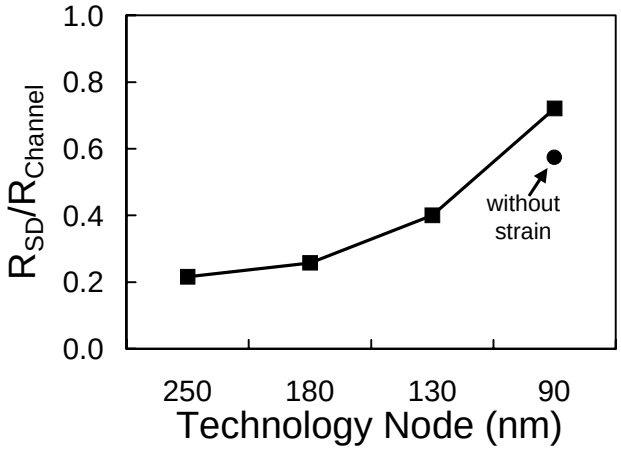

Fig. 9. The ratio of the source/drain resistance to the resistance of the transistor channel has been rising rapidly through successive technology generations [8]. Innovations such as strain, that help increase channel mobility, will exacerbate the trend. Ultimately, the parasitic resistance will limit device performance. New approaches for dopant activation and contact formation are essential to overcome this challenge.

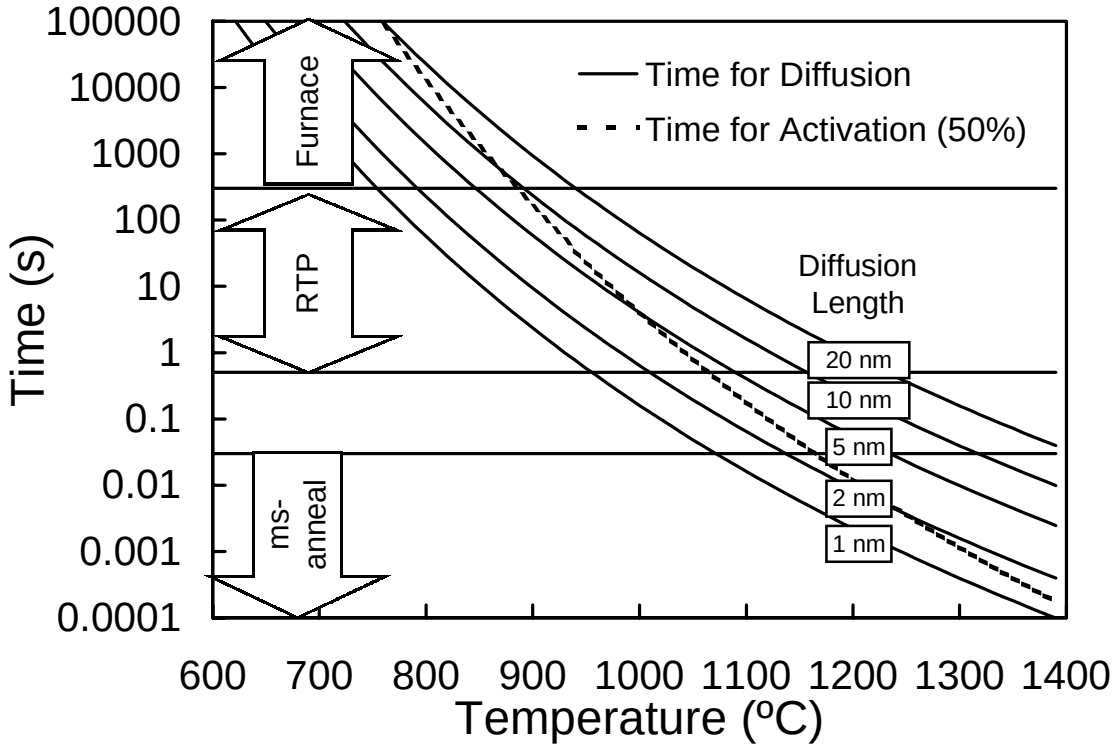

Fig. 10 Illustration of the thermal budget criteria for various degrees of B diffusion and for electrical activation of 50% of 10^{15} B/cm^2 implanted at 250 eV [22,28]. The diffusion lengths are minimal estimates based on intrinsic diffusion, and they do not include any enhancement effects. For advanced device technologies, where 1 nm of diffusion is significant, RTP processing is essential for most thermal steps. Activation of implanted dopants is only possible by very high temperature anneals with millisecond duration at temperatures just below the melting point of silicon.

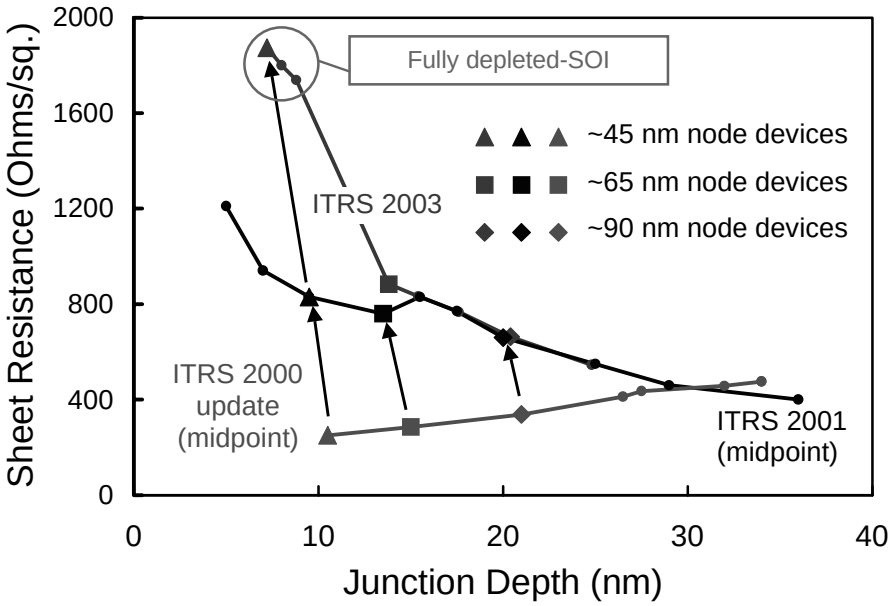

Fig. 11 Compromises in X_J/R_S requirements in recent ITRS roadmaps were necessary because of the difficulty in achieving sufficient dopant activation through conventional RTP [2,30].

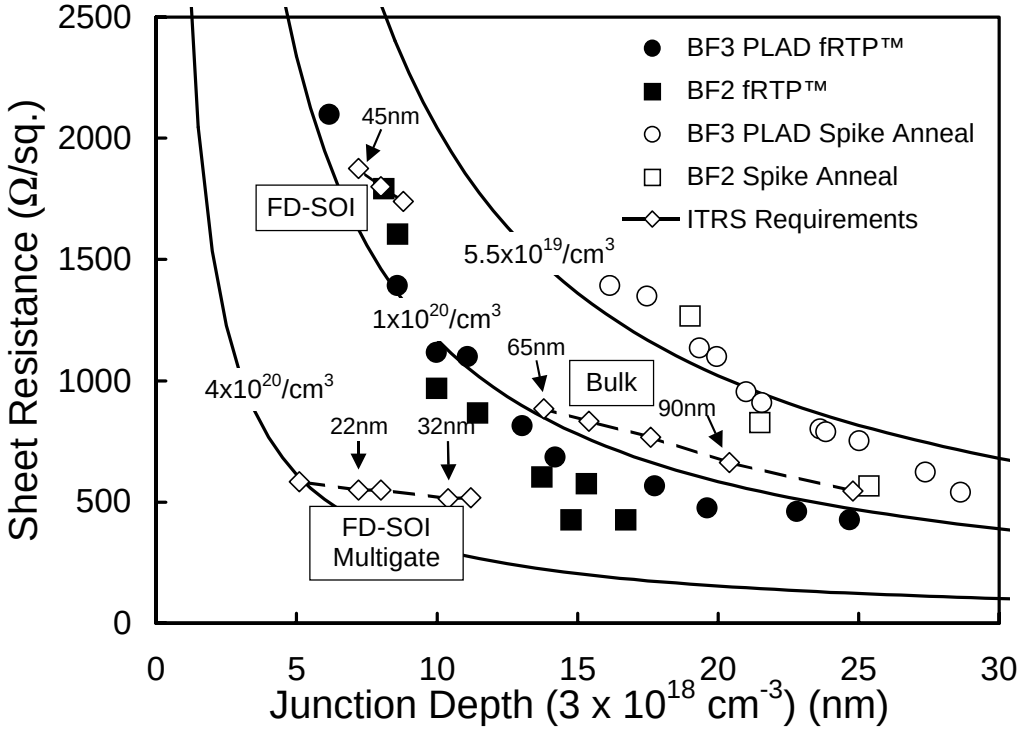

Fig. 12 A comparison of the X_J/R_S capability of flash-assisted RTP™ (fRTP™) and conventional spike anneals against 2003 ITRS specs [46]. ITRS specs vary for bulk, fully-depleted SOI and multi-gate devices. Solid symbols are fRTP™ results for plasma-doping (PLAD) or beam-line implants. Open circles are the corresponding spike-annealing results. The solid curves are predictions for ideal, box-shaped doping profiles with various levels of electrically active B (concentrations are marked on the curves) [36].

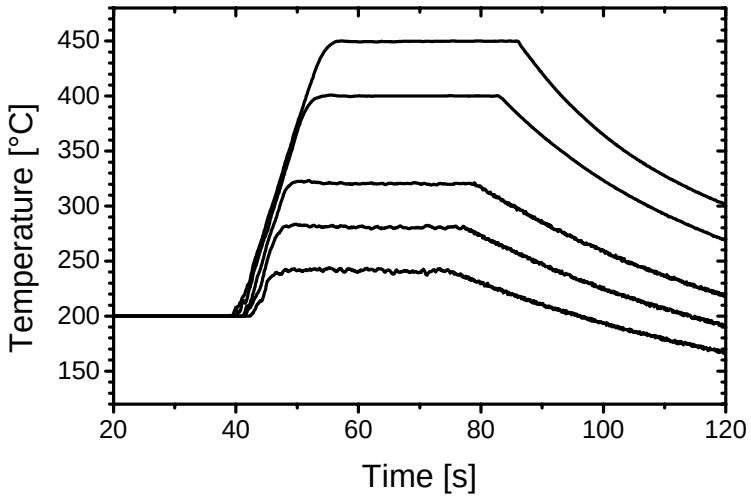

Fig. 13 Low-temperature heating cycles are becoming increasingly important for RTP processing of NiSi films (performance of Mattson Technology's Helios™ RTP system). Closed-loop control at temperatures as low as 250°C, together with relatively fast ramp-rates, will help integration of NiSi processes in advanced manufacturing.

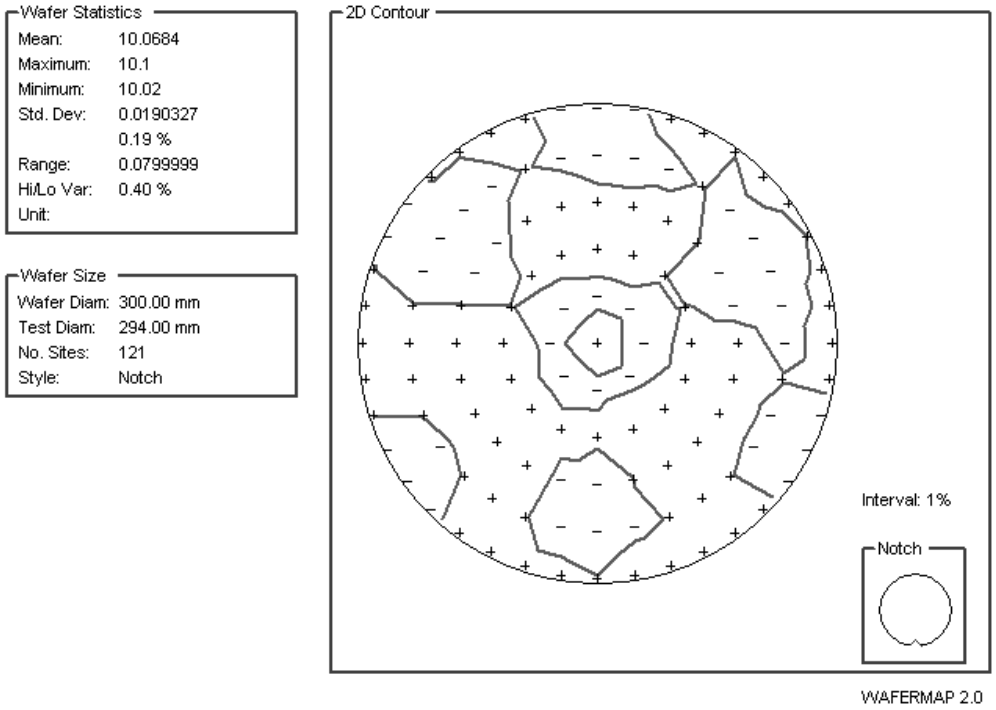

Fig. 14 Modern RTP systems can provide extraordinary within-wafer uniformity. This process result is from Mattson Technology's Helios™ RTP system. The temperature range from the RTO process of 60 s at 1100°C corresponds to a total temperature range of only 1.05°C across the 300 mm wafer.

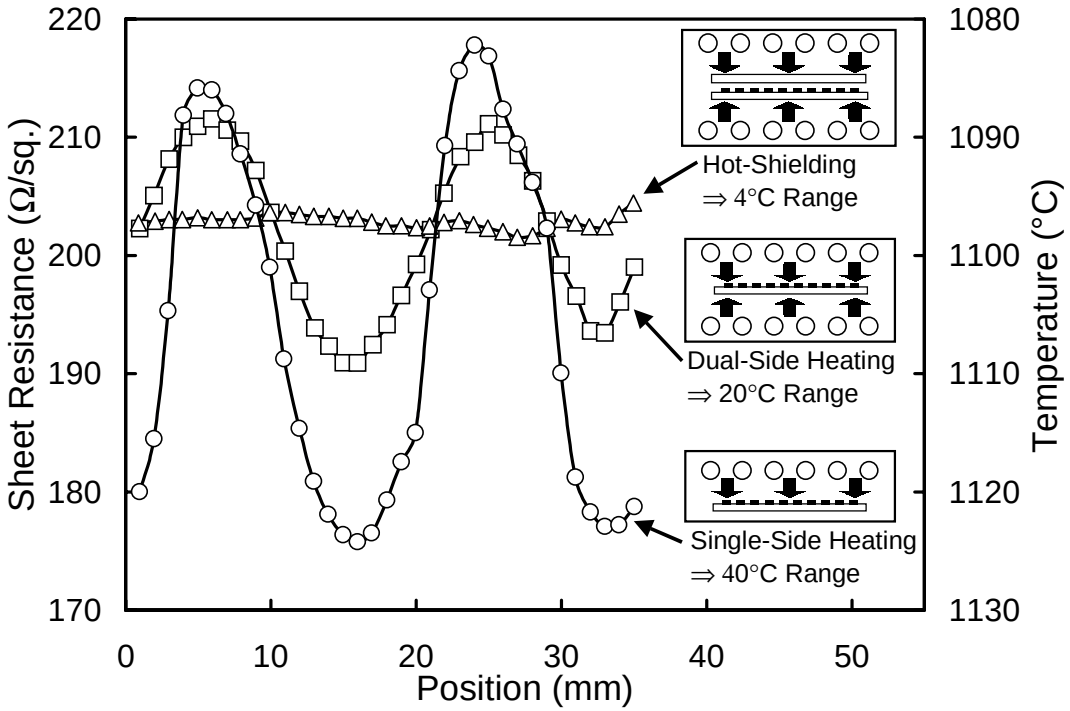

Fig. 15. The effects of RTP heating configuration on pattern effects during an 1100°C spike anneal of wafers implanted with 10^{15} As/cm^2 at 1 keV [109]. The results show the sheet resistance variation observed on a linear scan across part of the wafer. The wafer was patterned with a checkerboard pattern on its frontside and the metrology was performed on the backside, which had received the implant. The temperature scale is derived from the 1 Ω/(sq. °C) sensitivity of the process.

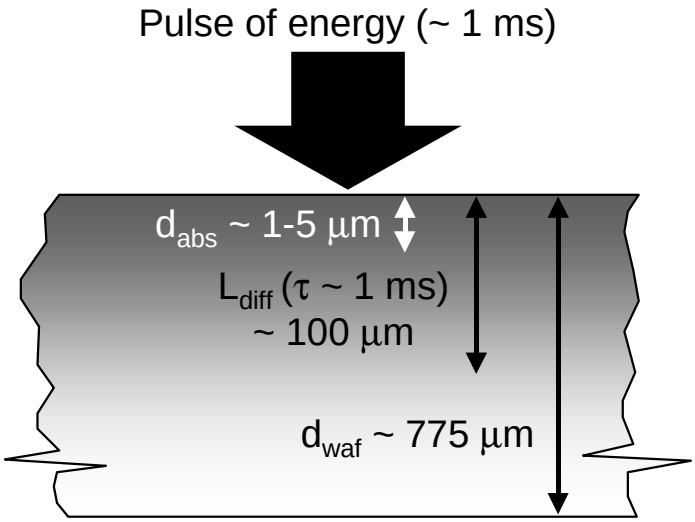

Fig.16 Critical length scales in millisecond annealing. For surface heating, the pulse of energy must be absorbed in a region (d_{abs}) that is small compared to the thermal diffusion length (L_{diff}). The bulk of the wafer remains cool during the energy pulse because $L_{diff} << d_{waf}$. After the pulse, the bulk acts as a heat-sink, leading to very fast cooling [50,51].

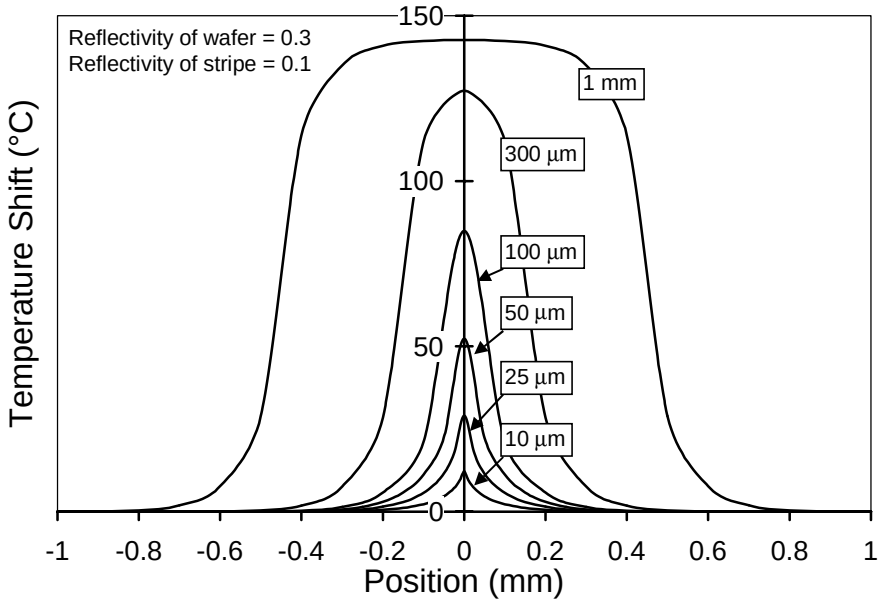

Fig. 17. Predictions of the pattern effect in pulsed heating [115]. The curves show the temperature non-uniformity expected to arise when a region that contains a stripe of absorbing material is exposed to a 1 ms duration pulse that produces a 500°C temperature rise on plain silicon. The numbers in boxes are the stripe widths. The absorbing region heats to a significantly higher temperature than the neighbouring silicon, producing a large pattern effect.