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# Damage-free, All-dry Via Etch Resist and Residue Removal Processes

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## Abstract

Using a unique inductively coupled plasma (ICP) technology, we have demonstrated an all-dry via cleaning process exhibiting extremely low plasma damage. Via test wafers were etched in two different oxide etch systems. Resist and residues were removed in an ICP strip system using $O_2$-only and $O_2/CF_4$ processes. Gate oxide integrity was determined by measuring leakage currents on antenna test structures of various sizes. Cleaned vias were examined under SEM and contact resistance measurements were performed. We found that the ICP processes exhibited leakage currents of less than 0.01nA for all test structures on damage test wafers. In addition, complete residue removal was observed by SEM and 100% yield was achieved for all contact resistance test wafers.

Key Words: Plasma ashing, resist strip, inductively coupled plasma, via residue clean, contact resistance.

## Introduction

With shrinking device geometry and higher plasma densities used in oxide etch, removal of post-via-etch polymer has become extremely challenging. Typical polymer removal processes involve the use of expensive organic solvents which are difficult to dispose of and environmentally unsound. Therefore, the need for all-dry plasma processes for post-oxide-etch resist and residue removal has become increasingly important[1]. These plasma processes must exhibit extremely low ion bombardment at the wafer in order to insure good gate oxide integrity and high device yield.

In this study, an inductively coupled plasma (ICP) strip system was evaluated for post-via etch resist and residue removal. The ICP source has been specifically designed to produce a high ratio of dissociation to ionization (2000:1). This results in a high density of reactive radical species and a much lower density of ions which can cause device damage[2]. A diagram of the source is presented in Figure 1.

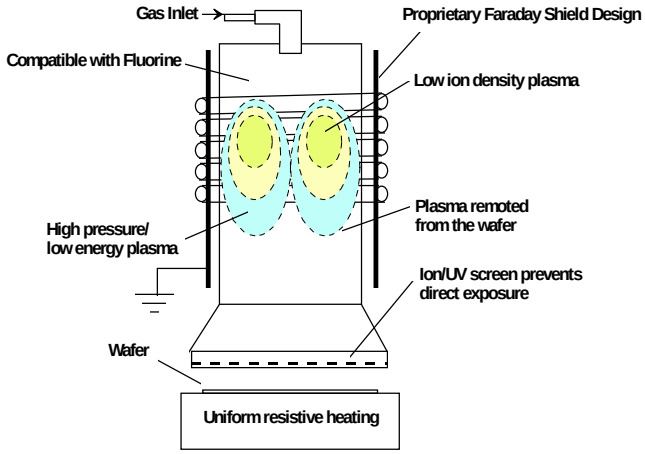



***Figure 1.*** *Mattson Technology Inductively Coupled Plasma (ICP) source. The patented Faraday shield design provides true inductive coupling of power to the plasma. Capacitive coupling is virtually eliminated, reducing the amount of ionization. The operating pressure is high (1.1 Torr) relative to other inductive etch sources, resulting in a low electron energy (avg. ~ 7eV) plasma, optimal for dissociation. Average electron energies of >12eV produce high levels of ionization.*

## Experiment

Several via test wafers based on 0.25μm design rules were produced for this study. Oxide etching was performed on two different capacitive, magnetically enhanced etchers using a polymerizing chemistry to achieve a tapered via structure.

ICP strip processes were developed to achieve complete residue removal (SEM analysis) and no TiN undercutting. Two processes achieved these goals: an $O_2$-only process and an $O_2$ process with a 15 second step containing $O_2$ + 1% $CF_4$. Both processes were run at 250°C, 1.1 Torr and 900 W RF power. The $CF_4$ process was run in order to compare contact resistance results with the $O_2$-only process. After developing these processes, a total of 8 via test wafers were run, 4 with the $O_2$-only process and 4 with the $O_2/CF_4$ process. These sets of 4 wafers were divided equally between the two oxide etchers. A DI water rinse was used as a post ash treatment for removal of any etch residues.

A plasma damage monitor wafer was run for each of the two ICP strip processes. These wafers have capacitors of various sizes built on them. These capacitors are in the form of antenna structures with ratios of gate to top layer antenna of 100,000:1, 1M :1, and 10M:1. They collect charge when exposed to a plasma environment and are used as an indirect test to determine the gate oxide integrity and failure mechanisms during plasma processing. A schematic of the final antenna structure is shown in Figure 2.

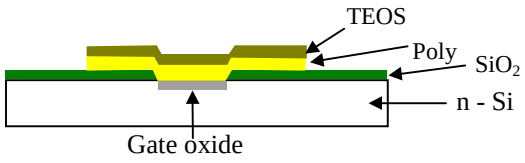



***Figure 2. Schematic of Final Antenna Structure.***

A voltage of 3.6V is applied through a probe to the gate oxide and leakage current measurements are taken. The chip site is considered as a fail if leakage currents greater than 1 nanoamp are observed. The current values obtained by this method are usually in the range of 0.001 to 0.005 nanoamp.

After the resist strip using Mattson's ICP stripper, the via test wafers were further processed at IBM's Advanced Semiconductor Technology Center and tested. Via contact resistance was one of the electrical parameters that was evaluated, since it is an indicator of the effectiveness of the polymer/residue removal process. On each wafer about 20 chips were tested. Contact resistance of a single via (0.25 μm ground rule) per chip was measured using a Kelvin Probe. These measurements were performed on all 8 via test wafers.

## Results and Discussion

Extremely low leakage currents were measured on both charge damage test wafers. The average leakage current for all the plasma damage wafers tested was 0.00047 nanoamp. No difference was observed between the two ICP processes. These damage results correlate well with many other plasma-damage-indicating tests performed for ICP processes (i.e., CHARM-2, C-V, $V_b$, SIMS).

Figure 3 shows a SEM cross-section of a quarter micron tapered via after the polymerizing RIE etch. The tapered profile [needed for a voidless metal fill] is obtained by side-wall passivation generated by $CF_4/CHF_3$ polymerizing chemistry. This tapered via profile though good from the process integration point of view, makes the job of residue clean even more difficult. The side-wall polymers consist of silicon dioxide residues deposited during the etch, and possibly Titanium Nitride sputtered on the walls during the over-etch.

Cleaning these residues is a major challenge faced by the resist strip community. We have demonstrated here an ICP based strip tool capable of residue-free resist strip, requiring only a de-ionized water rinse as the post wet processing step. Figure 4 shows an SEM cross-section of the via after resist strip and residue clean using Aspen ICP process. The tapered via and contacts seems to be free of any polymeric residues. No residues are seen on the top surface. Although good SEM results do not guarantee good contact resistance results, in this case, the contact resistances measured for all chip fields on all 8 test wafers were well within specification. Figure 5 shows the contact resistance data for all the wafers that was used in this study. On the x-axis the wafer identification number is given and the y-axis shows the contact resistance of the corresponding wafer. The ICP-treated wafers are enclosed by a square. No difference was observed in contact resistance between the $O_2$-only and $O_2/CF_4$ processes, indicating that the high density of radical oxygen generated by the ICP is sufficient to remove all residues.

Some of the via wafers processed on other non-ICP strippers showed high values in contact resistance. It is believed that high fluorinated chemistries (>4% $CF_4$) used on these wafers for adequate polymer

removal was responsible for out of spec contact resistance. Figure 6 shows a SEM cross section of a tapered via processed on such a non-ICP strip tool. The chip site that showed high contact resistance values was chosen for SEM cross-section. The purpose was to investigate the reason for high via contact resistance and to determine the influence of resist strip chemistry on contact resistance. Degradation of the underlying metal caused by high amounts of $CF_4$ during resist stripping can be seen in this figure.

## Conclusion

All-dry via etch residue clean processes with negligible plasma damage have been demonstrated using a novel ICP source technology. Contact resistance measurements show that both $O_2$-only and $O_2$/1%$CF_4$ processes developed at Mattson were effective in making the etch residues/polymers soluble and effecting their subsequent removal using only de-ionized water as the post-strip clean treatment. Antenna test structures show very low leakage currents and all contact resistance measurements are within specification. It is believed that the fundamental design of the ICP results in low ion bombardment of the wafer and a high density of dissociated radicals for effective residue removal.

**Tapered Via Cross-section after RIE Etch**

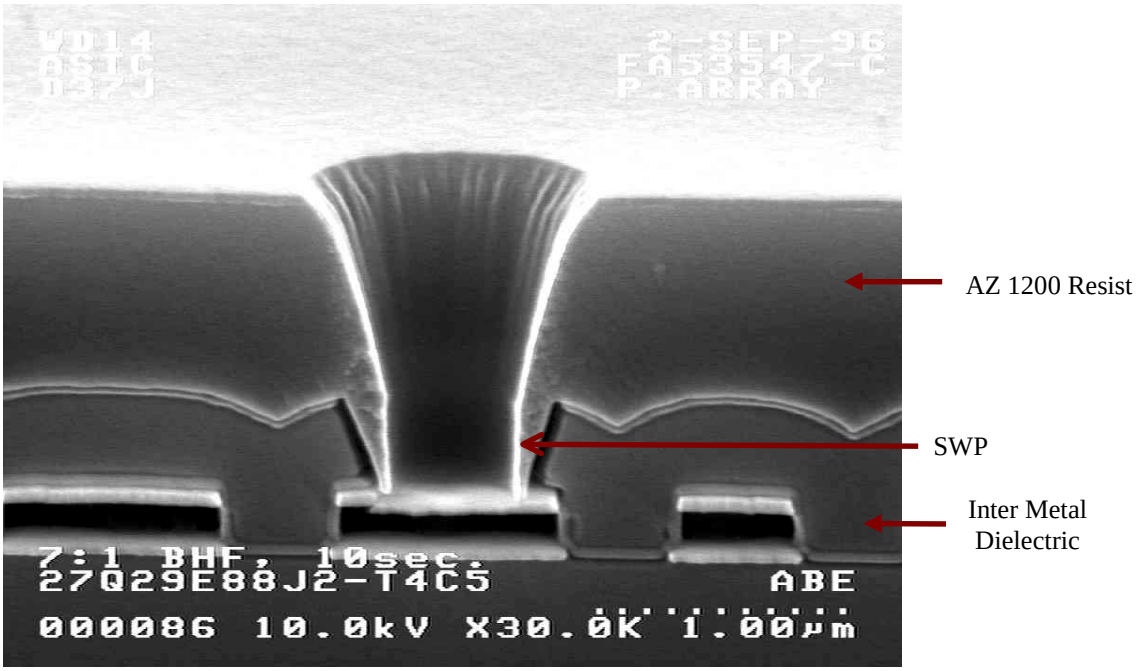



***Figure 3***. *SEM cross-section of tapered via [quarter micron ground rule] after RIE etch. The polymerizing RIE chemistry gives rise to side wall polymers that is a major strip issue.*

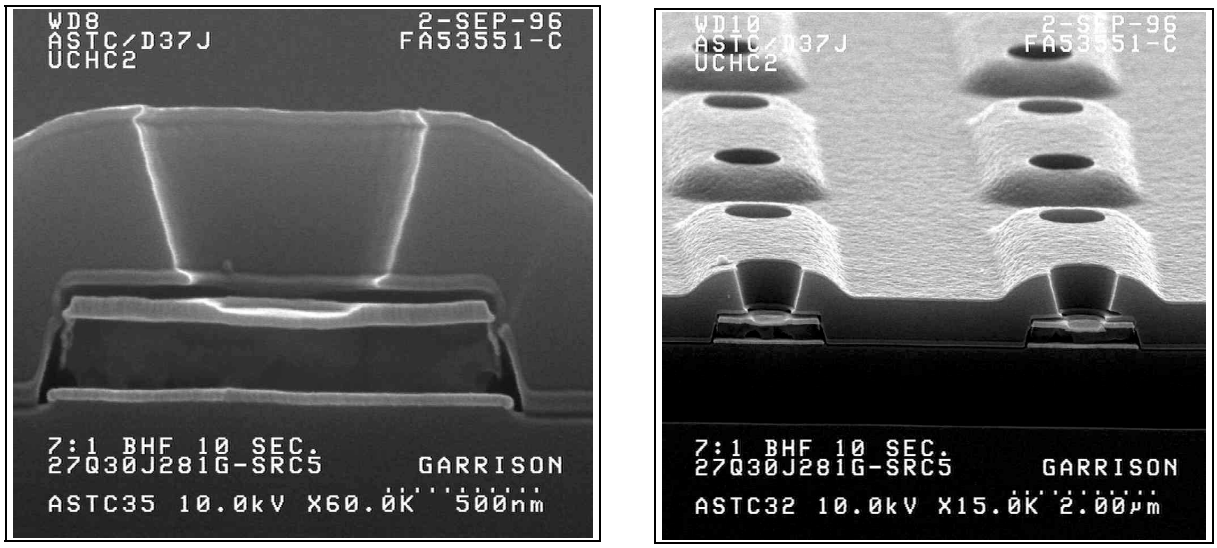



***Figure 4***. *SEM cross-section of tapered via [quarter micron ground rule] after resist strip using Aspen ICP process. The side walls and top surface are seen to be free of any polymeric residues.*

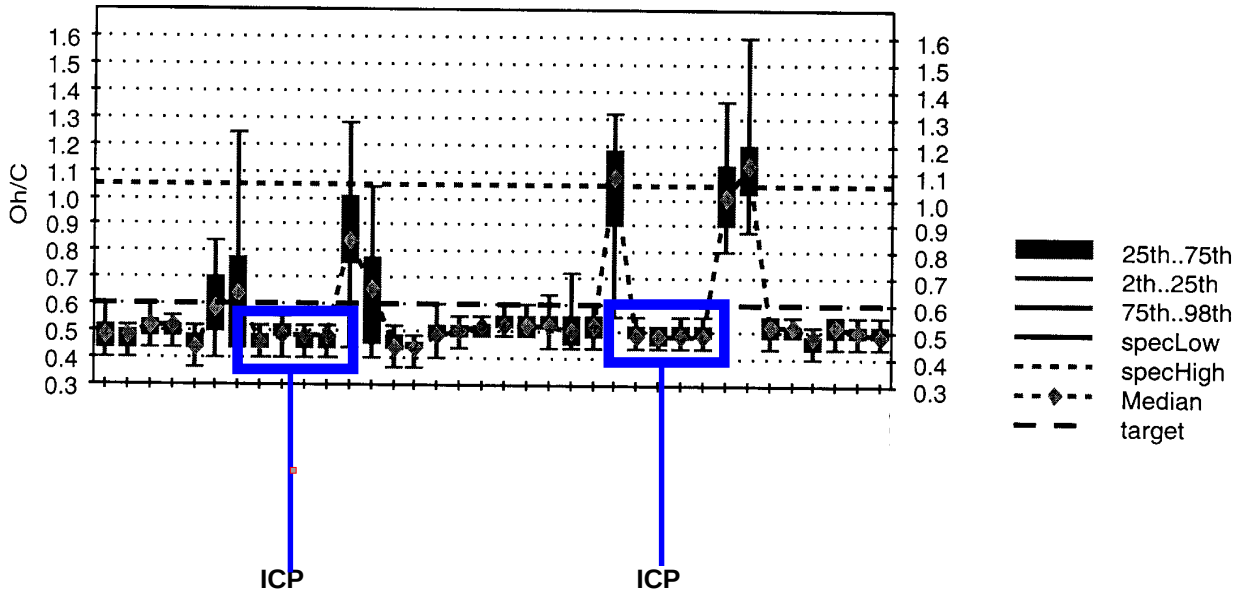
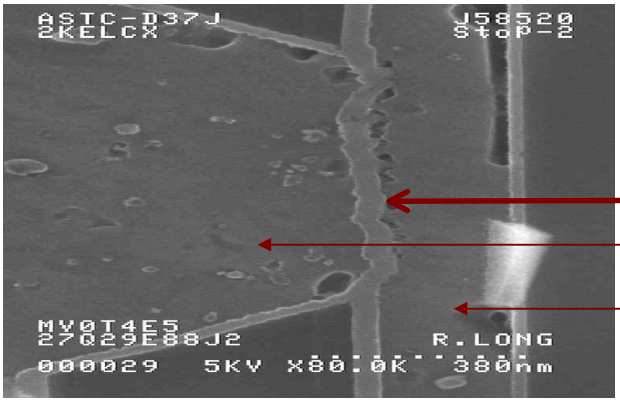



***Figure 5***. *Via Contact Resistance. Data for wafers processed using Mattson's ICP source are enclosed in boxes. The contact resistance values of these wafers have a narrow distribution and are well within the specifications. Notice some high fliers in contact resistance for wafers processed on other resist strip tools.*




Via filled with Metal

Metal Line

High contact resistance due to undercutting of TiN that exposes the Al layer underneath, forming TiF, $AlF/Al_2O_3$ .

Degradation of via metal interface during stripping possibly due to high fluorinated chemistry and/or high neutrals density in plasma.

***Figure 6. SEM cross section of via metal interface after third level metallization.***

## References

[1] S. Wilson, C. Tracy, J. Freeman, *Handbook of Multilevel Metallization for Integrated Circuits*, Noyes, NJ, 1993, p. 564-565.

[2] S. Savas, "Advanced Photoresist Strip with a High Pressure ICP Source", *Solid State Technology*, Vol. 39, No. 10, pp. 123-128 (1996).