HF/UHF SMD TCVCXO
OK-XA3XXXX-X Series

Description

The **OK-XA3XXXX Series** of SMD temperature compensated, voltage controlled crystal oscillators (TCVCXO) provides High and Ultra High Frequency with excellent temperature stability, extremely low phase noise and jitter with variety of different output types in a small surface mount FR4 based package.

Applications and Features

- Ultra High Frequency - up to 1GHz
- Small, Low Profile SMD Package
- Very Low Phase Jitter and Phase Noise
- Excellent Frequency Stability
- CMOS, Sine-wave, Differential PECL or LVDS outputs available
- Stratum 3 available
- COTS/Dual use

Creating a Part Number

OK - X A3 X X X X - X FREQ

Package Code
OK 7 pad 25x22x7mm SMD

Input Voltage
0 5.0V±5%
A 3.3V±5%

TCXO/TCVCXO Option
T No V. Control
V With V Control

Output Type
C CMOS
P PECL
S Sine-wave
L LVDS

Temp Frequency Stability, ppm
1 ±1.0
2 ±2.5
3 ±0.28
9 Customer Specific

Temperature Range, °C
B 0 to 70
C -20 to 70
D -40 to 85
E -10 to 60
9 Customer specific

Environmental
L Contains a level of lead that is in excess of RoHS directive and is not designed for reflow
R RoHS compliant

NEL FREQUENCY CONTROLS, INC.
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OK-XA3XXXX-X Series Continued
HF/UHF SMD TCVCXO

Rev. L

Absolute Maximum Ratings

Parameter	Sym	Condition	Min	Typ	Max	Unit	Note
Input Break Down Voltage	Vcc		-0.5		5.5	V	
Storage Temperature	Ts		-40		105	ºC	
Control Voltage	Vc		-1		9	V	

Electrical Parameters (1)

Parameter	Sym	Conditions	MIN	TYP	MAX	Unit	Note
Frequency Range	F	CMOS Sine-wave PECL,LVDS	30 30 30		200 1,000 1,000	MHz	
Input Voltage	Vcc	Code 0 Code A	4.75 3.135	5.0 3.3	5.25 3.465	V	
Input current	Icc	CMOS,Sine PECL, Sine,LVDS			30 100	mA	@100MHz, 3.3V @622MHz, 3.3V
Frequency Stability	ΔF/F	Overall, available			±4.6		20 years
Frequency Stability	ΔF/F	vs Temperature vs Vcc Aging		±0.5 ±0.1 ±1 ±3.5	±1	ppm ppm/V ppm/year ppm	See Chart First Year 10 years
Calibration	ΔF/F	As shipped, 25°C		±0.5	±1	ppm	
Load		CMOS Sinewave PECL LVDS	15pf/10KOhmOhm Internally AC-coupled 50 Ohm 50 Ohm to Vcc-2V or Thevenin equivalent 100 Ohm between the outputs, receiving end				
Duty Cycle		At 50 %	45/55	50/50	55/45	%	CMOS, PECL, LVDS
Rise/Fall Time	Tr/Tf	20 to 80%		3 0.35		ns	CMOS PECL, LVDS
Logic "1" level	Voh	CMOS	0.9Vcc			V	
Logic "0" level	Vol	CMOS			0.1Vcc	V	
Logic "1" level	Voh	PECL	Vcc-0.96		Vcc-0.81	V	100K available
Logic "0" level	Vol	PECL	Vcc-1.85		Vcc-1.65	V	100K available
Output Levels LVDS	Vod	Differential amplitude	247	330	454	mV	
		Amplitude error			50	mV	
	Vof	Offset Voltage	1.125	1.25	1.375	V	
		Offset Voltage error			50	mV	
Output power	P	Sinewave Into 50 Ohm </=400MHz	0 4	3 7		dBm	3.3V 5.0V
		Sinewave Into 50 ohm >400MHz	-5 0	0 5	5		3.3V 5.0V
Start up Time	Ts			2	10	ms	
Phase jitter		1 sigma		0.4 0.2	1 0.4	ps	100Hz to 20MHz 12kHz to 20MHz
Sub-harmonics		PECL, LVDS, Sine CMOS, Sine		-45	-40 none	dBc	F>250MHz F<250MHz
Spurious					-60	dBc	
Harmonics		Sine-wave		-30	-25	dBc	
SSB Phase Noise		@10 Hz @100 Hz @1 KHz @10KHz @100KHz		-80 -110 -140 -155 -160		dBc/Hz	@ 100 MHz
SSB Phase Noise		@10 Hz @100 Hz @1 KHz @10KHz @100KHz		-60/-60 -90/-90 -120/-120 -140/-145 -145/-150		dBc/Hz	@ 622 Mhz; PECL,LVDS/Sine
Input Impedance			> 10 K Ohm				
Control Voltage	Vc		0		3.3	V	for 3.3V supply
			0		5.0	V	for 5.0V supply
Modulation Bandwidth	MB		2Hz				Contact Factory for wider MB
Deviation		Vc=0V to 3.3V, 25°C	±5	±7		ppm	

Note 1. All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal Load.

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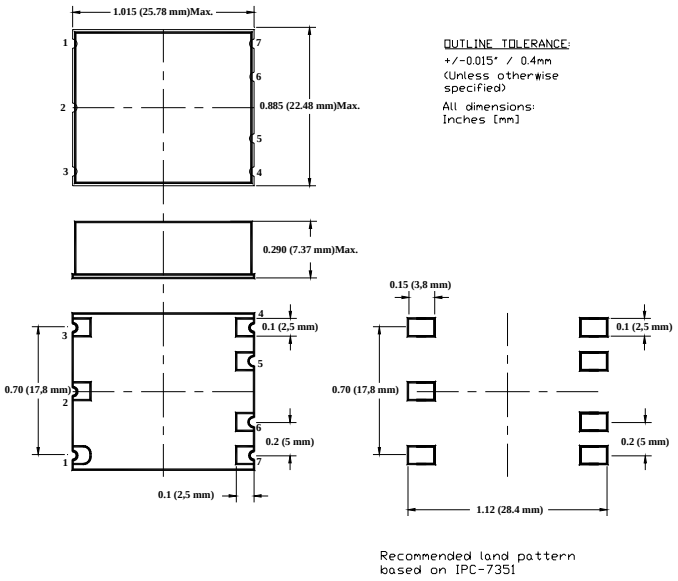
Electrical Connection

Pin	Connection
1	Voltage Control
2	NC
3	V_{CC}
4	Output, CMOS or Sine
5	Output, PECL/LVDS
6	Comp. Output, PECL/LVDS
7	Gnd

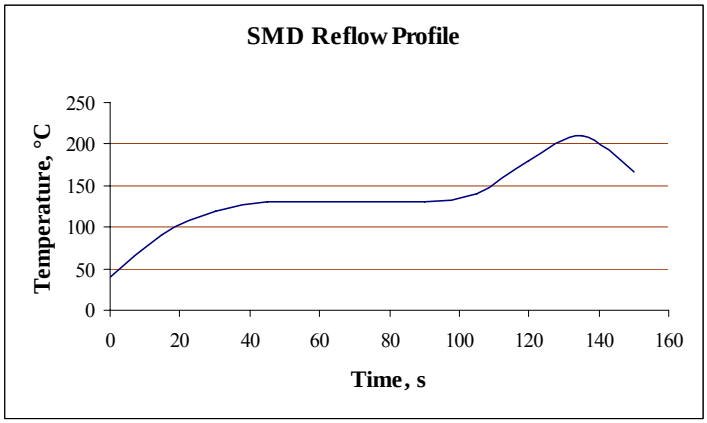
Note: For frequency stability over temperature ±1ppm and tighter, the package height may be 10mm or 12.5mm.



Environmental and Mechanical Characteristics

Operating temp. range	0°C to 70°C, -40°C to 85°C, see chart page 1
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. E
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than $1x10^{-8}$ atm.cc/s of helium (crystal only)
Soldering conditions	See MAX reflow profile below; The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.

Maximum Reflow Profile



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