NEL CRYSTAL CLOCK OSCILLATORS

Application Note for Complimentary (Differential) Output ECL (PECL) With Enable/Disable Feature

It is important to know that the nature of a differential pair is to have one signal to be the logical opposite (compliment) of the other signal in the pair. Thus when one signal is at a logic low the other signal is at a logic high.

The internal transistor structure of the ECL (PECL) gate is created so that the output transistor is configured in an open emitter format. Thus, when the gate output is in the logic high state, the output transistor is turned on and pulls up the output towards Vcc. When the output is in a logic low state, the output transistor is not turned on (transistor is off) and the signal is pulled down towards Vee by the external bias required to make ECL device operate properly.

When the two concepts above come together in an enable/disable complimentary (differential) output ECL (PECL) oscillator, the result is a disabled output pair that has one output at a logic high (connected through the internal resistance of the device to Vcc) and the other output is in a logic low state (the output transistor is off). Since most enable/disable outputs are used for automatic test equipment to inject a test signal into the circuit under test, the goal would be to have an open connection to the output signal in all cases. Since, in the case of the complimentary (differential) outputs, one of the outputs is at a logic high state, injecting a differential signal is not possible without over driving the output transistor. This is only true for the complimentary (differential) ECL (PECL) since with a single ended output, the proper condition can be selected to give the correct output state when the unit is disabled.

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