Using Large-Signal Measurements for Transistor Characterization and Model Verification in a Device Modeling Program

Maciej Myśliński[1], Giovanni Crupi[2], Marc Vanden Bossche[3], Dominique Schreurs[1], and Bart Nauwelaers[1]

[1] Katholieke Universiteit Leuven, Belgium,
[2] University of Messina, Italy,
[3] NMDG N.V., Belgium.

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Outline

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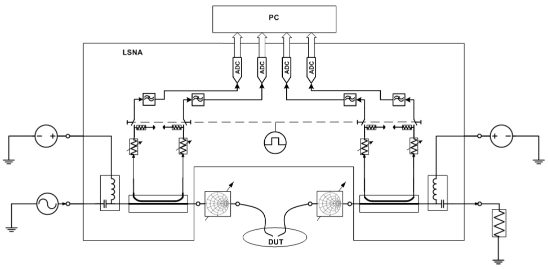
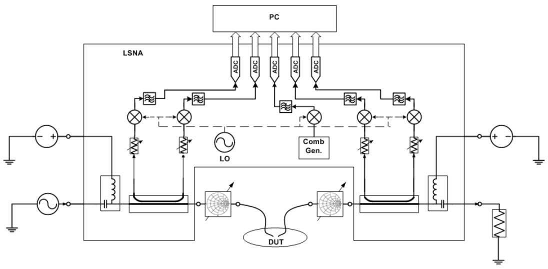
- Introduction
- Large-signal measurement data in a device modeling program
  - Example: IC-CAP
- Transistor characterization
  - Example: MOSFET
- Model verification
  - Example: Angelov model
- Results
- Conclusions

Introduction

- Large-signal network analyzer (LSNA)
  - Amplitude and phase of all harmonics and intermods up to 50 GHz
  - Realistic signals: 1-tone, 2-tone, N-tone up to +40 dBm
    - DC, small-signal, large-signal behavior
  - Non-50 Ω environment
  - Sampler/Mixer-based

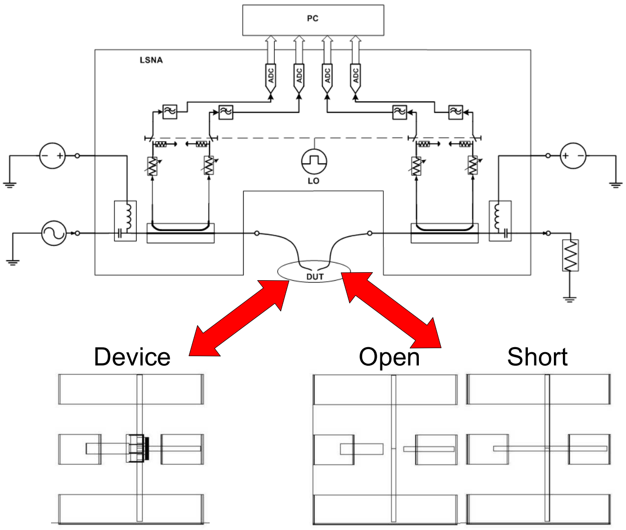




LSNA provides accurate complex values of the incident and scattered traveling voltage waves present at the ports of a 2-port DUT. Harmonic frequency components and intermodulation distortion products are measured in a wide frequency band, even up to 50 GHz.
The measured data give complete information about the behavior of the DUT under realistic signal conditions. The accepted excitations include: one-tone CW signal, two-tone signal, multi-tone signals (periodically modulated signals) with the input powers reaching +40 dBm.
With a single connection of the DUT DC, small- and large-signal behavior can be measured.
LSNA systems are adapted to work in non-50 Ohm environment (see impedance tuners at the input and output of the DUT).
There are sampler and mixer-based LSNA setups (see the diagrams). In the sampler-based solution, all the frequency components are obtained during one measurements cycle. The data are available faster but the dynamic range is lower than in the second type of systems. In the mixer-based solution, the frequency is swept over the required range and a number of measurements is taken each at different frequency.

LSNA data in IC-CAP

- Large-signal on-wafer measurements
  - Device:
    - Frequency sweep
    - RF power sweep
    - DC bias sweep
  - De-embedding structures:
    - Frequency sweep



Here, we give an outline of the procedure implementing large-signal measurements in the device modeling program, using as an example Agilent's IC-CAP.

1. Perform the LSNA measurements of the on-wafer DUTs:
a) In case of a transistor, we usually sweep the parameters like the fundamental frequency of the CW signal, the RF input power level, and the DC bias conditions.
b) In case the de-embedding structures are available (usually open and short dummy structures), only the S-parameter measurements are necessary at the harmonic frequency grid.

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LSNA data in IC-CAP

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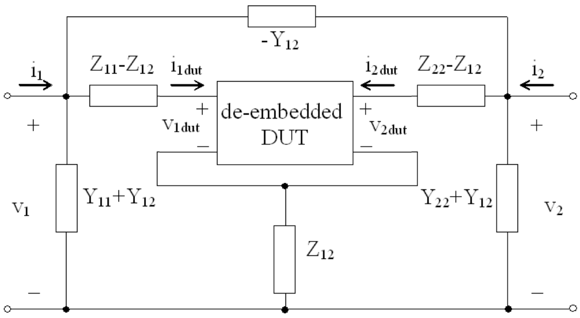
- Large-signal on-wafer measurements
- Data processing
  - De-embedding
  - Transformation to the program specific format



Y_{ij} → Y-parameters of open

Z_{ij} → Z-parameters of short, after de-embedding of open effects.

MDM files

$$i_{1dut} = i_1 - v_1(Y_{11} + Y_{12}) - (v_2 - v_1)Y_{12} = i_1 - v_1Y_{11} - v_2Y_{12}$$

$$i_{2dut} = i_2 - v_2(Y_{22} + Y_{12}) - (v_1 - v_2)Y_{12} = i_2 - v_2Y_{22} - v_1Y_{12}$$

$$v_{1dut} = v_1 - i_{1dut}Z_{11} - i_{2dut}Z_{12}$$

$$v_{2dut} = v_2 - i_{2dut}Z_{22} - i_{1dut}Z_{12}$$

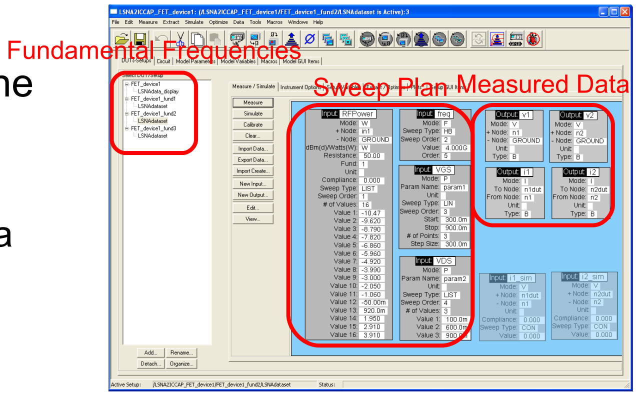
2. The next step of the procedure involves the measured data processing:

a) De-embedding is performed to remove form the large-signal current and voltage spectra the parasitic effects of contact pads and signal path between the probe tips and the device itself. A possible equivalent circuit representation of these parasitics is shown in the figure. The parallel parasitic admittances, mostly due to the contact pads, are identified from the small-signal measurements of the open dummy structure. The impedances of the presented equivalent circuit are obtained from the measured short dummy structure after de-embedding contact pads effects. Finally, the admittances and impedances are de-embedded from the large-signal currents and voltages in frequency domain, as shown in the equations.

b) The resulting the data is converted to a format readable in the device modeling program. In case of IC-CAP, this is .MDM file format.

LSNA data in IC-CAP

- Large-signal on-wafer measurements
- Data processing
- Implementation in the device modeling program
  - Measured data



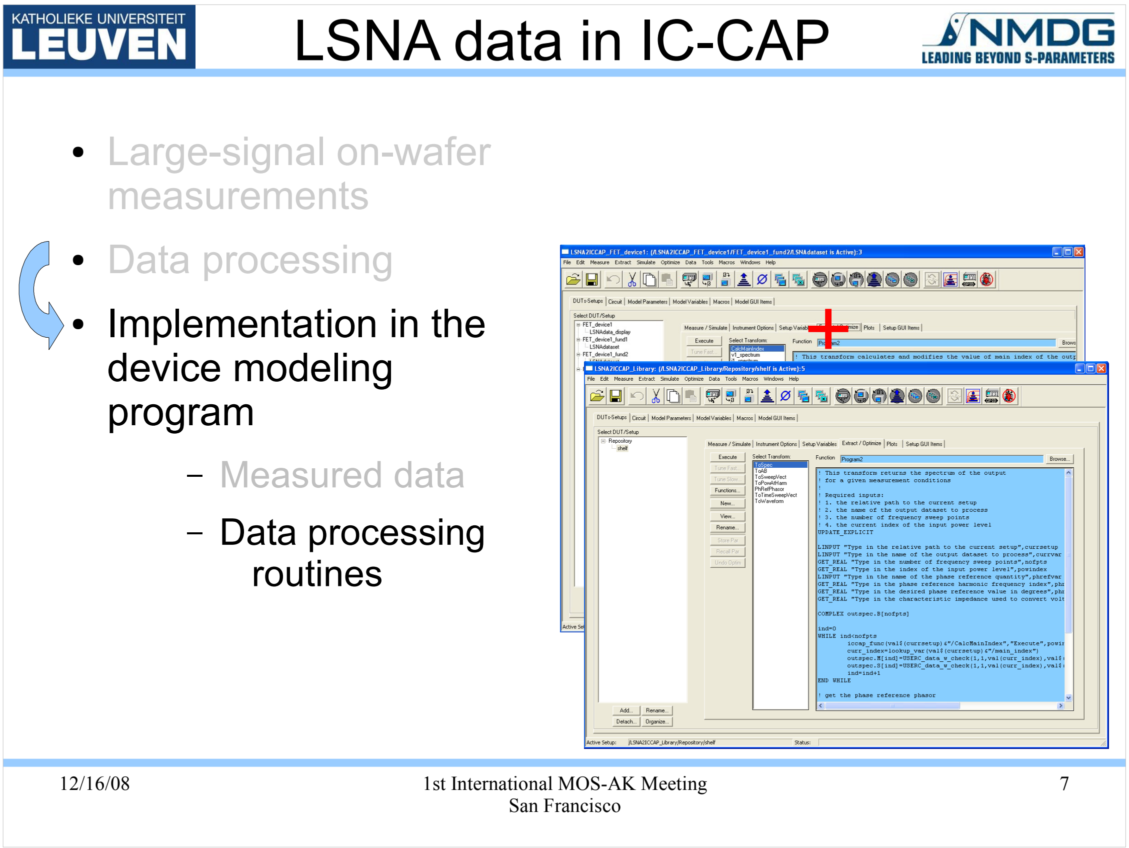
3. Finally, the large-signal data can be implemented in the device modeling software.

a) The (de-embedded) measurements are imported to the environment. In IC-CAP, we can see the sweep parameters as the inputs and the measurements as the inputs. On the presented figure two inputs are grayed out, because they are added to properly store simulated currents later on.

b) For the maximum usability of the measured data, the latter is accompanied by a set of data processing routines located in two files. One file is the same as of the measured data and it contains higher level procedures. Whereas, the second one serves as a library of the lower level functions doing the actual 'job'.

c) To properly assess the accuracy of a model, the LSNA data must be used during the simulations under the same conditions as these of the measurements. Therefore, a link to ADS harmonic balance simulator is established. There are also some external files needed, containing the measurements in a CITI format. This is due to the fact, that IC-CAP has problems working with simulator when the excitation is taken from the IC-CAP output variable.

d) All these data would be impractical without a graphic user interface straightforward in use. The plot shows the GUI in our case. At the top, it has a set of controls to select the measurements conditions of interest out of the loaded setup. Looking from left to right, the fundamental frequency drop down list, RF power slider and DC bias voltages sliders. Below, there are tabs selecting the domain of the plots displayed at the bottom of the window. User can choose among: V/I or A/B in frequency domain, both VI and AB in time domain, DC drain current, drain output power harmonics, and AM-AM AM-PM in power domain, as well as input, output and transfer locii as dynamic trajectories.



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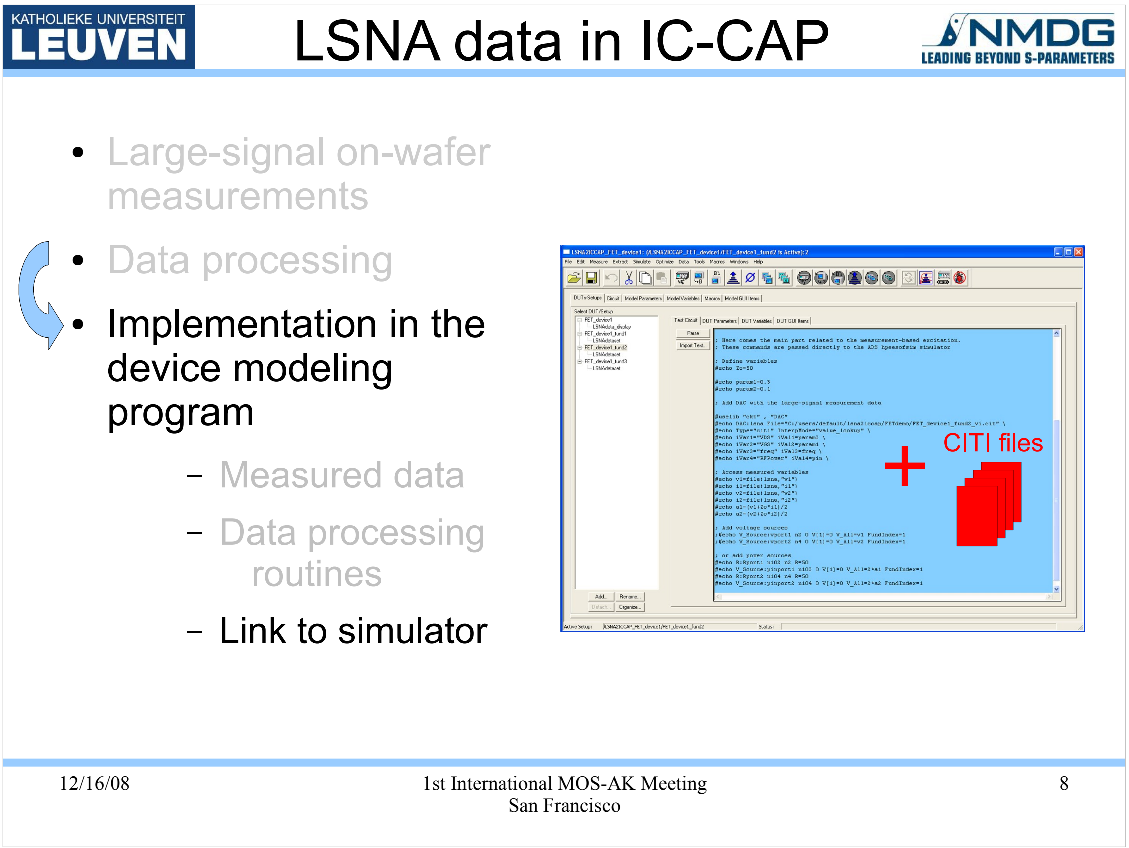

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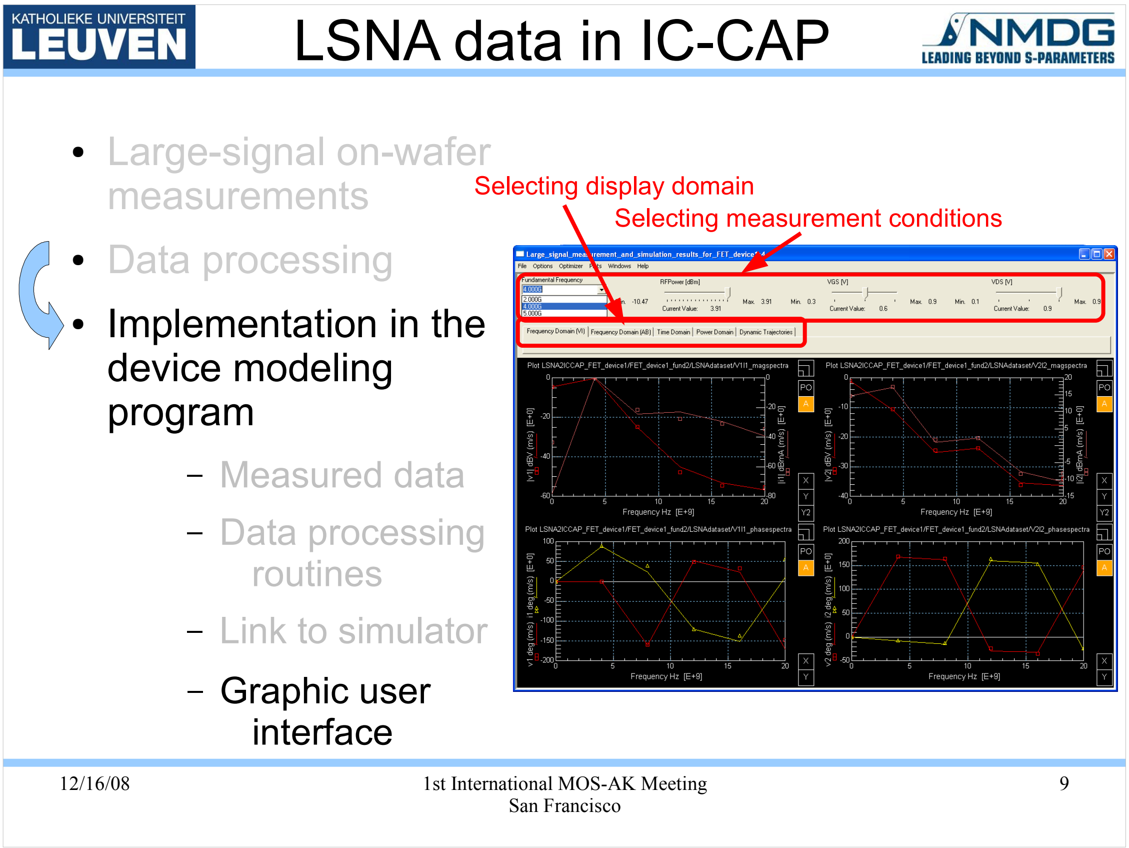

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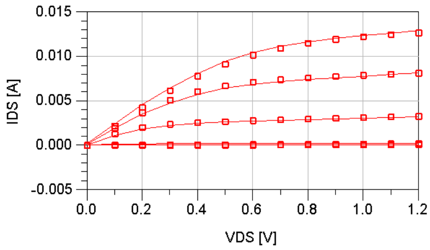
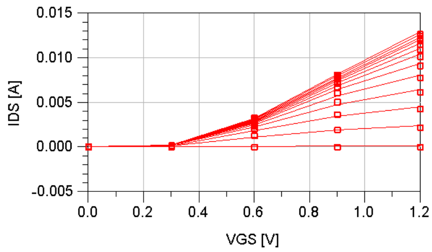
Transistor Characterization

- On-wafer DUT:
  - MOSFET
  - Open & Short de-embedding structures
- LSNA measurements:
  - f_0: 2, 4, 5 GHz
  - P_{in}: -10 → +4 dBm
  - V_{GS}: 0.3, 0.6, 0.9 V
  - V_{DS}: 0.1, 0.6, 0.9 V

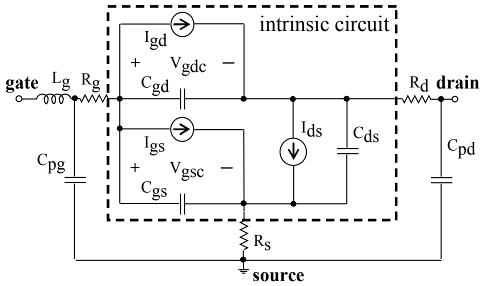




The described procedure was applied in the characterization of an on-wafer MOSFET device. The DC characteristic of this device are shown on the plots (squares – measurements, lines simulations with Angelov model).
For the de-embedding, we measured open and short dummy structures located on the same wafer and having the same contact pads layout.
The LSNA measurements were performed on the MOSFET under the reported conditions.

Model verification

- Angelov MOSFET model:
  - Neglected self-heating and intrinsic non quasi static effects,
  - Capacitance mode,
  - Extracted from DC and S-parameter measurements
  - Tuned around: V_{GS}=0.6 V, V_{DS}=0.9 V, f_0=4 GHz

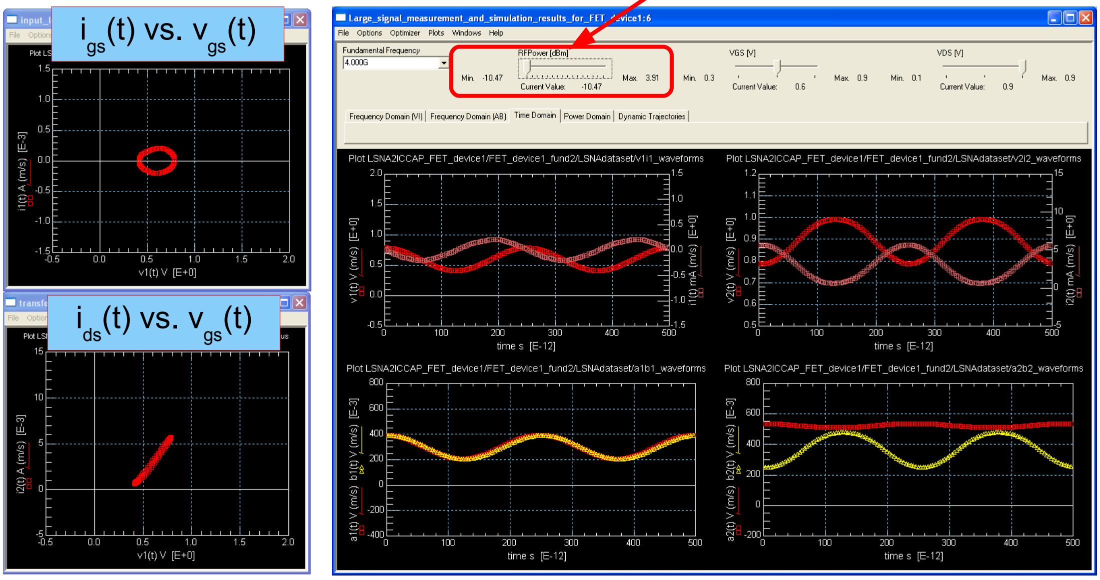


model AngelovM1 Angelov	B1=0	P31=0.54852	Rcmin=0kOhm
Idsmod=1	B2=3.92	P40=1.2	Rc=0kOhm
Igmod=1	Lsb0=0	P41=1.71519	Crf=35.3284fF
Capmod=1	Vtr=4	P111=0.001	Rcin=0kOhm
Ipk0=0.0066	Vsb2=0	Ij=0.0025	Crfin=0fF
Vpks=0.84	Cds=28.331fF	Pg=0.0002	Rth=50
Dvpks=0.027	Cgspi=2.6fF	Vjg=0.9	Cth=0
P1=2.5	Cgs0=5fF	Rg=22.4	Tcipk0=0
P2=0.1	Cgdpi=4.5446fF	Rd=10.7	Tcp1=0
P3=6.2	Cgd0=5.06055fF	Rs=11.2	Tccgs0=0
Alphar=2.5	Cgdpe=0fF	Ri=0	Tccgd0=0
Alphas=0.5	P10=1	Rgd=0	Tclsb0=0
Vkn=0.5	P11=1.71519	Lg=0pH	Tcrc=0
Lambda=0.1	P20=0.2	Ld=0	Tccrf=0
Lambda1=0.07	P21=0.54852	Ls=0	Tnom=25
Lvg=0	P30=0.25	Tau=0ps	

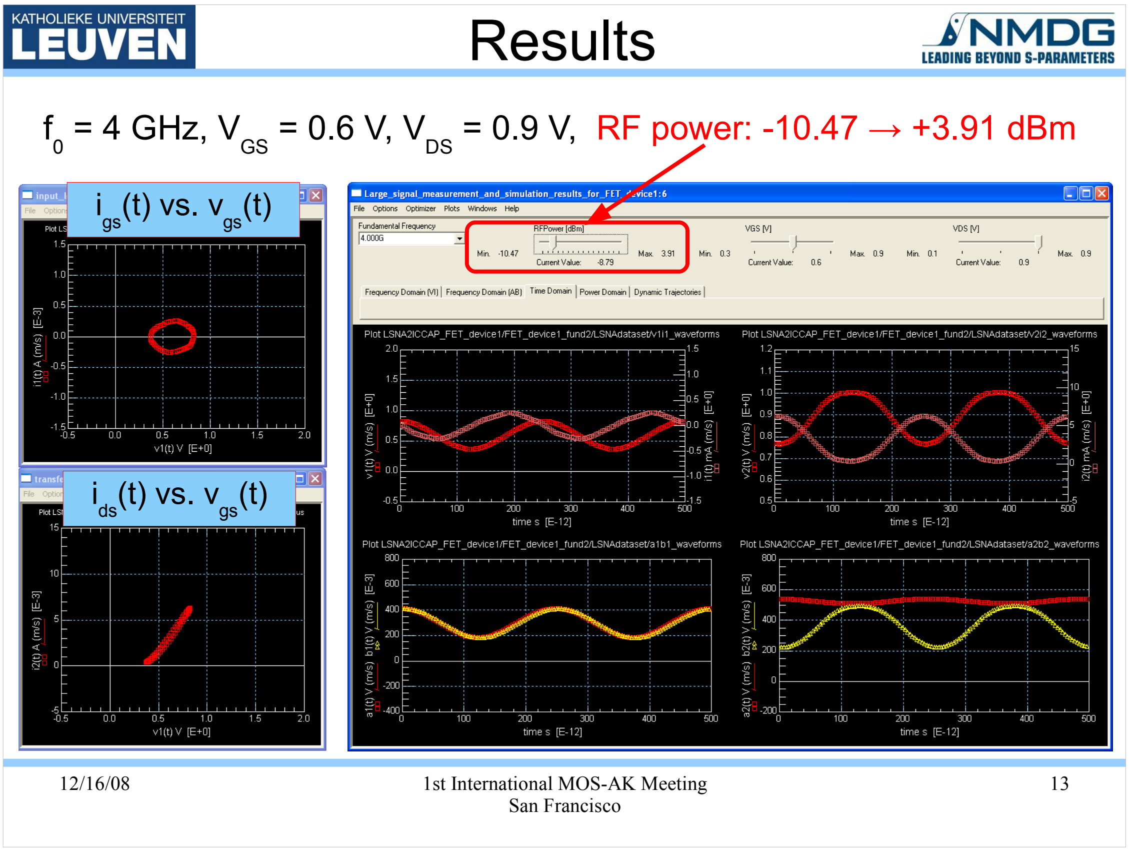
The measurements were applied to verify the accuracy of the Angelov model of the MOSFET device. Due to relatively low operating frequencies the model was simplified as shown on the equivalent circuit plot. The self-heating and intrinsic non quasi static effects were neglected and the capacitance instead of charge mode was used. The model was extracted from previously made DC and S-parameter measurements. The parameters were then tuned around a given bias point and fundamental frequency. The list of the resulting parameters is shown on the slide and it was implemented in IC-CAP.

Results

f_0 = 4 GHz, V_{GS} = 0.6 V, V_{DS} = 0.9 V, RF power: -10.47 → +3.91 dBm



The time domain results at these model tuning conditions are shown on the slide. We visualize the voltage and current (top) and incident and scattered (bottom) waveforms in port 1 (left) and 2 (right) of the transistor. The animation demonstrates the change in the measured waveforms due to the increasing RF input power level. At the same time, the separate plots on the left, depict the input (top) and transfer (bottom) locus dynamic trajectories for the considered signal conditions. In all figures, the symbols denote the measured, whereas the lines denote the simulated data. A very good match between predicted and measured traces can be observed, thanks to the model tuning.



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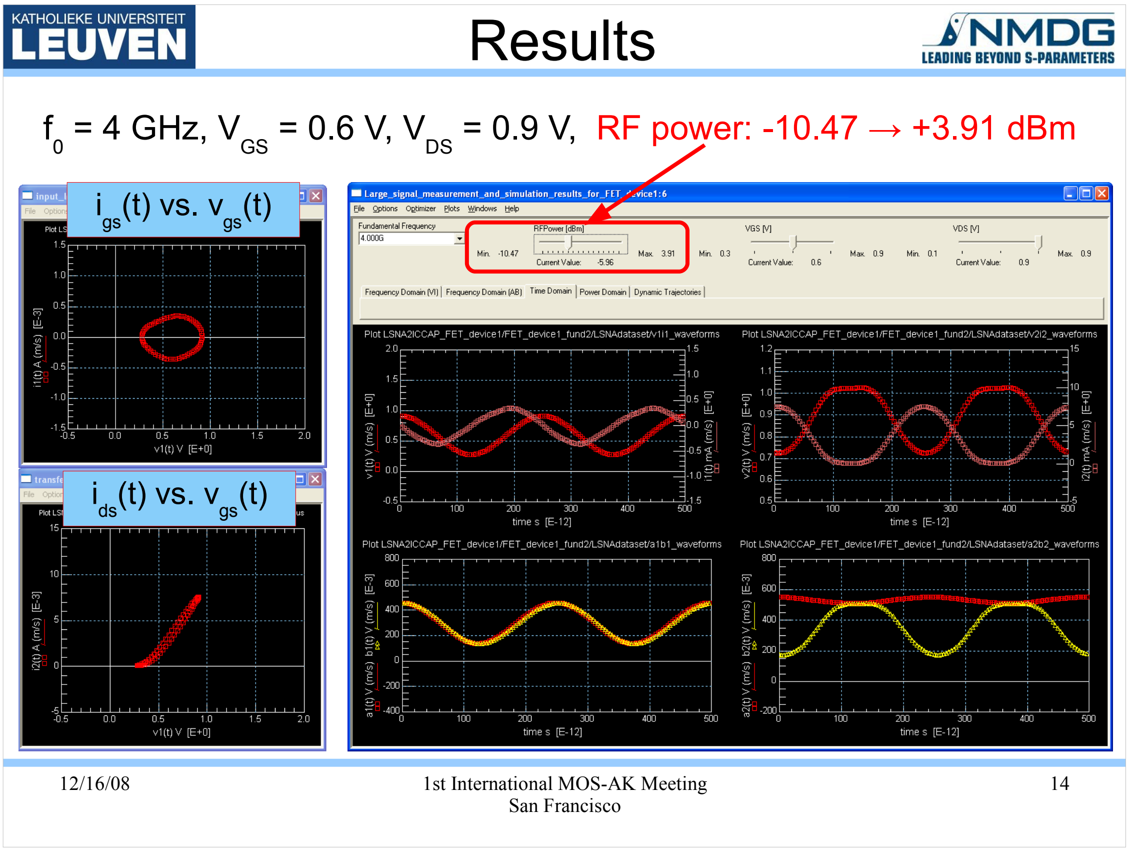

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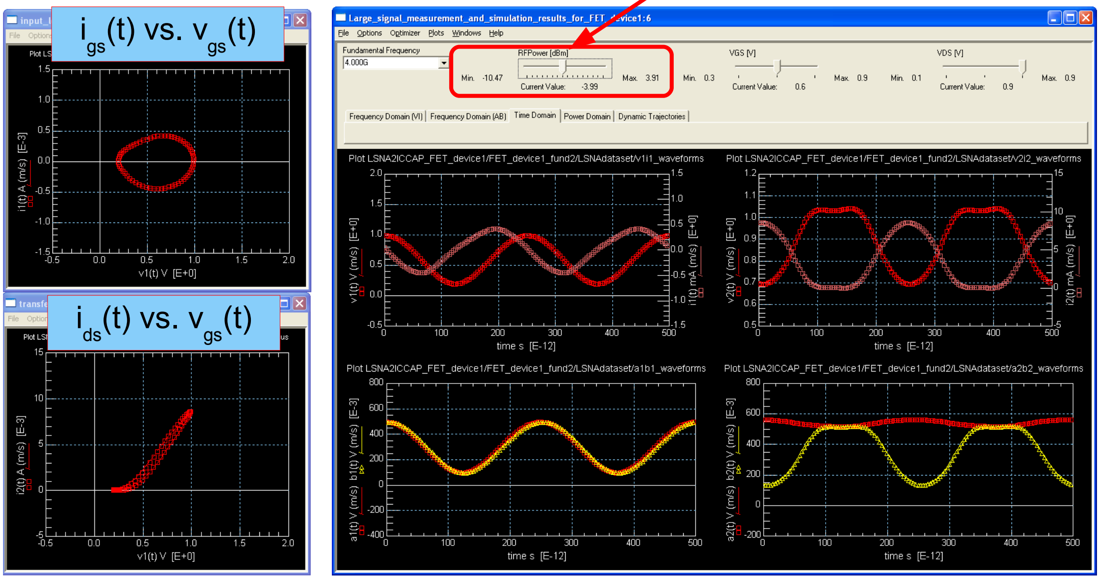

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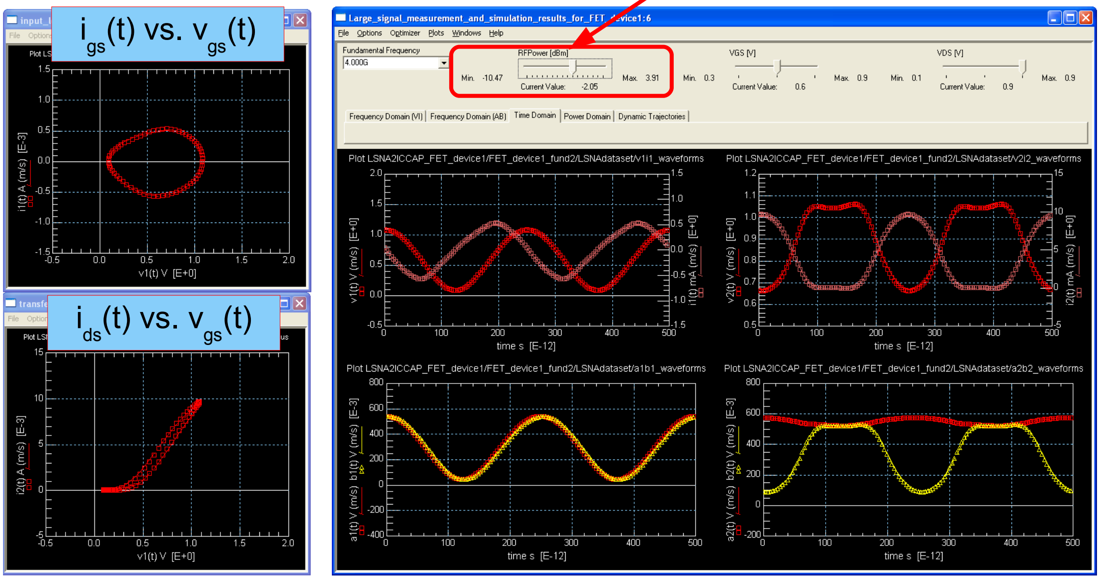

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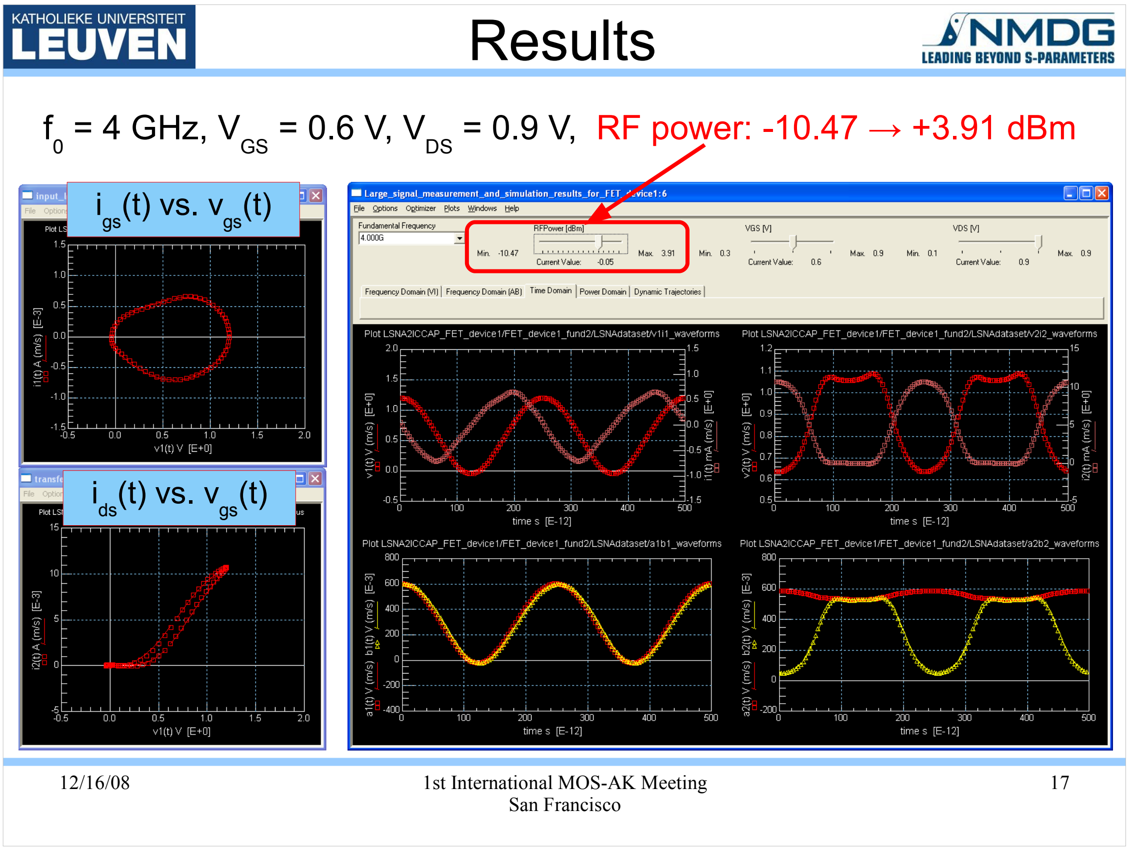

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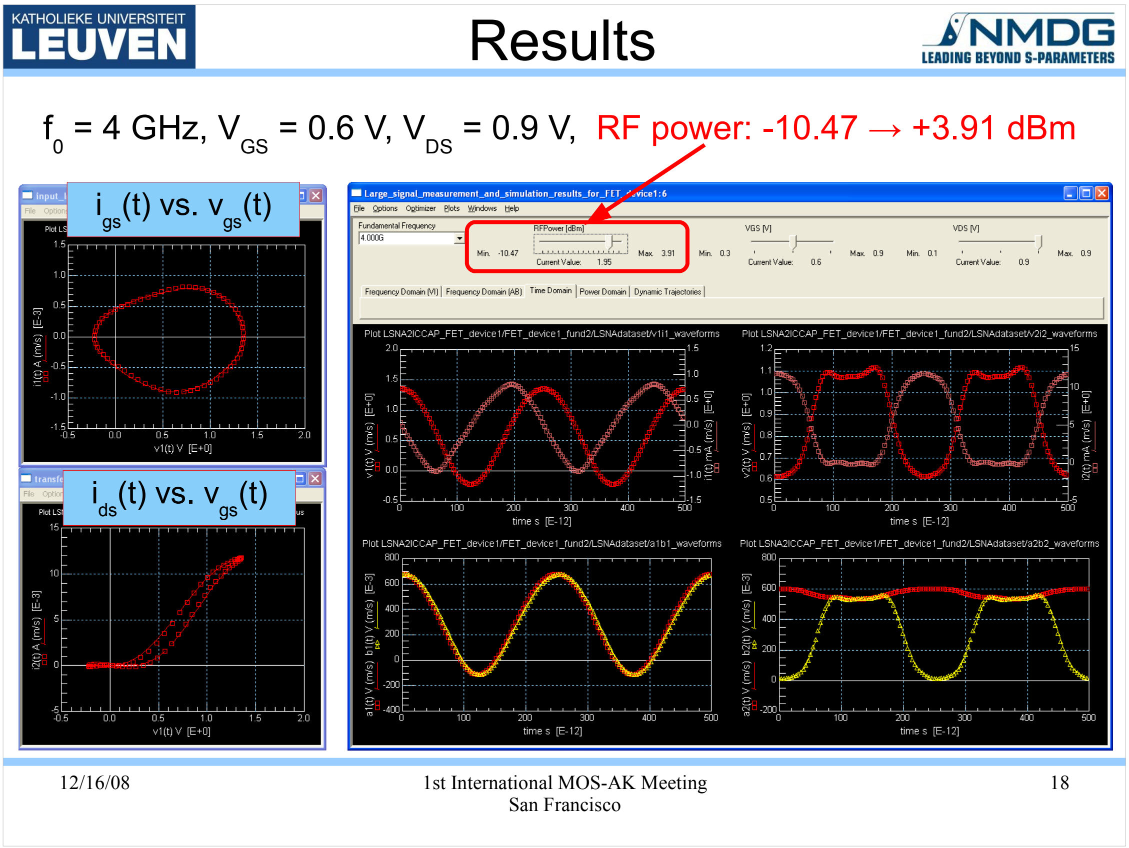

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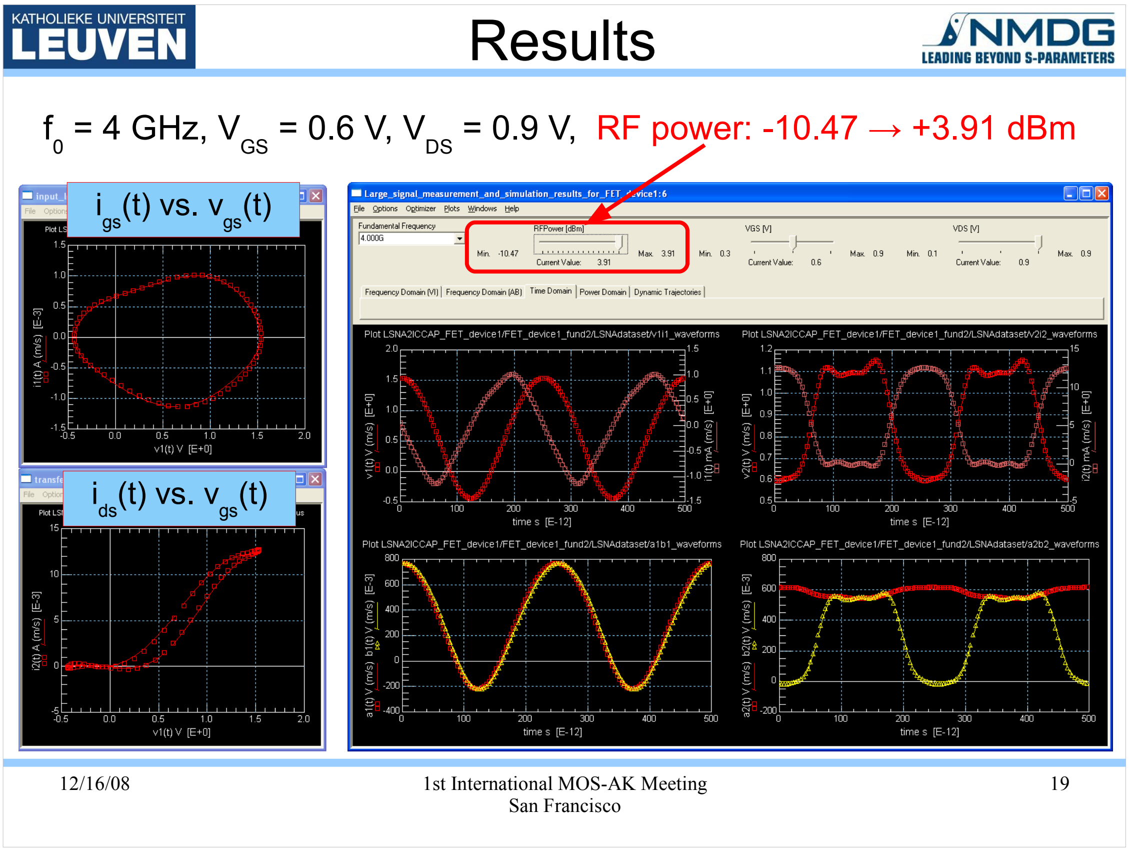

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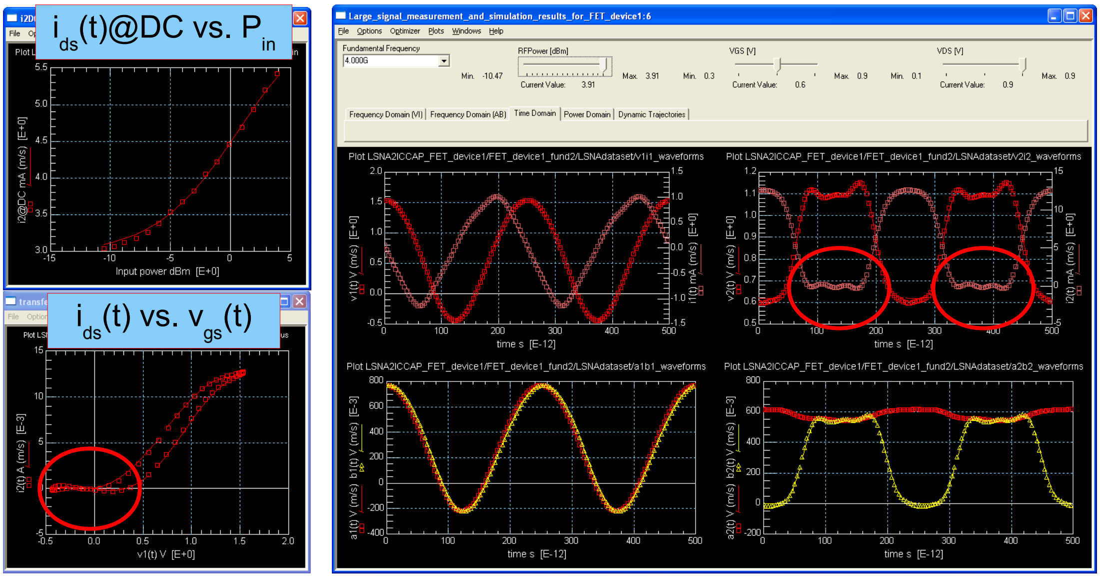
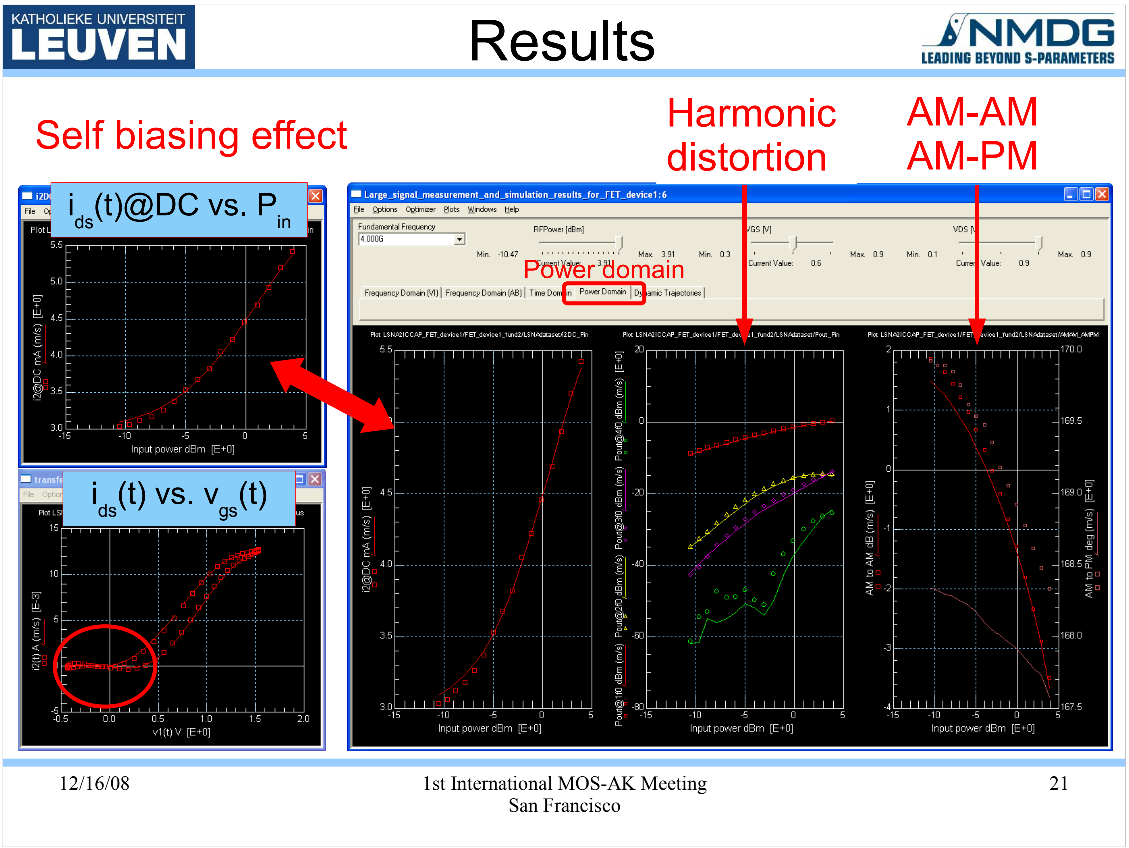
Self biasing effect



The clipping of the drain current around 0 mA observed both at the time domain and transfer locus plots is related with self biasing effect. This is evident on the next plot, where DC component of the drain current waveform is plotted as function of input power level. The main GUI window also contains this plot under 'Power domain' tab. The other two plots in this set allow observation of harmonic distortion of output signal power, and AM-AM AM-PM characteristics.



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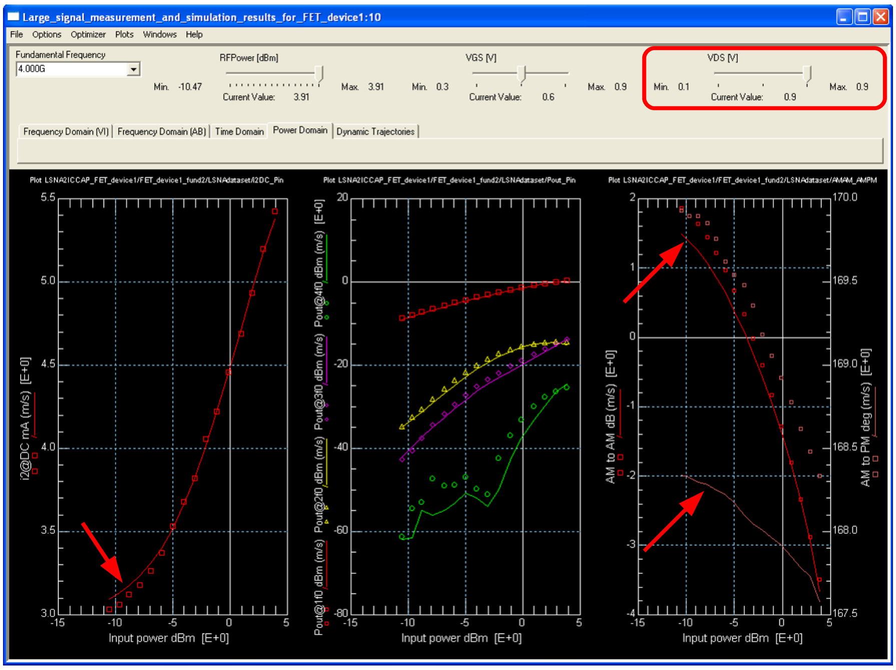

If we look more at the power domain plots, we can see that there are some discrepancies between measured and simulated data. Especially, at low input power levels, This is mainly due to a fact that the model was tuned at higher power levels. Note also that the simulated AM-PM characteristic seems to significantly differ from the measured one. In fact the difference is very small (see the scale of the plot) and it is within the phase measurement accuracy.
The power domain plots can be also used to test the performance of the model under other DC bias conditions. Therefore, we first sweep the drain DC voltage down to 0.1 V. The overall model's prediction is generally worse than before, but still the match at lower power levels is less accurate. Note that only due to the plot scale, the self biasing seems to be much worse than before.
Then we modify also the gate bias voltage and observer the curve traces.

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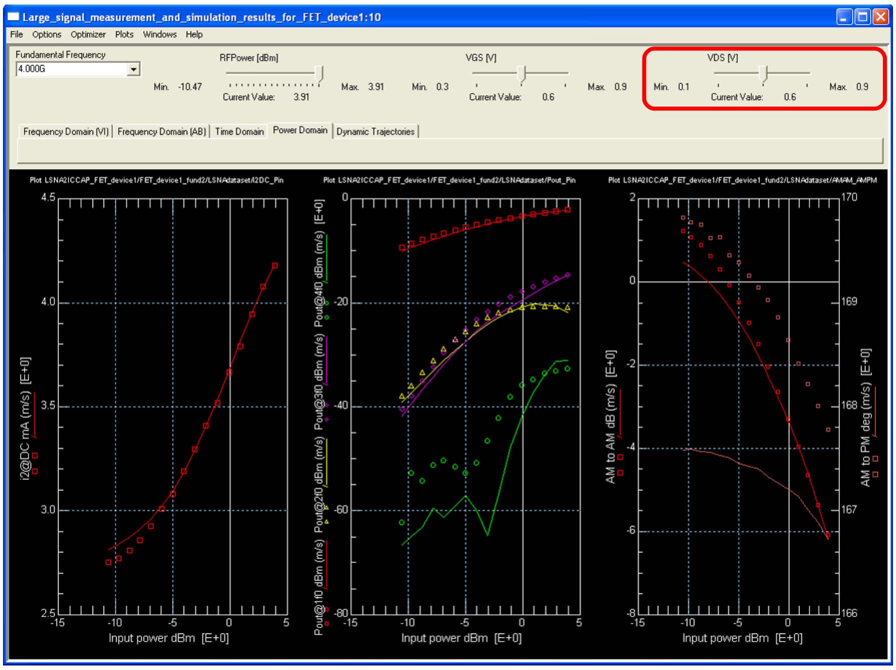

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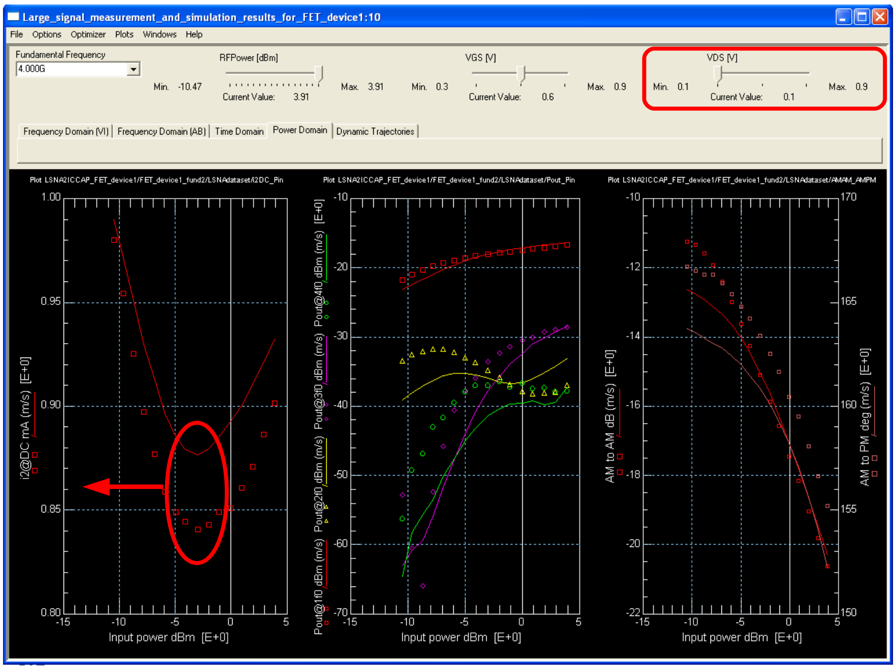

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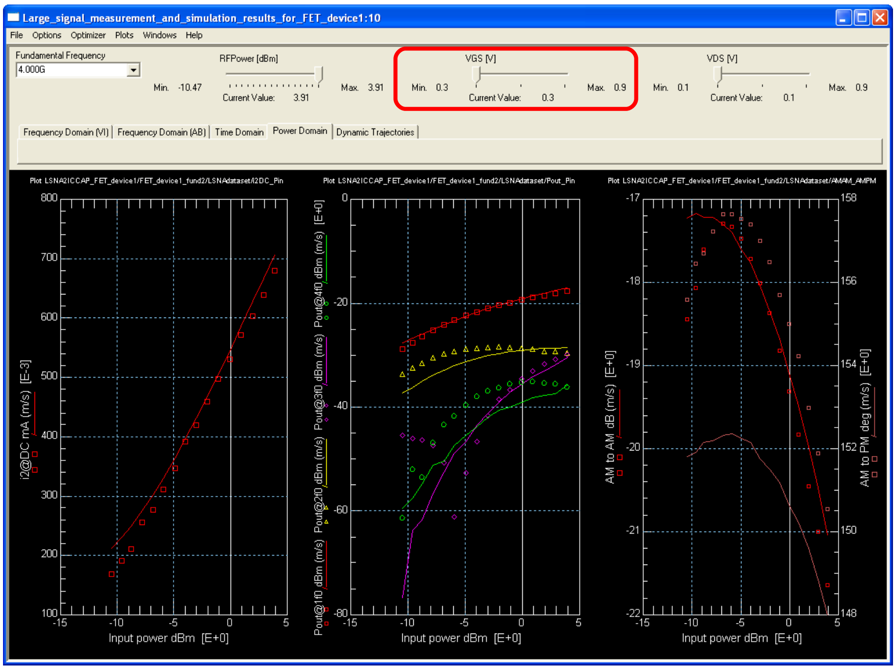
Then we modify also the gate bias voltage and observer the curve traces.

Results



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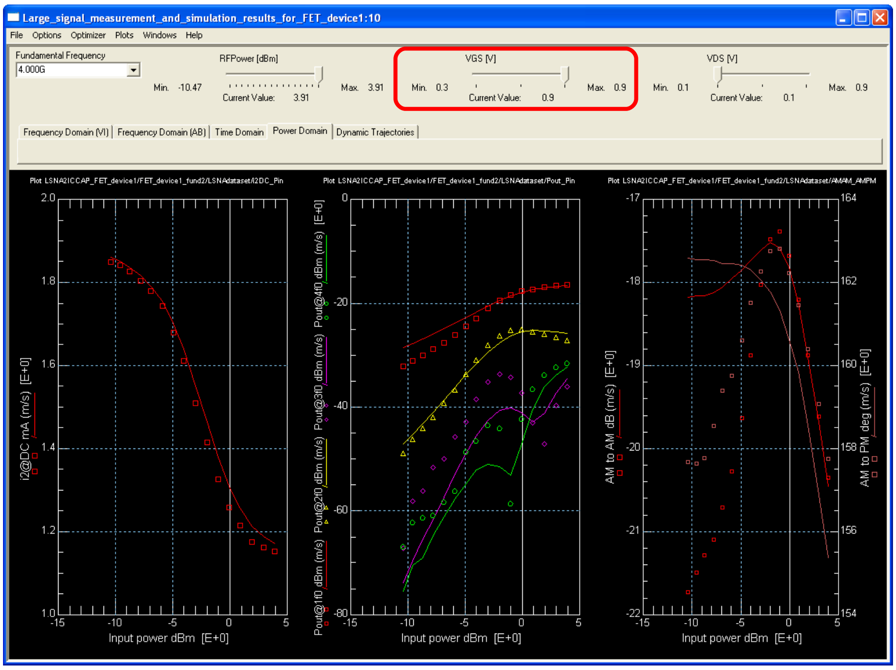

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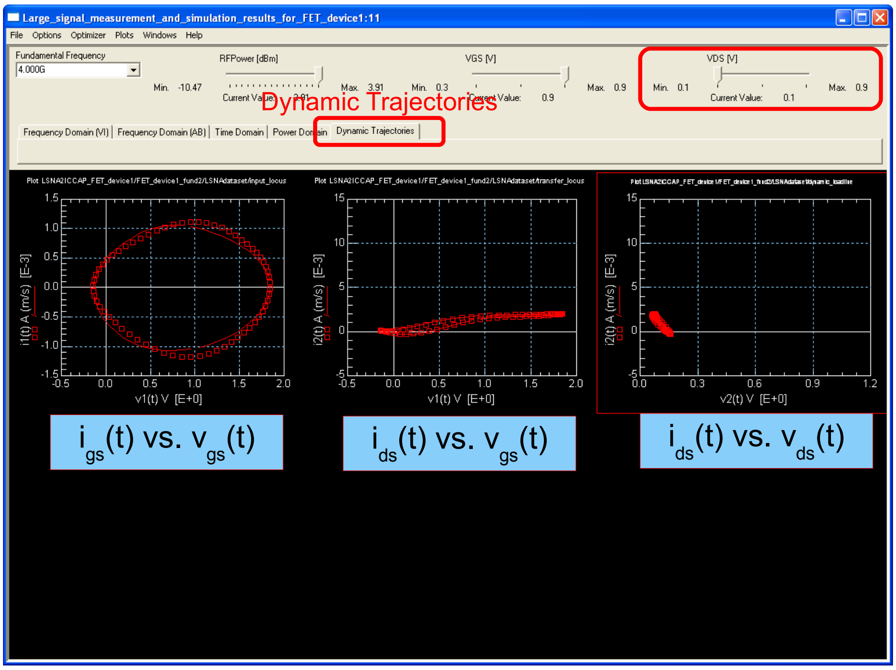

Dynamic trajectories are especially suited for the observation of the drain current behavior under changing DC bias conditions. Look how increasing the drain DC bias voltage changes the transfer and output (dynamic loadline) locii. In both plots we can observe that for a short time the drain current reaches negative values. This is due to a direct coupling through the gate-drain capacitances.

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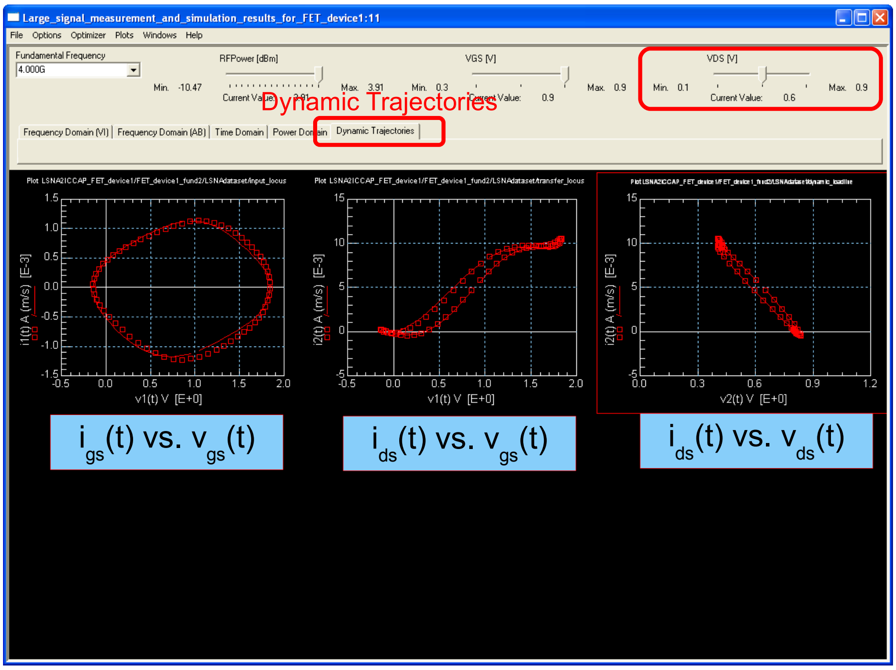

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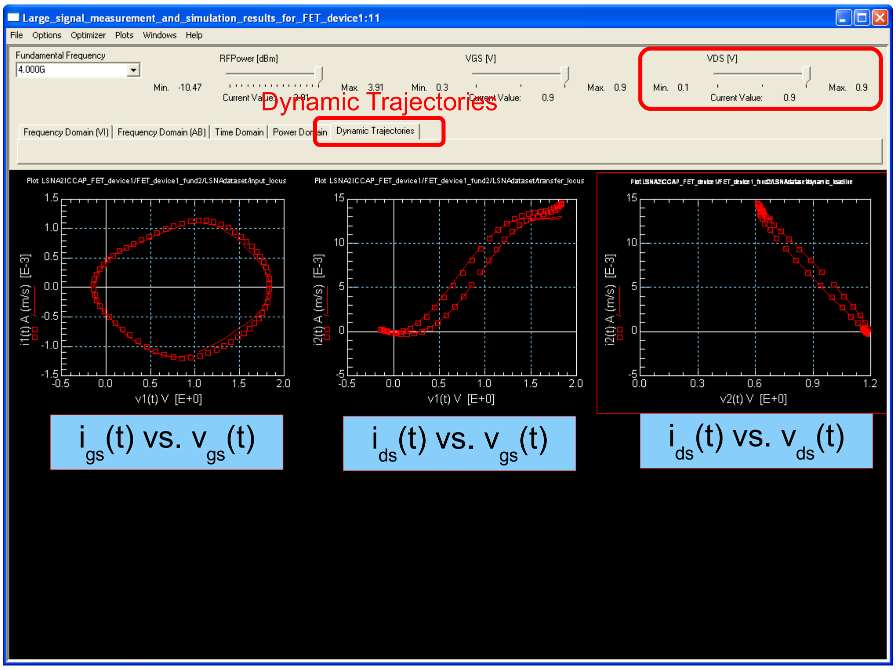

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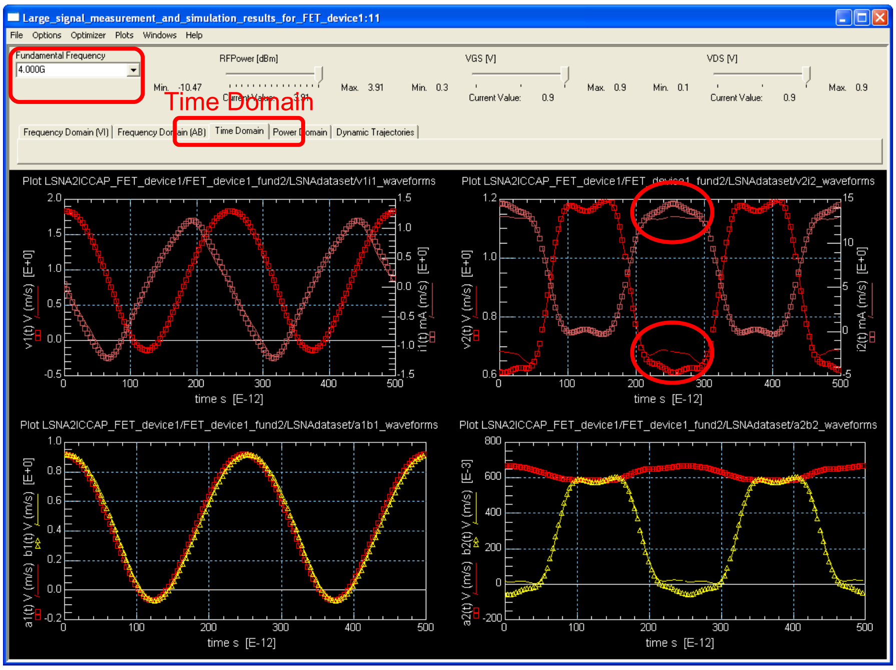

Let's go back to the time domain representation and sweep the fundamental frequency. In all three cases, there are some discrepancies between simulated and measured drain current and drain voltage waveforms. However, going back to the model tuning DC voltage conditions these discrepancies diminish rapidly.

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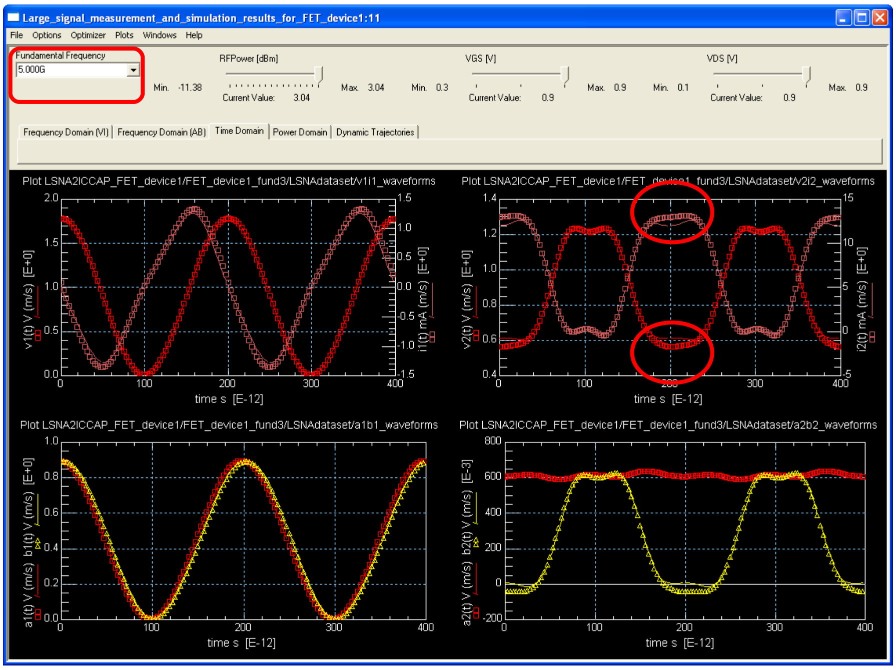

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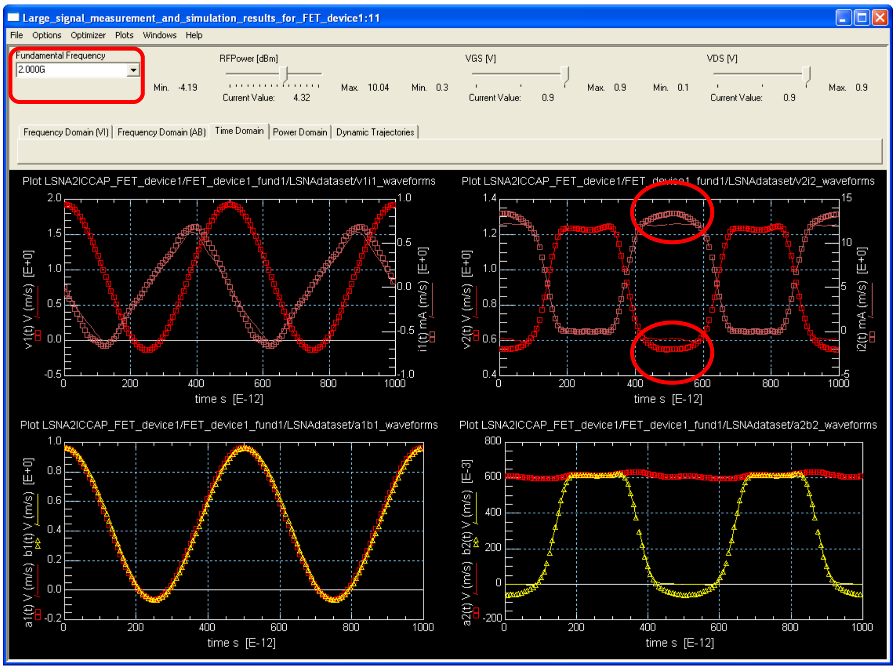

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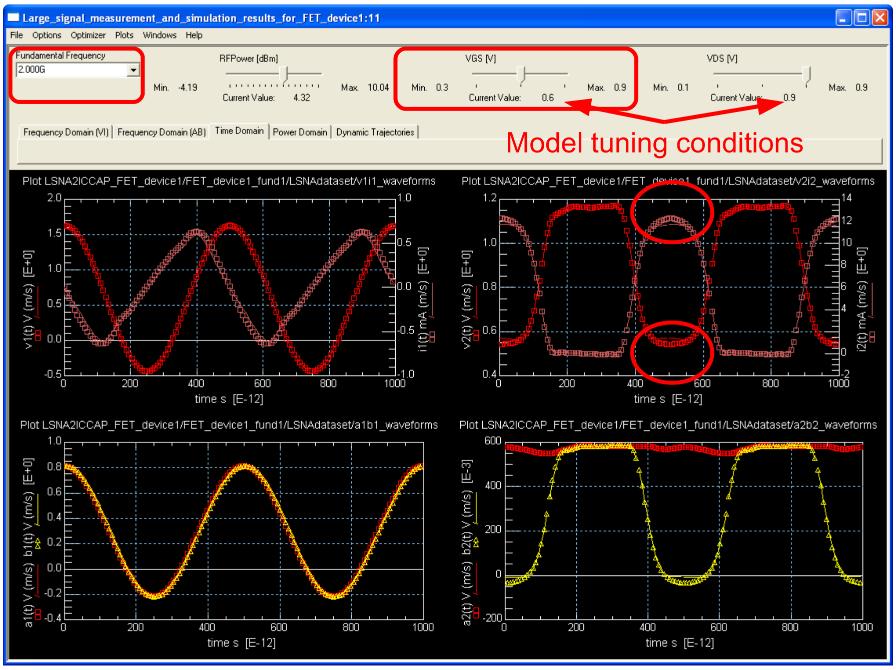

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Conclusions

- Large-signal measurements + device modeling program =
  - Complete large-signal device characterization and model accuracy assessment under realistic signals,
  - Simple access and improved usability of the measured data,
  - Model comparison and optimization.