

ZVxPlus Application:
Transistor Characterization,
Reliability and
Model Verification



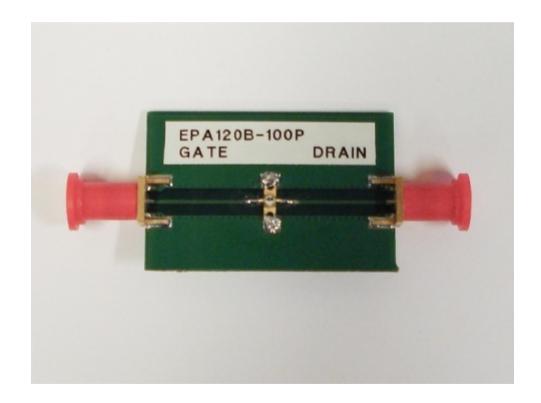
Outline

- The Device Under Test (DUT): EPA120B-100P
- Measurement Setup
- "Fire and Go..."
- Calibration and Deembedding Process
- DC IV Application
- DC+RF Measurement
 - Frequency Domain
 - Time Domain
 - Terminating Impedances
- Advanced Display: Dynamic lines
- Model Verification
- Conclusions

EPA120B-100P

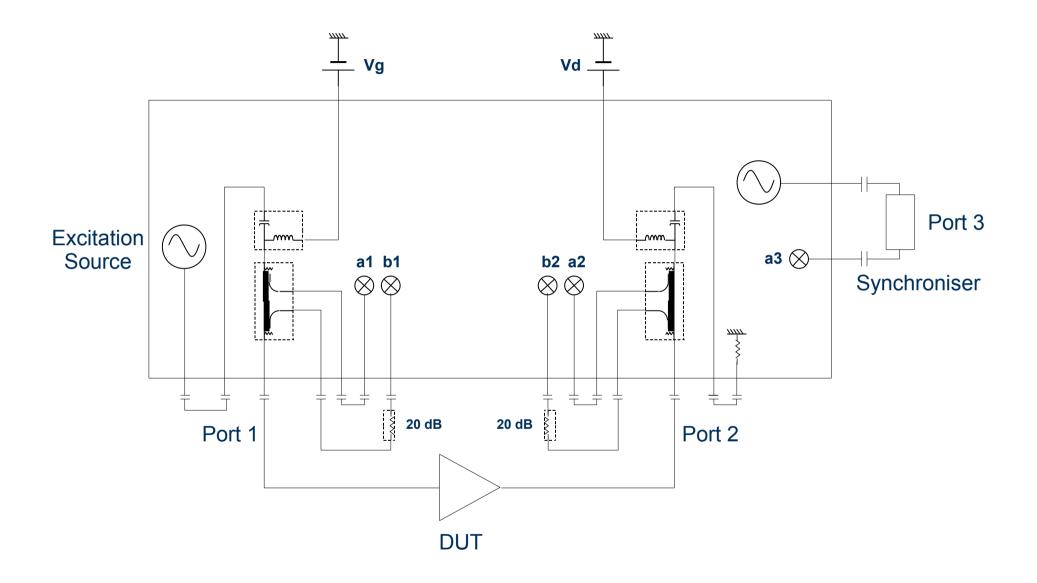
- EPA120B-100P
 - high efficiency heterojunction power FET
 - power output: + 29.0dBm typ.
 - power gain: 11.5dB typ. @ 12 GHz





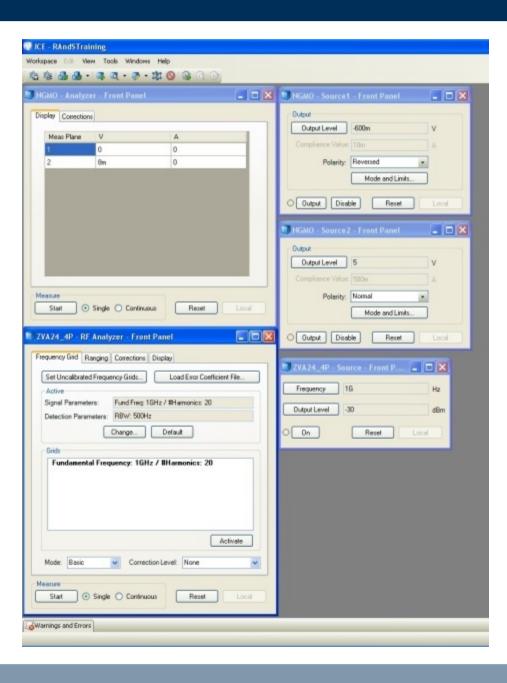
NMDG

Measurement Setup

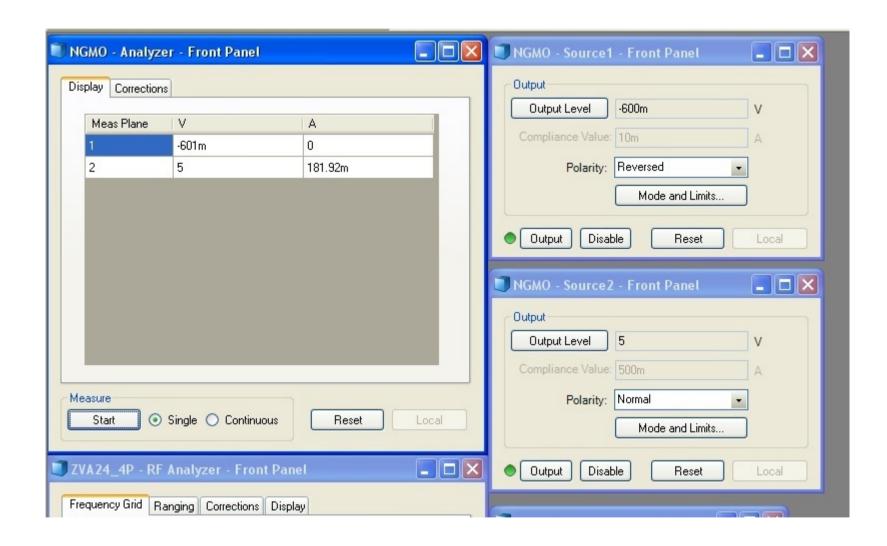


4 NMDG

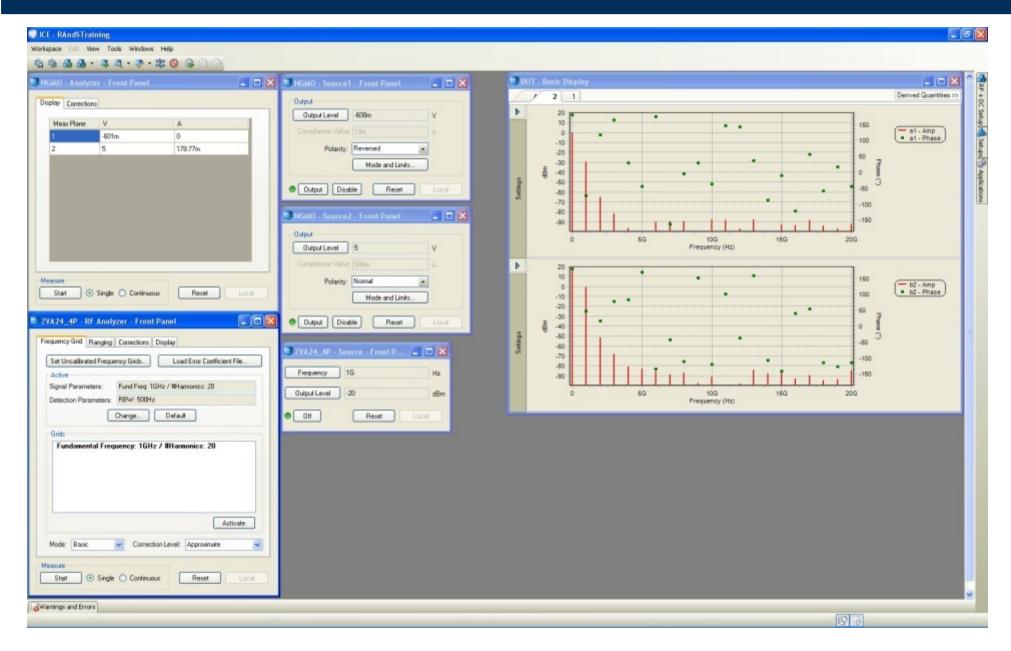
"Fire and Go..."



DUT properly working? (1)



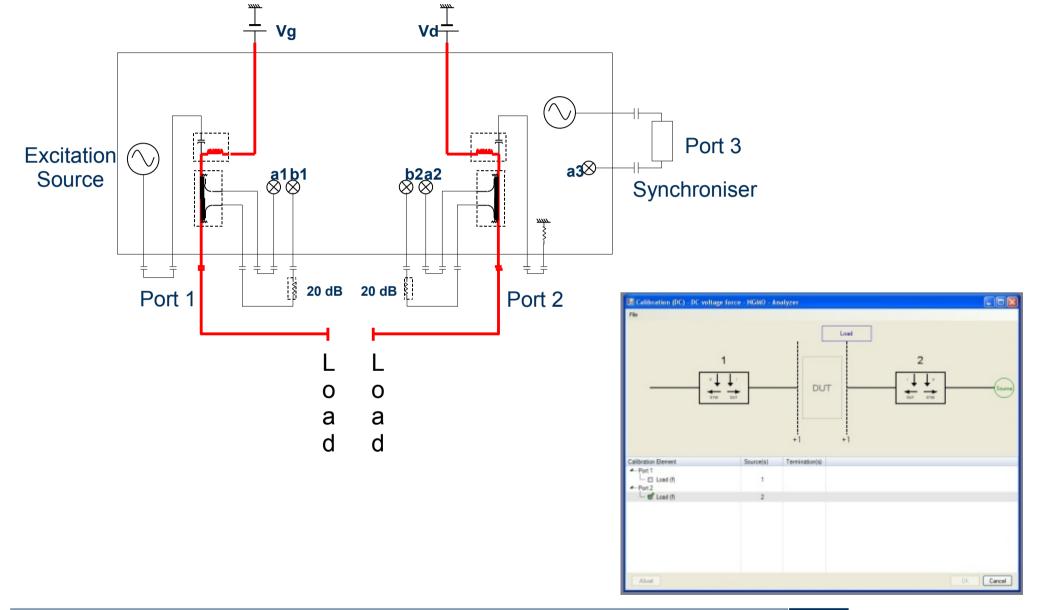
DUT properly working? (2)



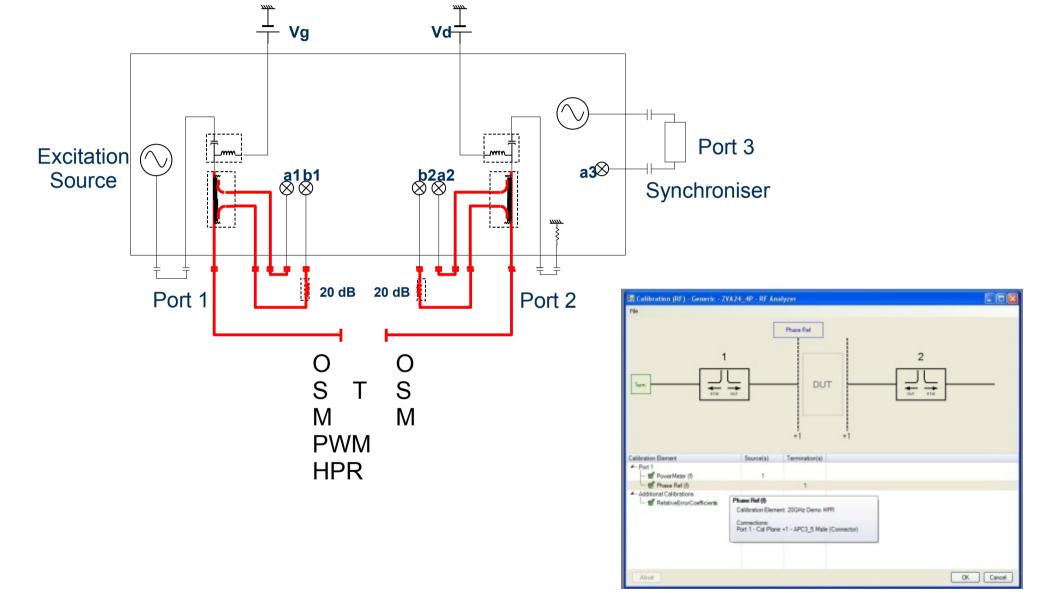
Next Step?

Calibration

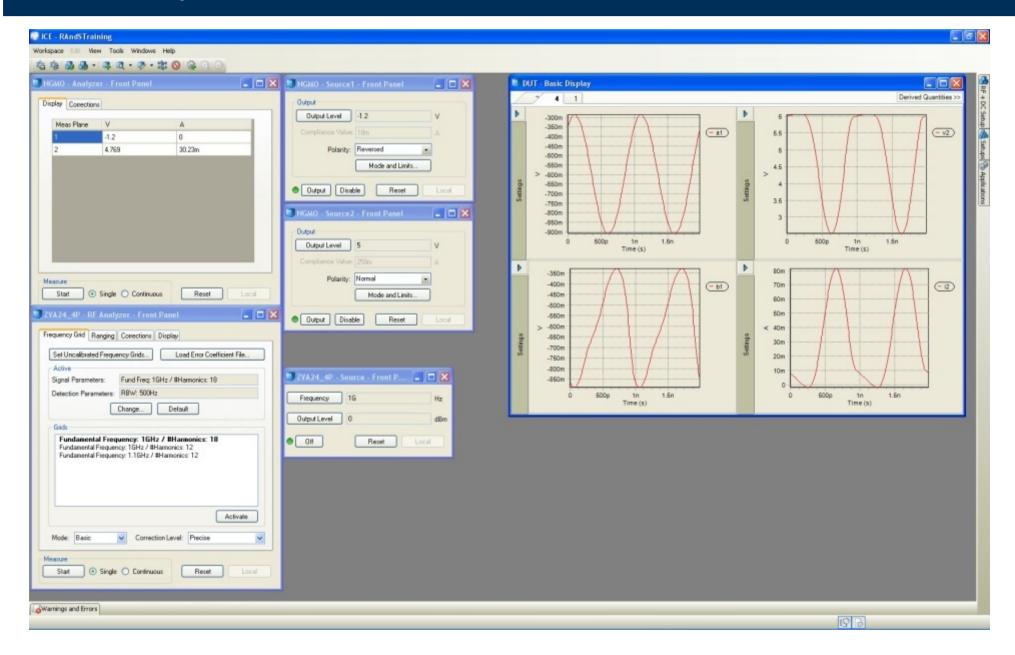
DC Calibration



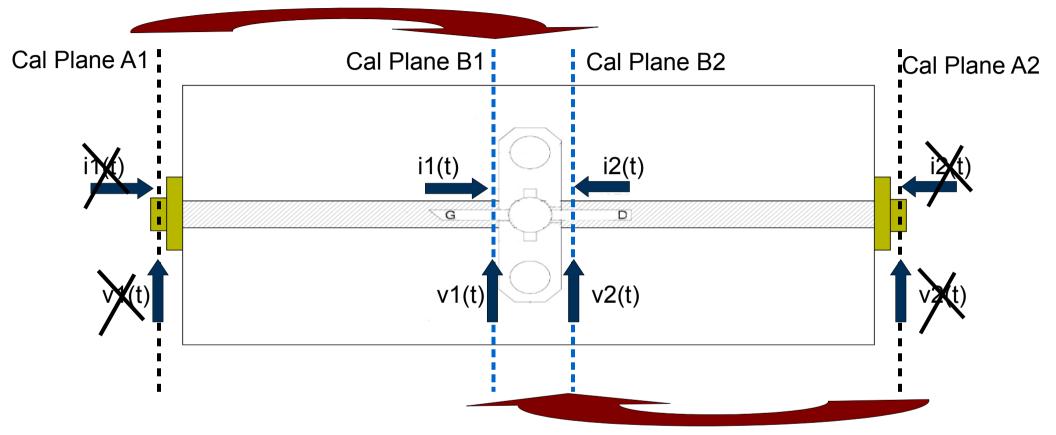
RF Calibration



DUT in pinch off?



Some words about deembedding



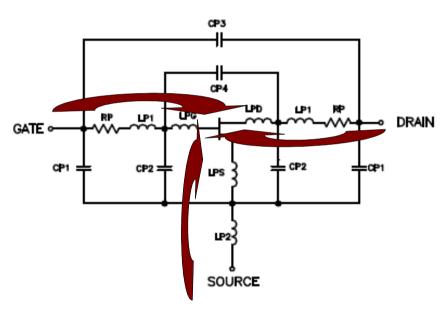
The DUT is placed on a PCB

- → using calibration plane A1 and A2 we measure the behaviour of the DUT AND PCB
- → using Multiline TRL (thru-reflect-line) we move the calibration plane to the DUT we measure the behaviour **ONLY** of the DUT

NMDG

Some words about deembedding

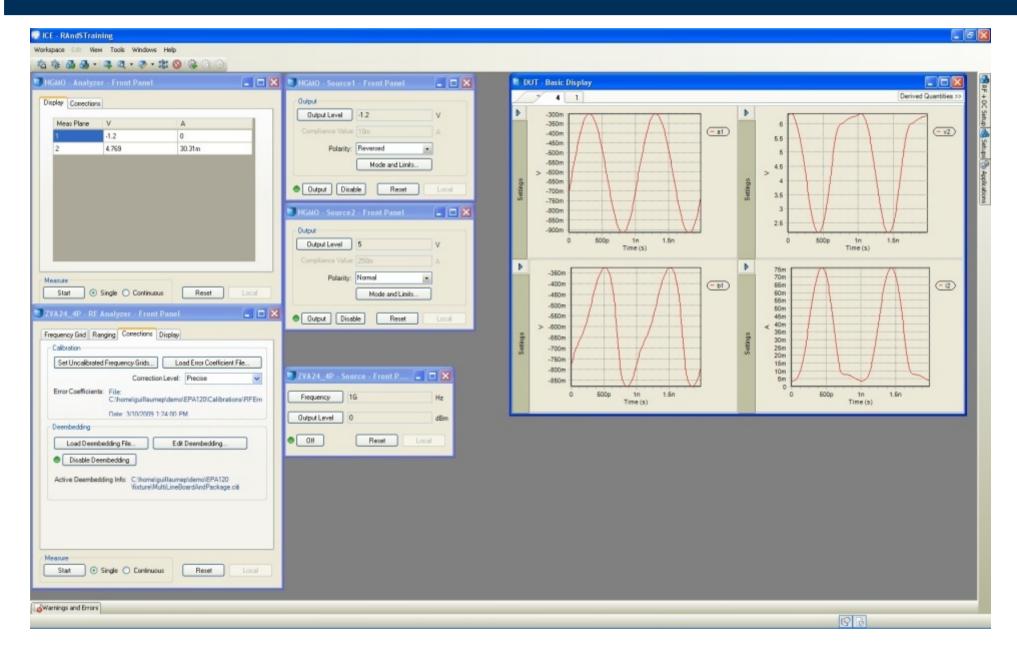
Include package



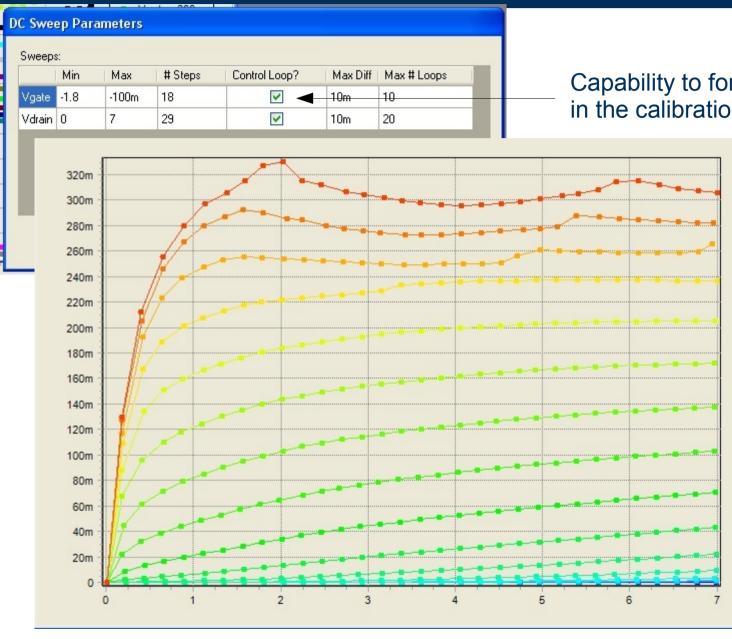
Using the FET Model, provided by the manufacturer the package can be included

PACKAGED FET MODEL

DUT in pinch off (with deembedding)



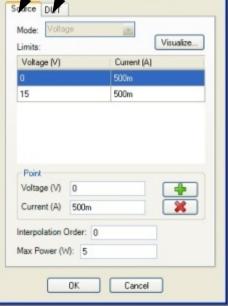
ICE DC IV Application



Capability to force the control variables in the calibration plane

DC Sweep Limits

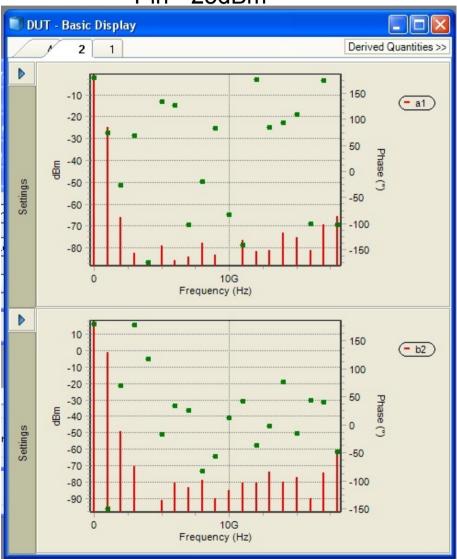
Defining limits at DC source and in calibration plane



ZVxPlus: Frequency Domain Characterisation - Phase

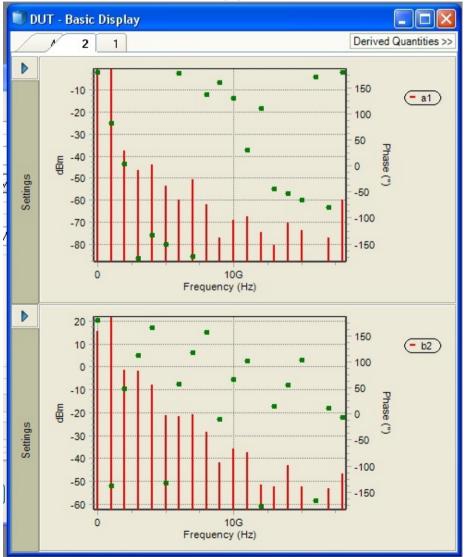
 $V_{gs} = -0.6V, V_{ds} = 5V f_0 = 1GHz$

Pin=-25dBm



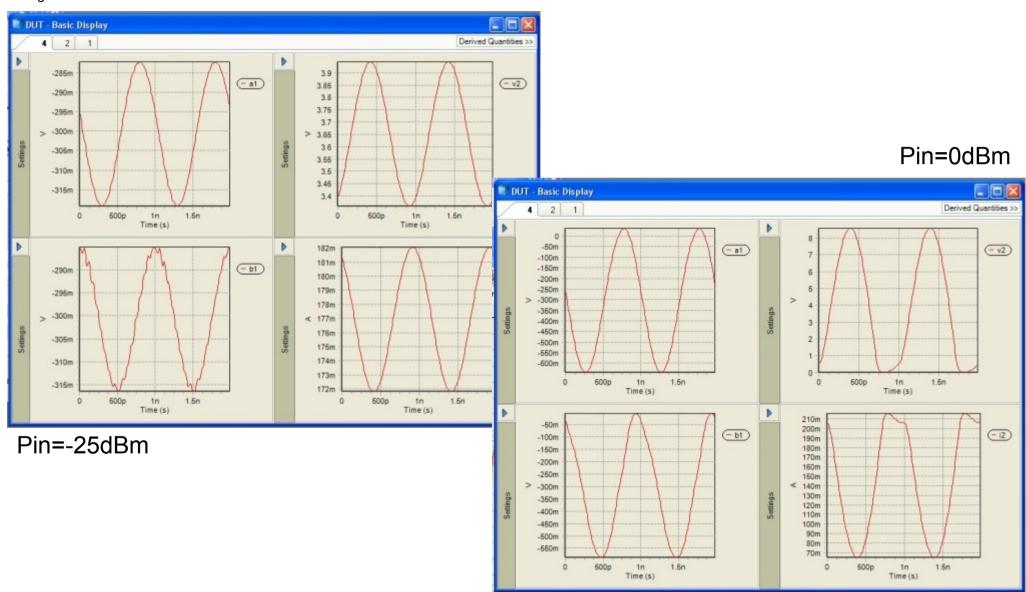
amplitude phase

Pin=0dBm



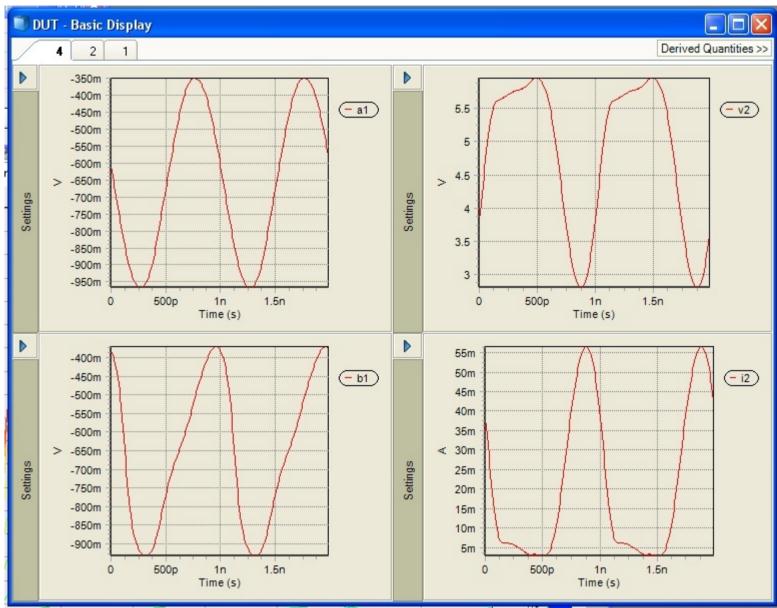
ZVxPlus: Time Domain Characterisation

$$V_{gs}$$
=-0.6V, V_{ds} =5V f_{0} =1GHz

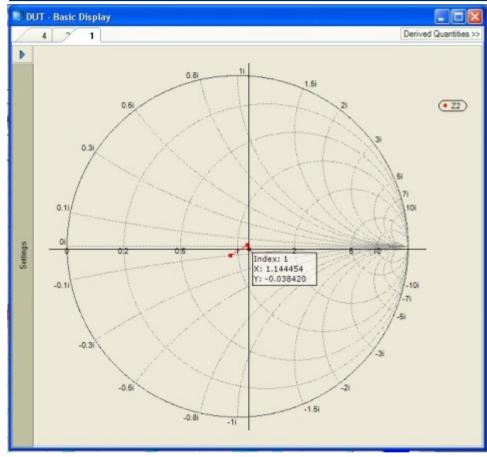


ZVxPlus: Time Domain Characterisation – Pinch Off

 $V_{gs} = -1.3V$, $V_{ds} = 5V$ $f_0 = 1$ GHz

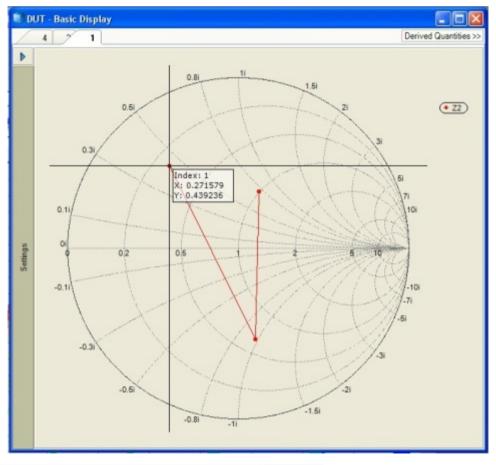


ZVxPlus: Terminating Impedances



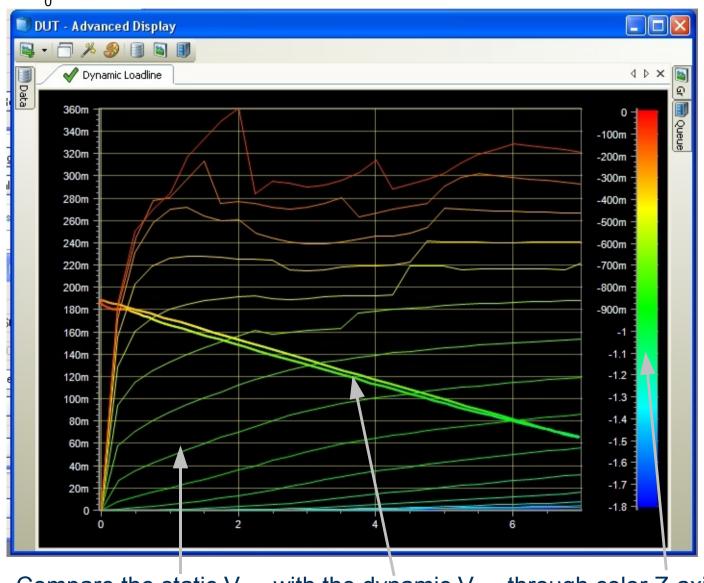
Output Impedance with 50 Ohm termination at fundamental and 2 harmonics

Output Impedance with Open termination at fundamental and 2 harmonics



ZVxPlus: Dynamic Loadline

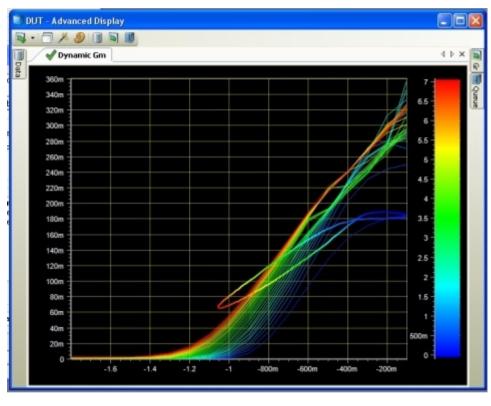
 V_{gs} =-0.6V, V_{ds} =4V f_0 =1GHz Pin = 0 dBm



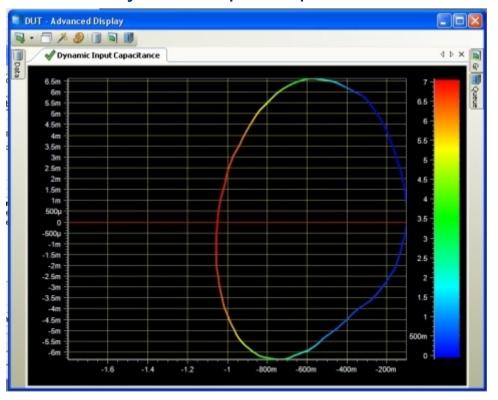
Compare the static V_{gate} with the dynamic V_{gate} through color Z-axis

ZVxPlus: Dynamic Gm and Input Capacitance

Dynamic Gm



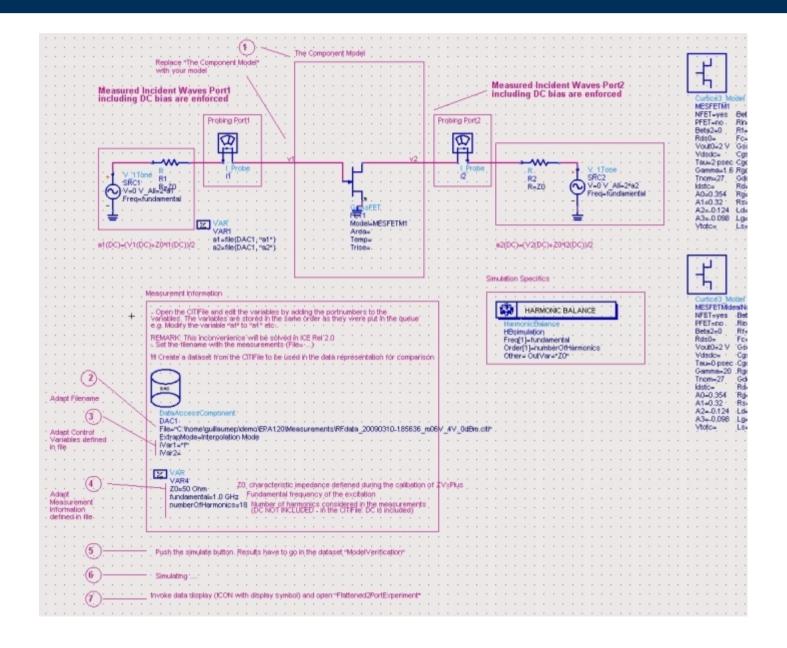
"Dynamic Input Capacitance"



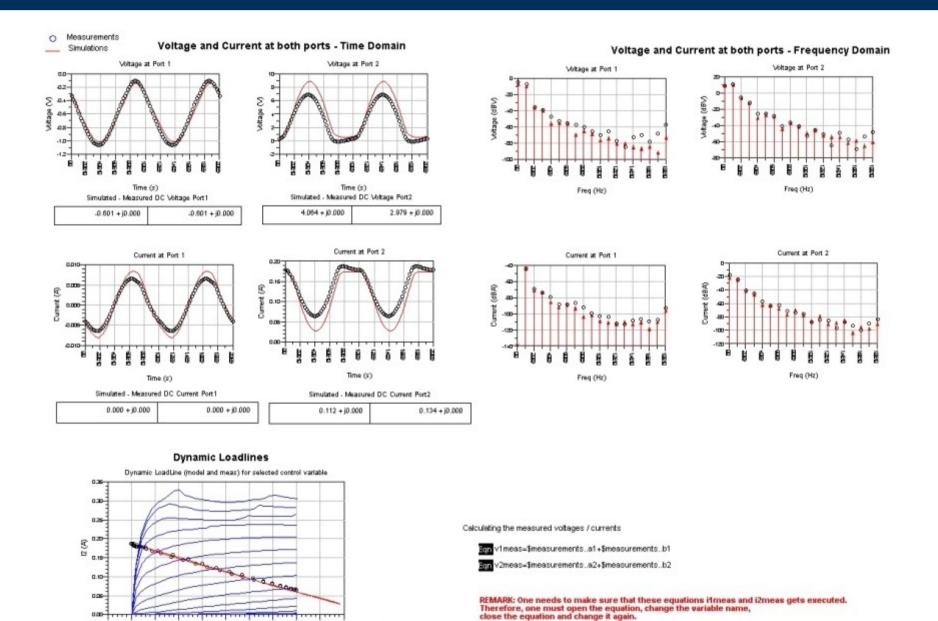
Exporting Measurements



Model Verification in ADS



Measurement vs Simulation



Conclusions

- Prepare measurement setup and ICE
- Calibration steps
- Deembedding capability
- DC and RF Transistor Characterization
- Basic Displays
- Advanced Displays: Dynamic Lines
- Model Verification