INT2095

U T A H

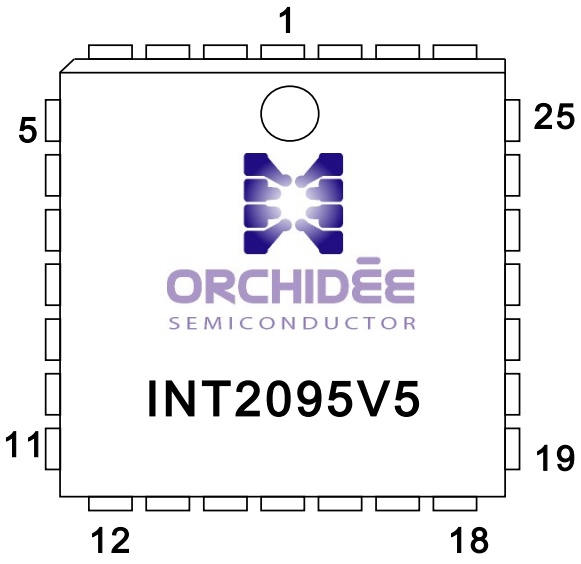
Orchidée Semiconductor U_p Interface Transceiver

Features

- Pin-for-Pin replacement for industry-standard PEB2095 (IBC) component
- Up to 3.0km (0.5mm) line interface performance
- NT (LT) and TE mode support
- IOM1 and IOM2 backplane interface modes
- Special function pins for interface to other INT2095's or layer-2 devices
- Custom versions with Orchidée core technology
- Low Power dynamic operation
- Single 5V supply
- 28-pin PLCC (standard) package

Description

The Orchidée Semiconductor INT2095 is a fully featured replacement for the industry standard Up interface layer-1 device. It supports loop lengths up to 2.0km over AWG24 cable and provides all signal conditioning, equalization and adaptive threshold adjustment to optimize line performance. The backplane interface supports both IOM1 and IOM2 modes and provides access to all subchannels of the interface including B, D, CI and M-channels. Special function pins (X0-X4) and a master clock output are included in the device for integration with other INT2095's or layer-2 devices.



March, 2001

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (V_{SS} = 0V, T_J = 25^{0}C)

Parameter	Symbol	Rated Values	Unit
Power Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_I	-0.3 to +7.0	
Output Voltage	V_O	-0.3 to VDD	
Input Current	I_I	-10 to +10	mA
Output Current per I/O	I_O	-10 to +10	
Storage Temperature	T_{STG}	-65 to +150	^{0}C

Recommended Operating Conditions (V_{SS} = 0V)

Parameter	Symbol	Rated Values	Unit
Power Supply Voltage	V_{DD}	+4.75 to +5.25	V
Junction Temperature	T_J	-40 to +100	^{0}C

DC Characteristics (Over Operating Range)

Parameter	Symbol	Conditions	Rated Values			Unit
			Min.	Typ.	Max.	
High Level Input Voltage	V_{IH}		2.0	-	V_{DD}	V
Low Level Input Voltage	V_{IL}		0.0	-	0.8	
High Level Output Voltage	V_{OH}	I_{OH} = TBD	2.4	-	-	
Low Level Output Voltage	V_{OL}	I_{OL} = TBD	-	-	0.4	
High Level Input Current	I_I	$V_{IH} = V_{DD}$	-	-	10	uA
Low Level Input Current	I_O	$V_{IL} = V_{SS}$	-10	-	-	
3-State Output Leakage Current	I_{OZH}		-10	-	10	
	I_{OZL}		-10	-	10	
Stand-by Current	I_{DDQ}	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$		TBD		

Pin Descriptions

Pin	Signal	Type	Description
1	VDDA	Supply	Analog Power, +5V
2	N.C.	Not Connected	
3	X0	I/O	Special Function Pin
4	X4	I/O	Special Function Pin
5	X3	Input	Special Function Pin
6	X1	I/O	Special Function Pin
7	XTAL_OUT	Output	Clock Output
8	XTAL1	Clock Oscillator	
9	XTAL2	Clock Oscillator	
10	M1	Input	Mode Select
11	nRST	Input	Asynchronous, Active-Low Reset
12	X2	Input	Special Function Pin
13	SDO	Output	IOM/IOM2 Interface
14	FSC	I/O	IOM/IOM2 Interface
15	DCL	I/O	IOM/IOM2 Interface
16	SDI	Input	IOM/IOM2 Interface
17	VSS	Supply	Ground
18	VSS	Supply	Ground
19	LIO2	I/O	Line Connection
20	LIO1	I/O	Line Connection
21	VDD	Supply	Digital Power, +5V
22	VDD	Supply	Digital Power, +5V
23	VDD2	Output	2.5V Analog Reference Voltage
24	VSSA	Supply	Analog Ground
25	CLK_EN	Input	Active High Clock Output Enable
26	DISS	Output	Disable Supply
27	nTST	Input	Active Low Test Mode Select
28	M0	Input	Mode Select

Operation Modes

Mode	TE	TE	NT	NT
IOM Interface	IOM1	IOM2	IOM1	IOM2
M0	0	0	1	1
M1	0	1 (or tie to nRST)	0	1
DCL	Output: 512kHz, 1:1 Duty Cycle, synchronized to U-interface	Output: 1.536MHz, 1:1 Duty Cycle, synchronized to U-interface	Input: 512kHz	Input: 4.096MHz
FSC	Output: 8kHz, 1:1 Duty Cycle, synchronized to U-interface	Output: 8kHz, 1:2 Duty Cycle, synchronized to U-interface	Input: 8kHz	Input: 8kHz
X0	Output: 3.84MHz	Output: 3.84MHz	Output: CONF4	Input: TS0
X1	Output: 1.536MHz, 1:1 Duty Cycle, synchronized to U-interface	Output: 768kHz, 1:1 Duty Cycle, synchronized to U-interface	Output: 15.36MHz, 1:1 Duty Cycle	Input: TS1
X2	Input: 0	Input: 0	Input: 0	Input: TS2
X3	Input: ENCKB	Input: ENCKB	Input: MPF	Input: MPF
X4	Output: 2.56MHz, 1:2 Duty Cycle, Output: 7.68MHz, 1:1 Duty Cycle, synchronized to U-interface	Output: 2.56MHz, 1:2 Duty Cycle, Output: 7.68MHz, 1:1 Duty Cycle, synchronized to U-interface	Input: PFOFF	Input: PFOFF

ORCHIDÉE SEMICONDUCTOR

INT2095

Description of Terms

ENCKB: Enable clocks in TE mode, deactivated state. Active-low input signal. When high, the clock outputs are in the high impedance state.

PFOFF: NT mode Powerfeed off state. Also indicated by a HI on the C/I channel.

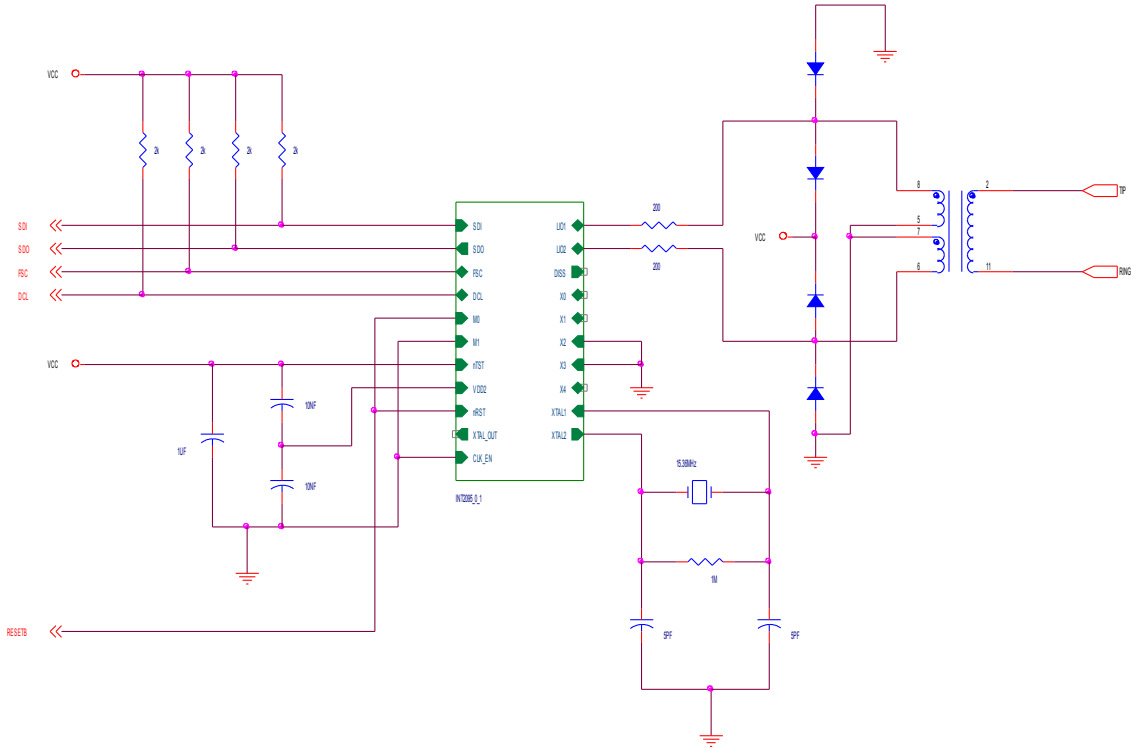
MPF: Main Power Feed serial input, 8-bits synchronous with the B1 channel of the IOM interface.

CONF4: General purpose output which is programmed via the Monitor channel registers.

TS2-TS0: IOM Timeslot assignment number (0 to 7) in NT mode.

INT2095

Connection Diagrams



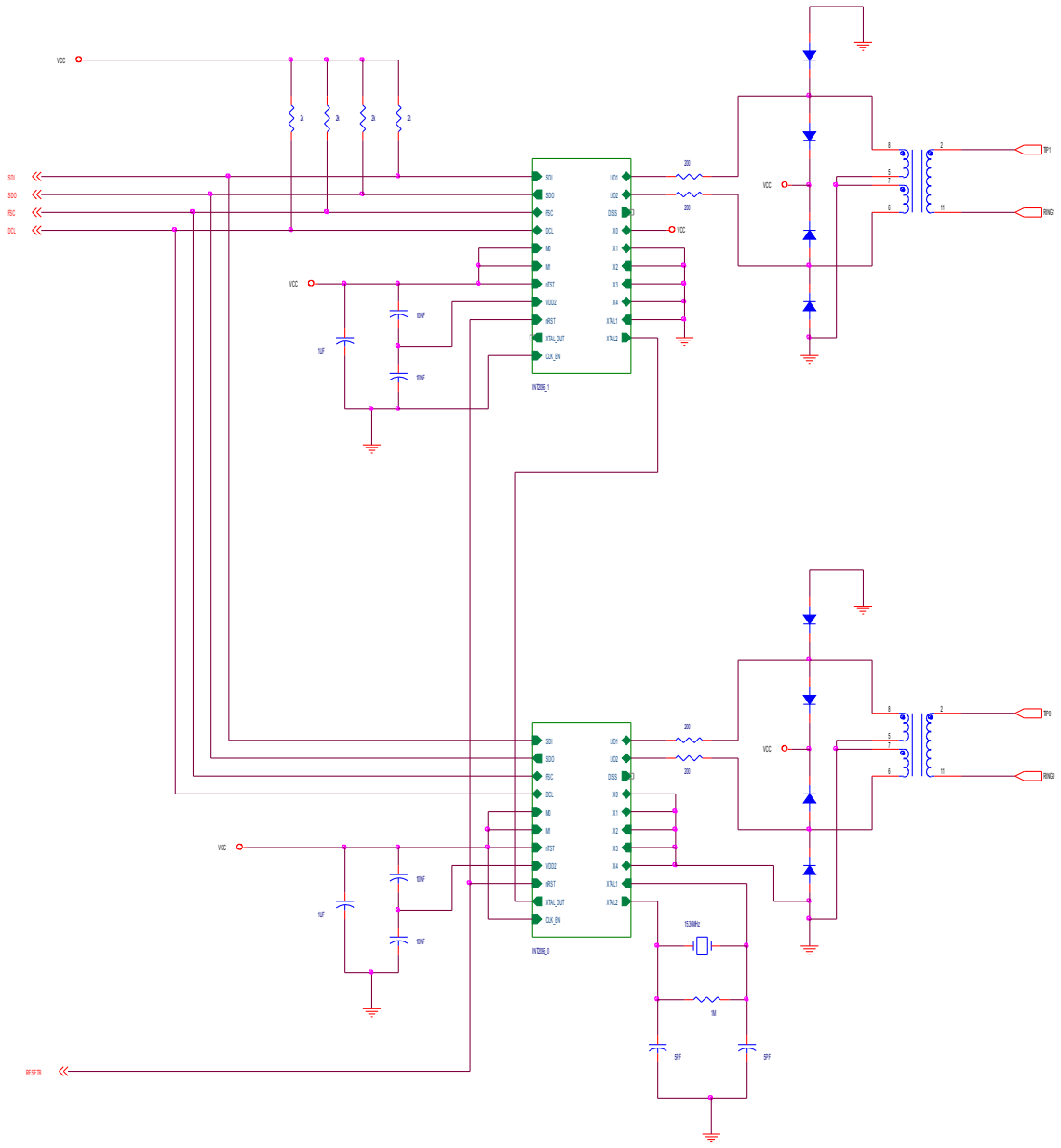
INT2095 applied in TE (IOM2)-Mode

March, 2001

ORCHIDÉE SEMICONDUCTOR

INT2095

Connection Diagrams (cont.)



2 INT2095's applied in NT (IOM2)-Mode

March, 2001

INT2095

Contact Information

Company Headquarters:
Orchidée Semiconductor, Inc.
102 S. Tejon St., Suite 1100
Colorado Springs, CO 80903 USA
Telephone: +1 719-578-3320
http://www.orchidée.com

Sales Offices:

North America Region
Orchidée Semiconductor
P.O. Box 7593
San Jose, CA 95150-7593
Tel: 408 321 7600
Fax: 408 321 7601

Contact:
Asif Subedar
e-mail: asifs@norcalts.com

Central Europe
Orchidée Semiconductor
Ruhbronnweg 11/1
D- 74385 Pleidelsheim
Germany
Tel: +49 7144 884550
Fax: +49 7144 884551

Contact:
Rainer Hake
e-mail: rhake@orchidee.com

Northern Europe/Scandinavia
Orchidée Semiconductor
Heleneborgsg 21
117 31 Stockholm
Sweden
Tel: +46 (0) 8 669 5650

Contact:
Lars Nilsson
e-mail: lars.nilsson@tele2.se

March, 2001