Yield Enhancement of Wineglass Contact Process Using QYield

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Abstract

A process using wineglass shaped contacts experienced sporadic occurrences of under-etched contacts. The spatial distribution of bad contacts was random as both well-defined and under-etched contacts could be seen within several microns of one another. The investigation into the cause of the problem focused on particles or bubbles in the photoresist and potential defects during the buffered oxide etch (BOE) used to isotropically etch the upper portion of the contact (bowl) or the anisotropic dry etch used to form the lower portion of the contact (stem). Typical equipment correlation troubleshooting procedures did not yield usable results because each etch step involved a dedicated tool. QYield software was then utilized to find any statistically significant correlation that was not evident to yield engineering. The results showed a correlation to specific operators and further investigation revealed a shift dependence, and ultimately, a direct correlation of failure rate to bath life of the pre-BOE etch wetting process.

Background

As integrated circuits shrink ever so smaller in order to fit more die on a wafer, the cost per chip is lowered and development of unique structures must take place, while ensuring the highest quality and performance of such chips.

An example of a more complex structure associated with such integration is the wineglass shaped contact. The wider top of the contact (bowl) allows high aspect ratio contacts to be more easily and completely filled by metal interconnect and to reduce the high stress that comes with a sharp contact edge. Additionally, because the density of devices is at its most critical at the silicon surface and less critical in the interconnect layers above, a contact that is smaller at its bottom and wider at its top allows more tightly packed devices, smaller chips, and greater profit margin per wafer. A sample cross-section of such a contact is shown in Figure 1.

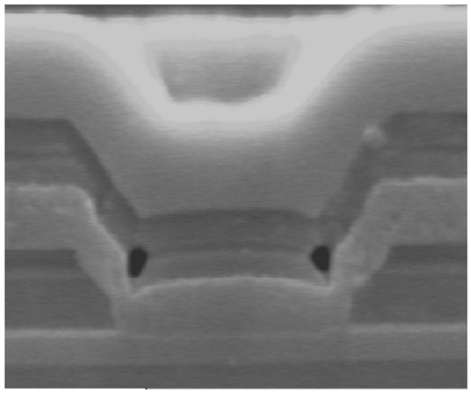

Figure 1

One drawback of this type of contact is that it is formed by a sequence of two separate etches. Not only does this increase the overall process time but it introduces one more cause for process variation.

The problem experienced on one of our High Voltage Integrated Circuit (HVIC) processes affected lots randomly and resulted in up to 50% yield loss. Inspection of such lots showed that random minimum sized contacts were either not open or displayed a “blown” or widened bowl.

Under-etched contacts could have been explained by particles or bubbles in the photoresist or some defect that blocked one of the two etches. Blown bowls were a little more difficult to explain. Their shape was not deformed as one would expect from a photoresist adhesion or flow problem, they were merely wider than normal. Figure 2 shows an example of what we were seeing.

The sequence of steps involved in formation of the contact along with the potential problems that can occur at each step is as follows:

1. Prime and Coat wafers with photoresist – poor adhesion, particles/bubbles in resist
2. Print contact pattern on wafers with UV Stepper – out of focus
3. Develop photoresist to open the areas that will be etched
4. Bake photoresist to prevent reflow – missed step, flowing resist
5. Dip wafers in surfactant bath to prevent wet etch capillary effect - insufficient wetting
6. Etch wafers in BOE bath, rinse, dry in srd - particles blocking etch, bubbles
7. Etch wafers in plasma etcher – particles blocking etch
8. Strip photoresist
9. Deposit metal interconnects

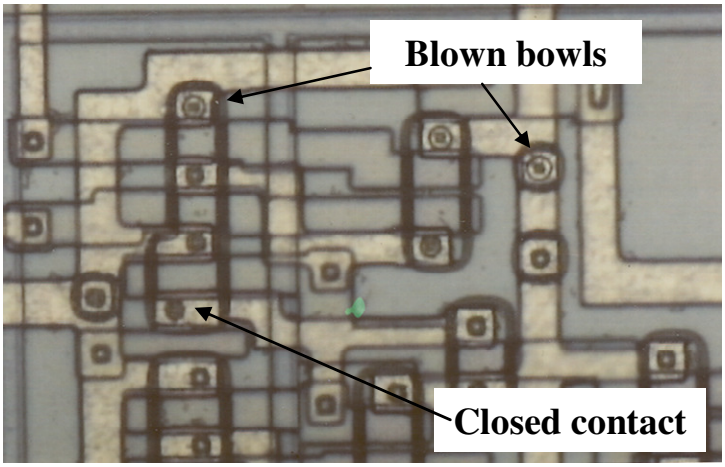

Figure 2

Investigation and Results

With knowledge of the nature of the small contacts, we were able to eliminate the Print (Align) and Bake steps. Any problems here would have affected every contact in a localized area. The problem was clearly defect density related. The Prime and Coat steps were also exonerated after showing that no problem was found on other layers. If the resist was not adhering properly or if particles or bubbles existed in the resist, every layer, some of which had smaller geometries than the contact layer, would have been affected.

Therefore, by process of elimination, we began to focus on the wet bowl and dry stem etches. The BOE bowl etch was first targeted. BOE is known to contain high particulates due to the nature of the process. It is industry practice to follow all BOE etches with clean steps in order to remove excess particles from the wafer surface. A time line was generated of all lots through the BOE sink and revealed that no correlation to time existed. In fact, lots run on a brand new bath were just as likely to have small contacts as a bath that had been running consistently for several days.

Finally, we looked at the critical pre-BOE wetting step, a dip in a surfactant bath that reduces surface tension and allows for a uniform etch. This step is generally wrapped into the etch step so the same timeline

as BOE was assumed and this revealed nothing out of the ordinary. No correlation to maintenance on the tool was found. At this point we talked to the operators that performed the process. Because the tool was not automated, the operators were required to manually dunk the cassette of wafers into the surfactant bath. We found that they had a rule of thumb by which they dunked a specific number of times before transferring the cassette of wafers immediately into the BOE bath.

The realization that the pre-wetting step was reliant on the routine of each operator became an aha! moment. We vigorously pursued this line of investigation with the idea that each operator performed the dunks a little differently and thus could explain the issue. We met with each operator, asked them to walk us through the process, stood by them as they showed us what they did, hoping to discover the mysterious anomaly that could explain everything.

When each operator showed us their method, it appeared each was consistent across the group and across shifts, the air drained from our proverbial balloon. Where to turn next?

When the yield manager suggested using QYield to analyze the data and potentially find a solution, we moved forward. However, because several different yield loss mechanisms could affect any given lot and many caused the same bins and even some of the same probe tests to fail, QYield analysis did not yield usable results at this time.

The challenge for engineering at that point was to find a unique parametric or probe test that could differentiate this specific problem from all the rest. Ultimately, two electrical test parameters were found that had a higher rate of failure on lots affected by small contacts than on clean lots. This came as quite a surprise to engineering considering the defect nature of the failures. One would not readily think that a defect mechanism would consistently affect one particular small device in the test die.

Examination of the test structure in question revealed that it had both minimum sized contacts as well as surrounding topography close to the contact, an ideal combination for the failure to occur.

Some of the credit for finding these sensitive devices must be given to QYield which forced us to find an electrical result that differentiated this problem from all the rest. With the new data in hand, we moved forward with a second round of QYield analysis. Figure 3 shows the graphical result and Figure 4 the statistical result.

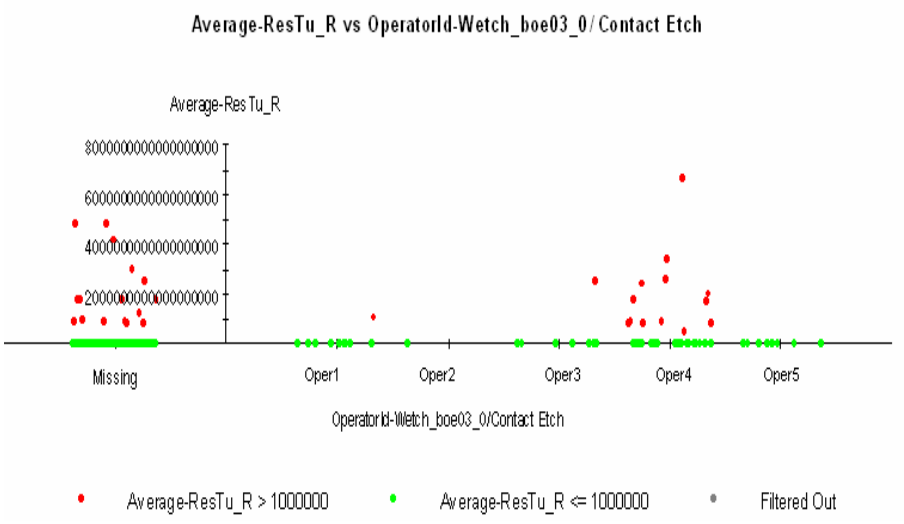

Figure 3

Rule 1: OperatorId-Wetch_boe03_0/Contact Etch = Oper4

	Average-ResTu_R > 1000000?			
	Target True		**Target False**	
General Population*	16.4%	(34)	83.6%	(173)
Rule Condition True	35.0%	(14)(a)	65.0%	(26)
Rule Condition False	6.5%	(2)	93.5%	(29)(d)

Figure 4

Figure 3 shows a higher tendency to fail when Oper4 (and occasionally Oper3) performs the processing at the pre-wet and BOE etch steps, something we believed we had just eliminated with our previous investigation. The statistical analysis resulted in a value close to 100% for the Condition False/Target False entry. As explained by the QYield documentation:

"If the fraction d where the rule is false and the target is false is near 100%, then the rule is a necessary condition for the target to occur: the target condition does not occur unless the rule is true…….If the fraction d where the rule is false and the target(Average-ResTu_R > 1000000) is false is near 100% and the fraction a where the rule condition is true and the target is true is not near 100% then this implies that other factors, possibly not represented in the data, are required to explain why the target is true."

In other words, QYield clearly showed a necessary condition for the rule to occur, and then pointed out that other factors might exist.

It occurred to us that the operators represented by Oper3 and Oper4 worked on second shift, while the rest worked on first and third shifts. We looked at the bath change schedule of the surfactant bath and it showed that it was regularly dumped, cleaned and refilled once daily and that change occurred following the second shift or at the beginning of third shift.

QYield had revealed that the tendency to fail for small contacts was extremely high on one shift, which led us to the realization that second shift represented the end of each day's bath life. Follow-up experiments proved that wafers run on a bath that was less than 12 hours old did not show the problem, while those run on a bath that was between 12 and 24 hours old did show the problem. The secondary factor may have been related to volume of wafers run throughout the day or performance of the bath itself on a day to day basis.

Based on these findings the surfactant bath change frequency was changed from once daily to twice daily. The problem was not detected after the change.

Conclusion

Most yield troubleshooting occurs quickly and without a documented problem solving algorithm. Normally an engineer or a team of engineers attacks the most probable causes of a problem, frequently with much success. However, when a more complex and subtle issue appears, better tools and better methodologies are required. In this case, not only did the QYield methodology force engineering to find just the right data needed for statistically relevant analysis, but it was able to crunch a massive amount of data and reveal the root cause of our problem. Based on the QYield results, yield engineering looked at something it had not thought to look at previously, solving a costly problem and improving the wet etch process for all technologies.