RS9110-N-11-03

Module Integration Guide

Version 3.0

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About this Document

The RS9110-N-11-03 is a dual-band 802.11n single-stream module with built-in MAC/BBP, RF and PA, and front-end components. It interfaces to a host processor through an SDIO or SPI interface. This document provides information that may be used while integrating the module into an end solution.

Table Of Contents

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1 Reference Schematics

The following is a reference circuit schematic of an Evaluation Board using the RS9110- N-11-03 WLAN module. The schematics show both SDIO and SPI host interface options. The layout corresponding to this schematic is also shown in this document as a reference.

1.1 SDIO Interface Integration

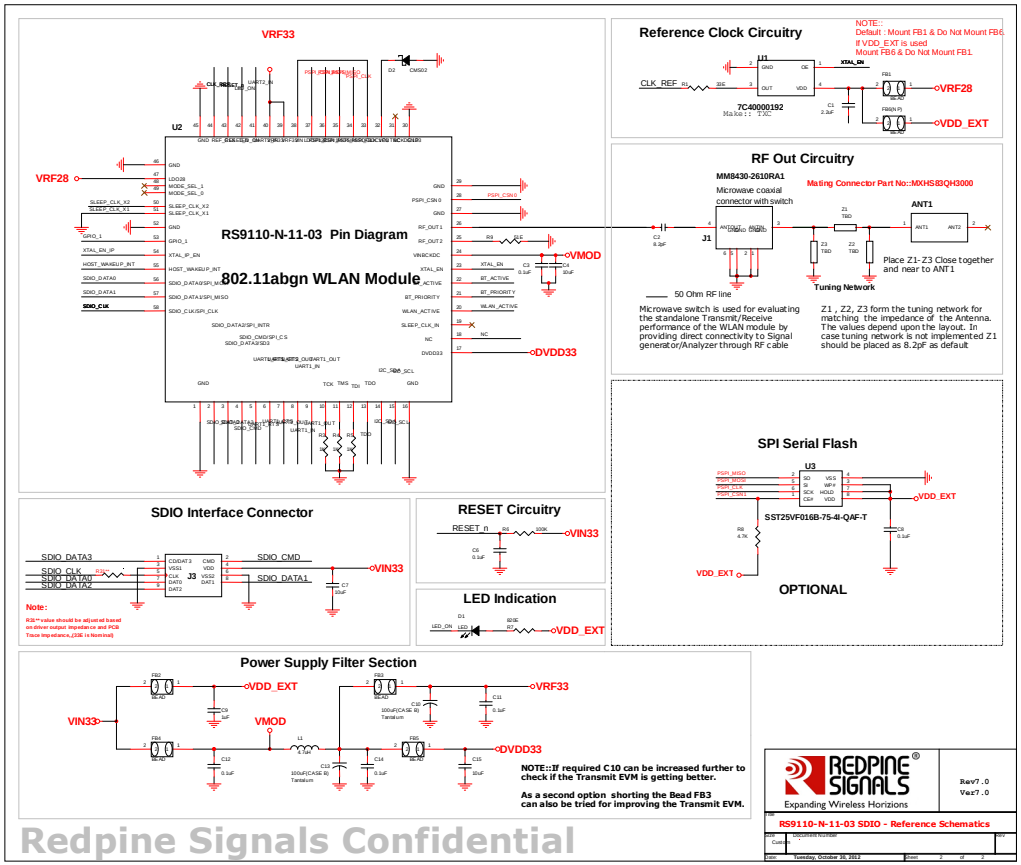

Figure 1 SDIO Interface Integration

NOTE: Pull up resistors should be present on SDIO_CMD & SDIO_Data lines according to the section 6.6.5 of SD physical layer specification, version 2.00

1.2 SPI Interface Integration

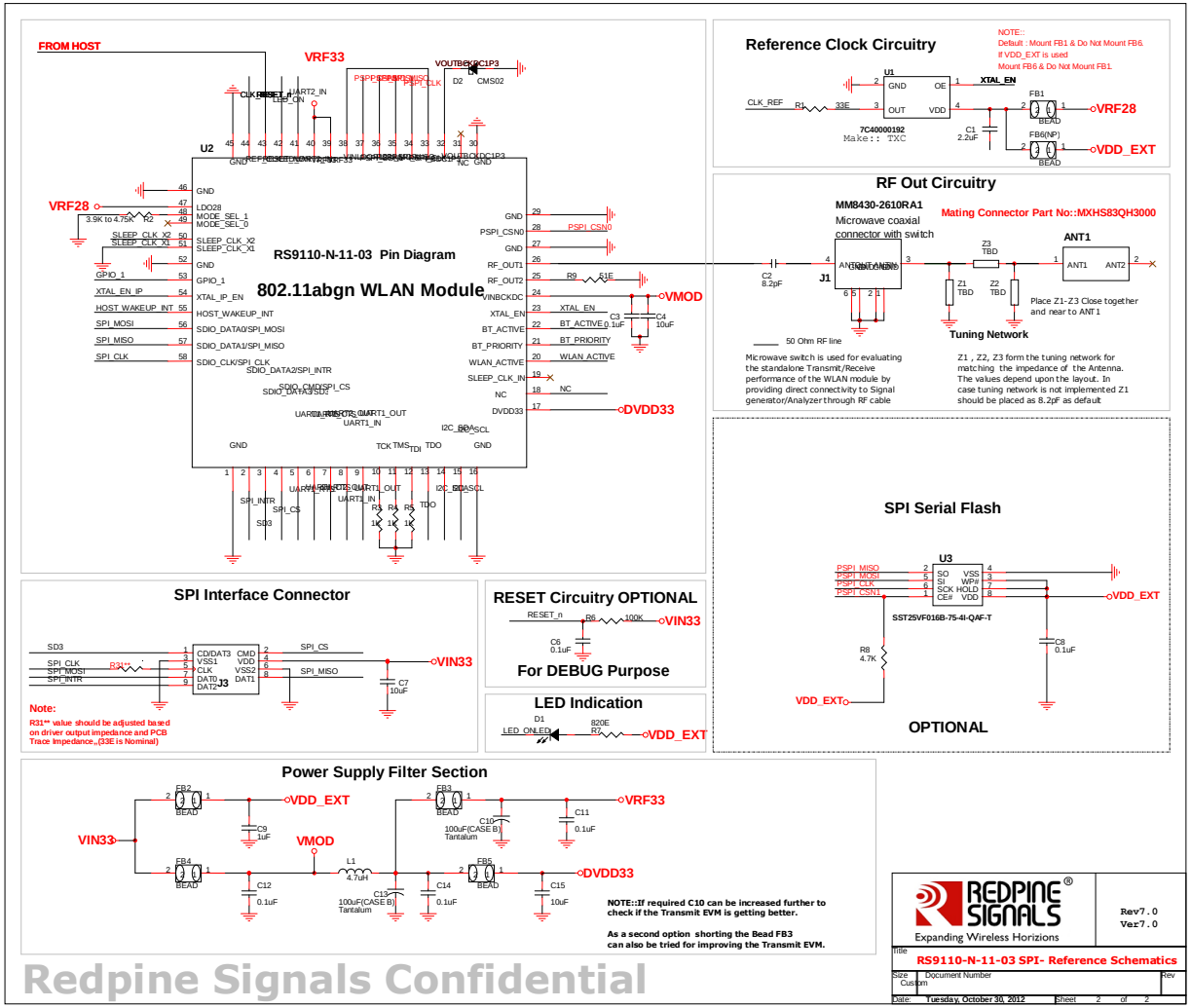

Figure 2 SPI Interface Integration

NOTE on SPI_CS and SPI_CLK: Based on the Host SPI configuration, during BOOT UP, SPI Master could be coming up as GPIO pins. In the wake of this possibility, it may be needed to add a pull up on the SPI_CS and a pull up (CPOL=1)/pull down (CPOL=0) on the SPI_CLK. The value of pull up/ pull down resistor should follow the recommendations as given on the HOST side.

However, a WLAN application that uses the RS9110-N-11-03 module may differ in the following:

1. Antenna connection:
   The 'microwave coaxial connector with switch' shown would not be required.

   The RF_OUT1 (Module Pin No. 26) signals may be directly connected to an on-board chip antenna, or may be terminated in an SMA connector of any form factor for enabling the use of external antennas.

   The RF-OUT2 (Module Pin No. 25) is terminated through 50ohms precision resistor (1% Tolerance) to ground.
2. The LED is optional.

2 Bill of Materials

2.1 SDIO Interface

Item	Qty	Reference	Value	Description	Jedec	Mfg	Part No
CAPACITORS							
1	1	C2	8.2pF	CER CHP C 8.2P +-0.25P C0G 0402 25V LF	0402	Murata	GRM1555C1H8R2CZ01D
2	5	C3,C6,C11,C12,C14	0.1uF	CER CHIP C 0.1U 10% X5R 0402 6.3V	0402	Murata	GRM155R61A104KA01D
3	1	C9	1uF	CAP CER 1.0UF 16V 10% X7R 0805	0805	Murata	GRM21BR71C105KA01L
4	1	C1	2.2uF	CER CHIP C 2.2U 20% X5R 0402 4V	0402	Murata	GRM155R60G225ME15D
5	3	C4,C7,C15	10uF	CER CHIP C 10U 20% X5R 0805 10V	0805	Murata	GRM21BR61A106KE19L
6	2	C10,C13	100uF	CER CHIP C 47U 20% 10V CASE B	CASE-B	Kemet	B45196H2476M209
RESISTORS							
7	2	R1,R31**	33E	CHIP RES 33R 5% 200PPM 0402 1/10W	0402	Panasonic	ERJ-2GEJ330X
8	1	R9	51E	RES 51.0 OHM 1/10W 1% (0402)	0402	Panasonic	ERJ-2GE J510X
9	1	R7	820E	CHIP RES 820R 5% 200PPM 0402 1/10W	0402	Panasonic	ERJ-2GEJ821X
10	3	R3,R4,R5	1K	RES 1.0K OHM 1/16W 5% 0402 SMD	0402	Yageo	RC0402JR-071KL
11	1	R6	100K	CHIP RES 100K 5% 200PPM 0402 1/10W	0402	Panasonic	ERJ-2GEJ104X
INDUCTORS							
12	1	L1	4.7uH	Power Inductor	2520	FDK	MIPF2520D4R7
13	5	FB1,FB2,FB3,FB4,FB5	BEAD	Beads	0805	Murata	BLM21PG221SN
Diodes							
14	1	D1	LED	LED	0603	Lite-On Inc	LTST-C190KGKT
15	1	D2	CMS02	Schottky Diode	SMD	Toshiba	CMS02TE12L,Q
ANTENNA TUNING NETWORK							
16	3	Z1,Z2,Z3	TBD	Refer to the description in the schematic. Sample part number for Z1 given here.		Murata	GRM1555C1H8R2CZ01D
IC'S							
17	1	U1		40MHz Crystal Oscillator		TXC	7C40000192
18	1	U2		RS9110-N-11-03 802.11abgn WLAN Module		Redpine	RS9110-N-11-03
19	1	ANT1	Antenna	2.45GHz &5GHz SMD Antenna		RAINSUN	AN1003

20	2	J1		Microwave Coaxial Connector with switch		Murata	MM8430-2610RA1
21	1	J3		5X2 Box Header		Burg Header	
No Populate							
22	1	C8	0.1uF	CER CHIP C 0.1U 10% X5R 0402 6.3V	0402	Murata	GRM155R61A104KA01D
23	1	R8	4.7K	CHIP RES 4K7 5% 200PPM 0402 1/10W	0402	Panasonic	ERJ-2GEJ472X
24	1	U3		16MBIT Serial Flash	WSON	SST	SST25VF016B-75-4I-QAF-T
25	1	FB6	BEAD	Beads	0805	Murata	BLM21PG221SN

2.2 SPI Interface

Item	Qty	Reference	Value	Description	Jedec	Mfg	Part No
CAPACITORS							
1	1	C2	8.2pF	CER CHP C 8.2P +-0.25P C0G 0402 25V LF	0402	Murata	GRM1555C1H8R2CZ01D
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10	3	R3,R4,R5	1K	RES 1.0K OHM 1/16W 5% 0402 SMD	0402	Yageo	RC0402JR-071KL
11	1	R2	3.9K to 4.7K				
12	1	R6	100K	CHIP RES 100K 5% 200PPM 0402 1/10W	0402	Panasonic	ERJ-2GEJ104X
INDUCTORS							
13	1	L1	4.7uH	Power Inductor	2520	FDK	MIPF2520D4R7
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26	1	FB6	BEAD	Beads	0805	Murata	BLM21PG221SN

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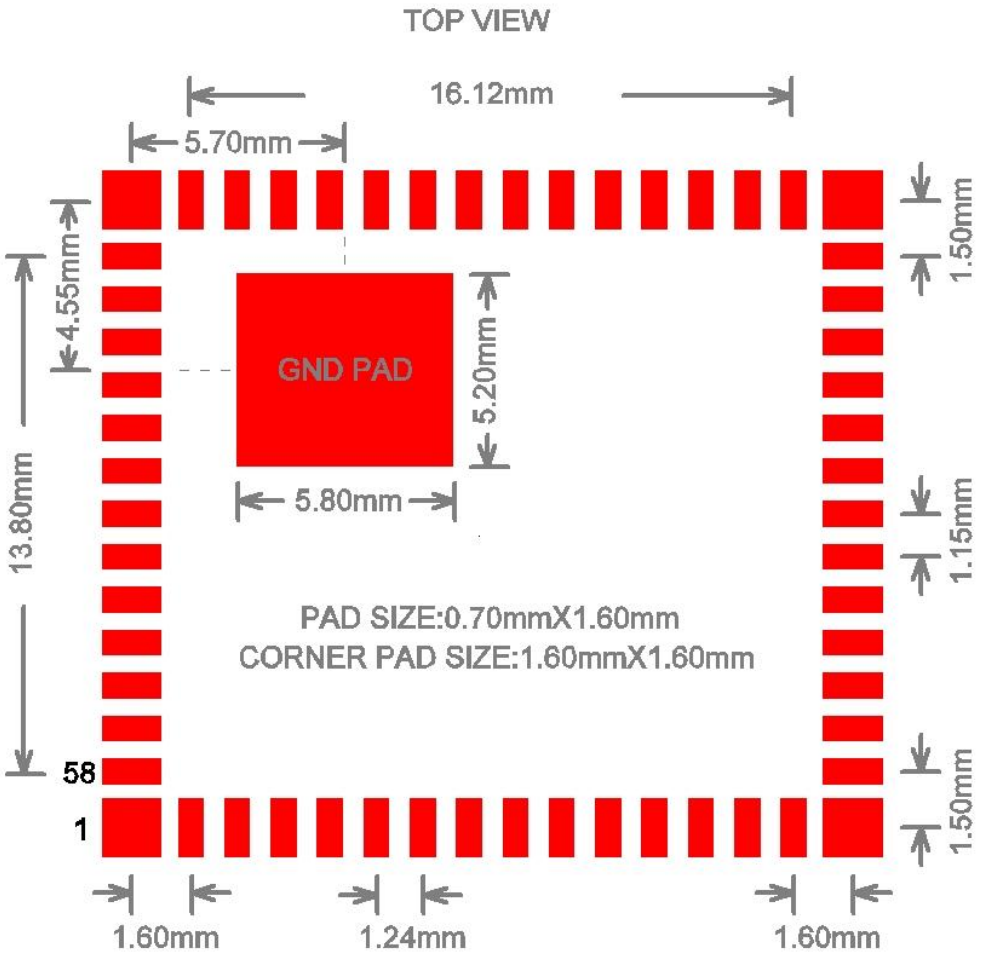
3 Recommended RS9110-N-11-03 PCB Landing Pattern



4 Circuit and Layout Guidelines

The following are guidelines for integrating the RS9110-N-11-03 module into a wireless LAN solution.

1. The WLAN module has a central ground pad of size 5.8mm x 5.2mm. An application's layout must have a provision to include this.
    a. Please provide a 5.,8 mm X 5.2 mm Copper pad on the Top side of the application board. Please open the solder mask in this area so that the Cu is exposed.
    b. Please provide a 5.8 mm X 5.2 mm or higher Copper pad on the bottom side of the application board. Please open the solder mask in this area so that the Cu is exposed.
    c. Please provide at least 20 via's to connect these pads to the Ground plane. We recommend that the via's should be at least 10 mil x 18 mil.
2. For RESET one of the two options should be followed
    a. The RESET can be Host driven. At the time of Power-on, Please ensure that the reset is held low for 20mSec or more. After this the reset should be driven high.
    b. Reset may be driven by an R-C circuit. The recommended value of 'R' is 100 Kohms and the recommended value of 'C' is 0.1uF.
3. The RF trace on RF_OUT should have a characteristic impedance of 50 ohms. They can use any standard 50 RF trace (Microstrip or Coplanar wave guide). The width of the 50 ohms line depends on their PCB stack like the dielectric of the PCB, thickness of the copper, thickness of the dielectric and other factors. Customers should work with their fabrication unit to on these factors.
4. To evaluate transmit and receive performance like Tx Power and EVM, Rx sensitivity etc., a 'microwave coaxial connector with switch' should be placed between RF_OUT and the antenna.
5. CLK_REF is the reference clock to the module and should therefore be routed with minimum trace length and should be routed away from other switching or sensitive traces.
6. The design for embedded system with the Wi-Fi Module should provide for a peak power load of 400mA.

5 Chip Antenna Layout Recommendations

The choice of antenna will depend on the application. However, some recommendation is listed below if an on-chip antenna is desired to be used:

- Rainsun AN1003
- Fractus FR05-S1-NO-1-004

Please make sure that the Cu is etched out in all the Layers in the Antenna region. The Ground plane should be removed from under and both sides of the antenna. Please follow the rules listed in the picture below while doing the layout for the chip Antenna.

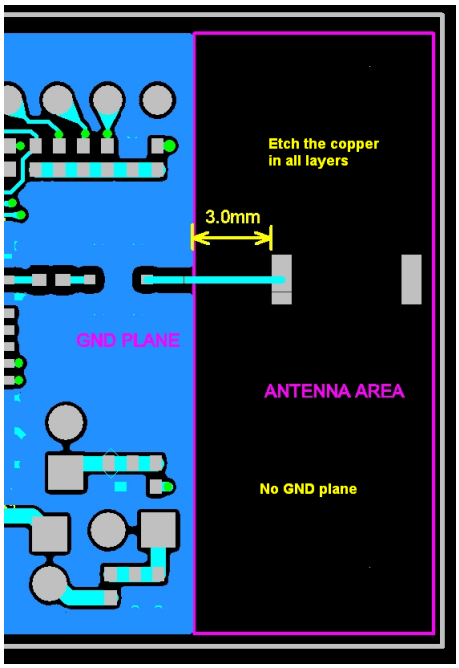


Figure 3 Antenna Layout

The chosen Chip Antennae are λ/4 antennae and would require external ground plane for proper functioning and the length of the ground plane behind the antenna (from the feedpoint of antenna to backwards) should be atleast 1 or 2 inches.

Interms of feedtrace which does not have ground underneath (3mm length), will be resonant part of the antenna and lower its frequency. This can be a useful tuning method although this kind of short trace should have little effect which can be observed on a Network Analyzer. It is recommended to characterize the antenna portion using a Network Analyzer. Electrical performance of any Chip antenna is influenced by the physical characteristics of the surrounding ground plane, feed line, other devices, and materials. This can be used as an advantage by manipulating certain parameters to affect resonant frequency and match:

1. Ground plane configuration
2. Distance from antenna

3. Topology around antenna
4. Feed point transmission line impedance
5. Trace width
6. Trace length
7. Matching Network
8. PCB substrate thickness
9. PCB substrate dielectric constant.

5.1 Antenna Matching Network

Provision should be given for a pie network as shown in the schematics. The values shown below are just for example. The values of the pie network components depends on the Antenna part, Customers layout, Gnd plane in the layout & other components in the system which could affect the radiation pattern of the Antenna. Please use a Network Analyzer to optimize the values of the match network for the best return loss.

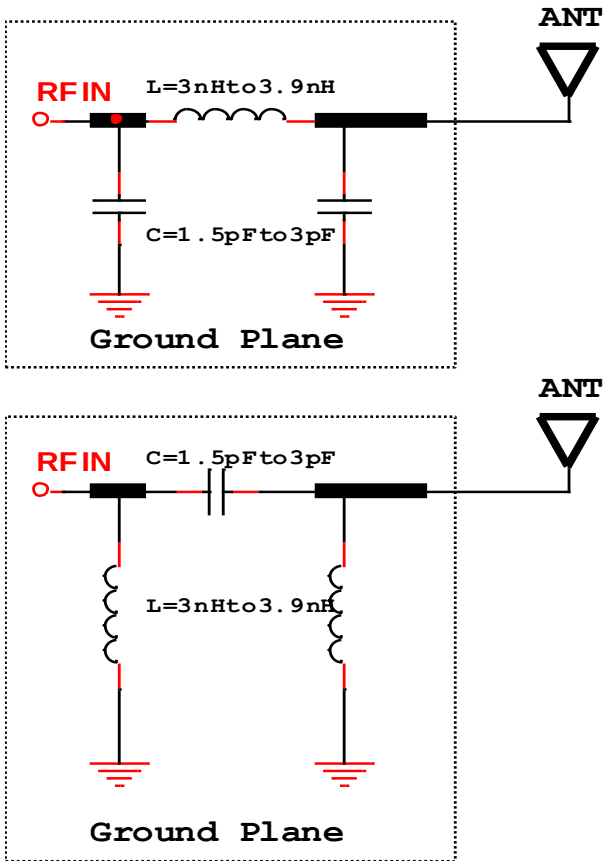


Figure 4 Antenna Matching Network

The radiation pattern of the Antenna can be studied in an Anechoic Chamber using a Network Analyzer & a Horn Standard Gain Antenna

6 Reference Oscillator Specifications

Parameter	Specifications	Units	Comments
Nominal Frequency	40	MHz	
Frequency Accuracy	± 20	PPM	Over operational temperature at rated voltage.
Supply Voltage (V_{DD})	2.8 ± 10% or 3.3 ± 10%	V	Power supply should ideally be locally regulated, and with adequate filtering.
Power Supply PSRR	> 60	dB	
Operational Temperature	-40 to + 85	°C	For industrial grade products.
Output Voltage '0' level	< 10% of V_{DD}	V	
Output Voltage '1' level	> 90% of V_{DD}	V	
Output type	Square Wave		
Duty cycle	45 to 55	%	
Rise time/Fall time	< 10	ns	
Periodic Jitter	30 ps pk-pk	ps	Typical Spec of the Oscillator we use
Wake-up time from Standby	< 1	ms	
Wake-up time from power-on	< 5	ms	
Standby current	< 20	uA	
Active current	< 10	mA	
Output load	> 15	pF	
Phase Noise at offset: 10 Hz 100 Hz 1 kHz 10 kHz 100 kHz	 < -89 < -121 < -135 < -146 < - 150	dBc/ Hz	Typical Spec of the Oscillator we use.

6.1 List of Recommended Crystal Oscillators

1. TXC part number 7C40000192 (This part was used for characterizing all our boards)

The following can also be used based on the specifications

2. Ecera part number FD4000113
3. Fox Xpresso part number FXO-HC538R
4. Kyocera part number KC25200C40C3KE00
5. Tai-Saw Technology part number TW0377E
6. Epson Toyocom SG 150-SCE
7. Epson Toyocom SG 211-SCE
8. Golledge GXO-5332L/E 40.0MHz
9. ECS EC-2532HS

Note: Before finalizing the choice of a crystal oscillator, it is advisable to carry out detailed EVM measurements on a prototype or evaluation board.

7 Recommended Specifications for Schottky Diode

- Forward voltage: VFM = 0.40 V (max)
- Average forward current: IF (AV) = 3.0 A
- Repetitive peak reverse voltage: VRRM = 30 V

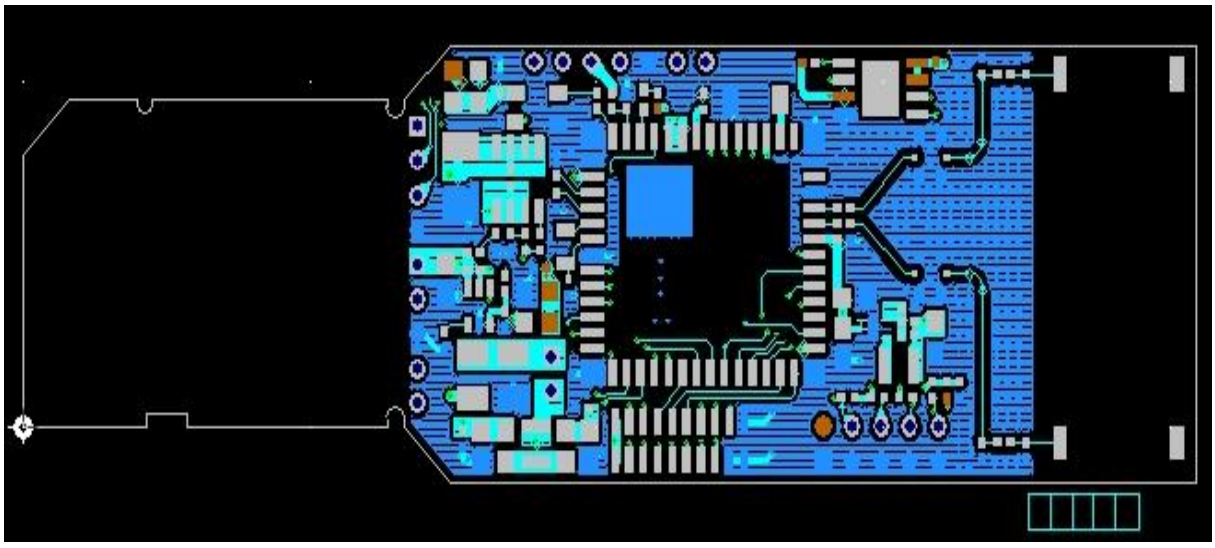
7.1 Recommended Parts

a. Toshiba part number CMS02
b. NXP part number PMEG3030BEP

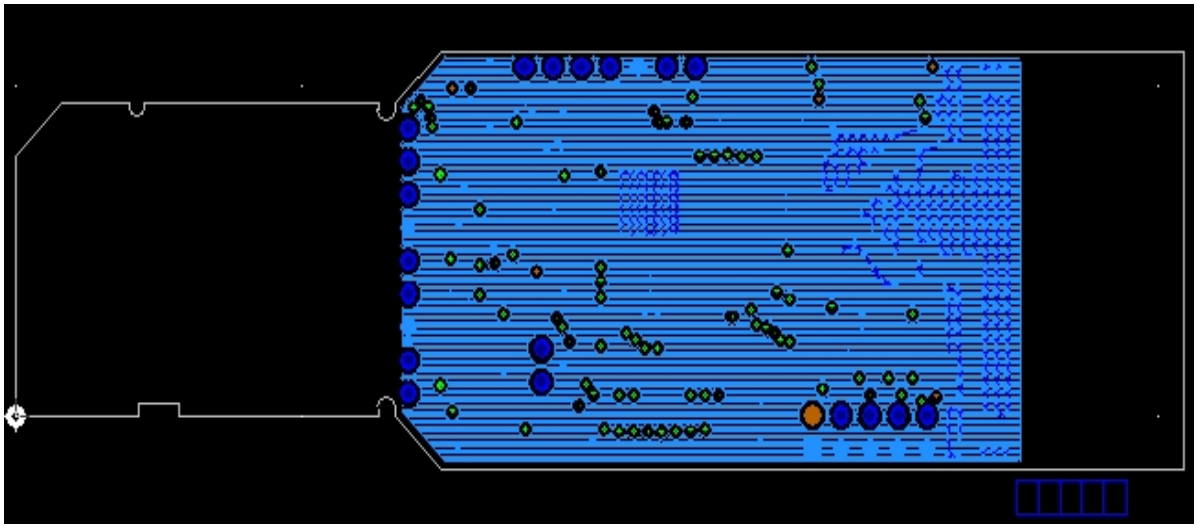
8 Sample Layout

This section provides a sample layout of a board that instantiates RS9110-N-11-03. This reference board is an SDIO module with a standard interface into an SDIO slot.

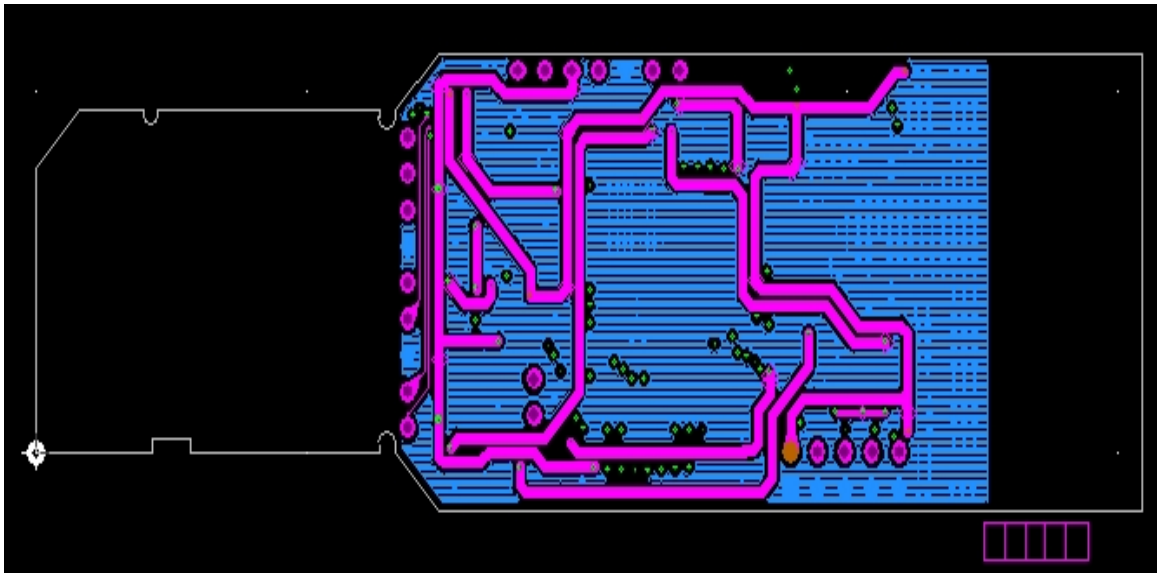
8.1 Top Layer



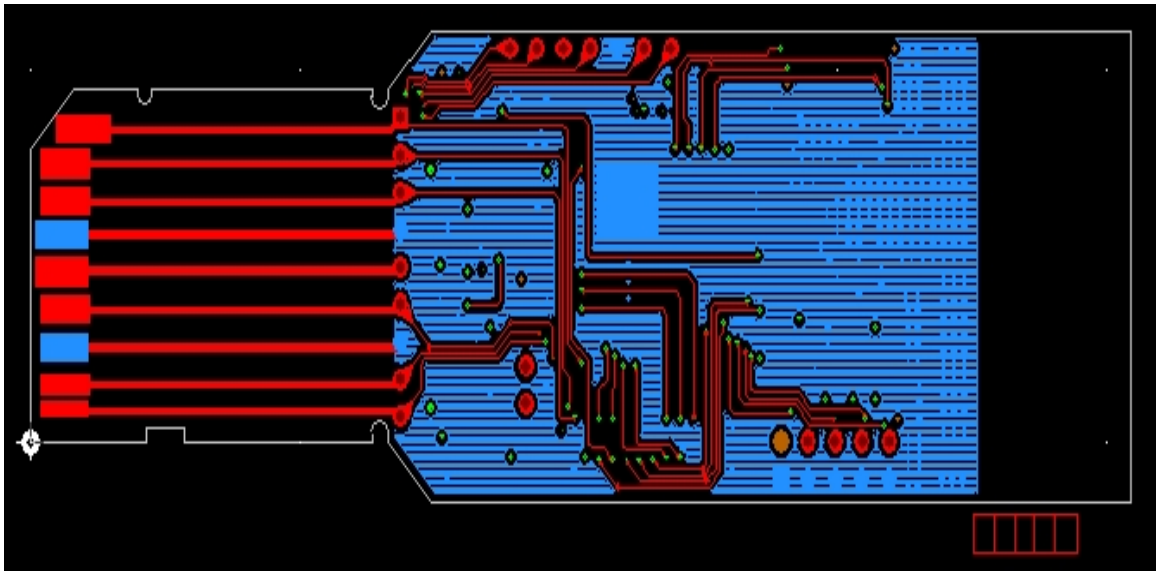
8.2 Layer 2



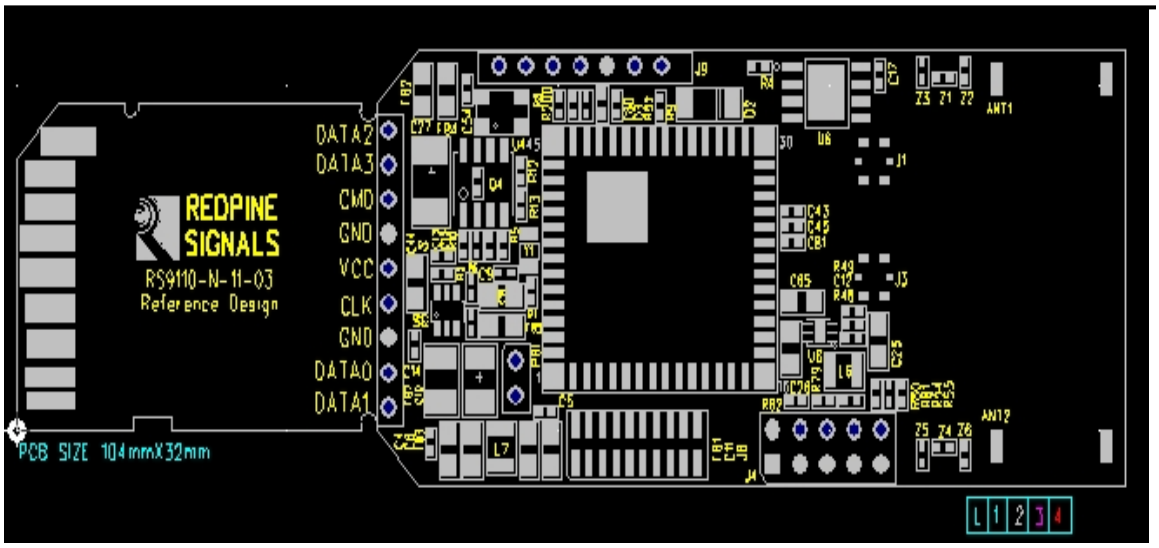
8.3 Layer 3



8.4 Bottom Layer



8.5 Component Placement


DATA2
DATA3
CMD
GND
VCC
CLK
GND
DATA0
DATA1
REDPINE
SIGNALS
RS9110-N-11-03
Reference Design
PCB SIZE 104mmX32mm

Revision History

Revision No.	Version No.	Date	Author	Changes
1	1.0	Dec '08	Suresh	Initial Version. Applicable to module series A01.
2	1.1	Jan '09	Suresh	Introduced NC's. Applicable to module series A01.
3	2.0	Jan '09	Suresh	New layout including the external clamp diode. Applicable to module series B01.
4	2.01	Feb '09	Suresh/Venkatesh	Added PCB landing pattern
5	2.02	May '09	Peddi Indukuri	Updated company logo
6	2.03	July '09	Suresh	Diversity Related Additions
7	2.04	Sep '10	Suresh	Mode_Sel_0 made as NC
8	2.05	Aug '10	Mohan	Updated recommended part numbers
9	2.7	Jan '11	Mohan Vellanki	New schematics and PCB layout pattern Added Reference Oscillator Specifications
10	2.8	Feb'11	Mohan Vellanki	Updated with new schematics
11	2.9	Sep'11	Suresh/Mohan	Updated with comments on antenna usage
12	3.0	Nov, 12	Diganta	Added alternative connection to the crystal VDD