Author: Stephan R. Kurtz

Mixers as Phase Detectors

Most systems which require phase information use mixers somewhere in the measurement or comparison of the phase information. Theoretically, any mixer with a dc coupled port could be used as a phase detector. Practically, however, mixers often display some very non-ideal characteristics (e.g., dc offset) when used as phase detectors. The actual mixer chosen for a particular application will often depend on the degree to which these non-ideal characteristics can be tolerated.

This article discusses the general theory behind the use of mixers as phase detectors; the origin of some of the various non-ideal characteristics and how they can be minimized; some of the factors affecting phase detector response; and finally, some general guidelines to be considered when picking a mixer for a phase detector application.

HOW PHASE DETECTORS WORK

The basic concept upon which phase detection rests is that the application of two identical frequency, constant amplitude signals to a mixer results in a dc output which is proportional to the phase difference between the two signals. While it is true that even a single diode can be used as a mixer, most phase detectors involve the use of double balanced mixers (for reasons to be discussed later). With this in mind, the theory presented here assumes that a double balanced mixer is being used. Figure 1 is a schematic of a typical double balanced, four-diode ring mixer.

The voltage at the secondary of the LO transformer causes currents to flow through diode pair D1, D2 or D3, D4, depending on polarity. The DC voltage at B or C is held at virtual ground potential by the voltage divider action of the conducting diode pair. The diode pairs (D1, D2 and D3 D4) alternate conduction, causing the ends of the RF transformer's secondary winding (B and C) to be alternately at ground potential, switching at a rate equal to the frequency of the input signal to the LO port. The instantaneous voltage at the IF port is determined by: 1) the level and polarity of the instantaneous voltage at the RF transformer' s secondary winding; and 2) which terminal of the secondary is at ground potential at that instant. The output at the IF port contains the sum and difference of the frequencies of the signals input to the LO and RF ports. If the RF and LO signals have identical frequencies, then their difference is zero Hz, or dc, which is the desired output for a phase detector. Their sum, which is twice the input frequency, can be selectively filtered out if it is not already beyond the frequency response of the IF port.

MATHEMATICAL DESCRIPTION

In order to demonstrate mixer operation mathematically, we need to first look at the mixing process as it occurs in each diode. The conductance waveform for the diode can be expressed in terms of the local oscillator frequency and its phase angle as shown below:[2]

$$G(\omega_L t + \Phi_L) = \sum_{n=-\infty}^{\infty} g_n \exp\left(j(n(\omega_L t + \Phi_L))\right) \quad (1)$$

where

$\omega_L \equiv$ frequency of the LO signal

$\Phi_L \equiv$ phase angle of the LO signal

$j \equiv \sqrt{-1}$

$g_n \equiv$ constants.

Applying an RF signal, the small signal voltage across the diode is VRF $(\omega_R t + \Phi_R)$, which results in a diode current waveform of

$$i_D = G(\omega_L t + \Phi_L)\, V_{RF}\, (\omega_R t + \Phi_R) \quad (2)$$

If V_{RF} is expressed as

$$V_{RF}\, (\omega_R t + \Phi_R) = \sum_{m=-\infty}^{\infty} v_m \exp\left(j(m(\omega_R t + \Phi_R))\right) \quad (3)$$

then combining equations (1), (2), and (3) yields

$$i_D = \sum_{n,\, m=-\infty}^{\infty} g_n\, v_m \exp\left(j(n(\omega_L t + \Phi_L) + m(\omega_R t + \Phi_R))\right) \quad (4)$$

In a four-diode ring mixer as shown in Figure 1, the total current seen at the IF port is given by

$$I_{IF} = 1/2\, (i_{D2} - i_{D1} + i_{D4} - i_{D3}) \quad (5)$$

where i_{Dj} is the current flowing through diode j.

Combining equations (4) and (5) gives

$$I_{IF} = \sum_{n,\, m}^{\infty} -2g_n\, v_m \exp\left(j(n(\omega_L t + \Phi_L) + m(\omega_R t + \Phi_R))\right) \quad (6)$$

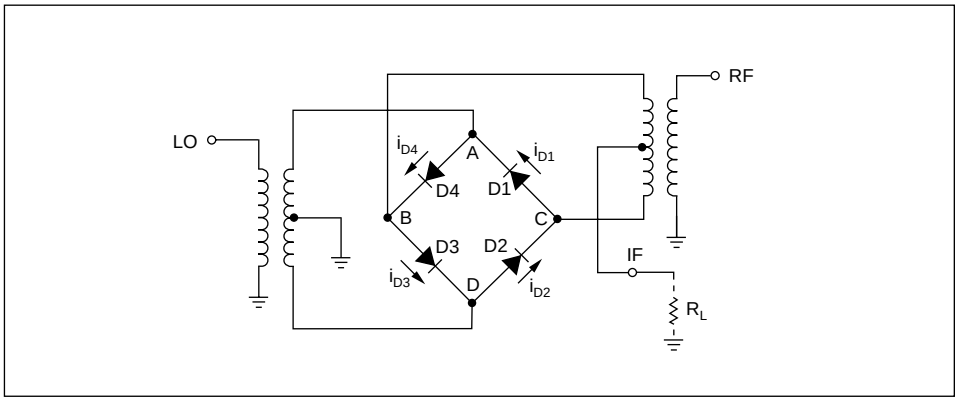

Figure 1. A typical double balanced four-diode ring mixer.

Author: Stephan R. Kurtz

where n, m = all odd integers.

All terms in equation (6) other than those for n × m = -1 represent unwanted intermodulation products and must be filtered out if not already sufficiently attenuated by the frequency response of the IF port.

In a phase detection application ω_L is equal to ω_R which results in a current at the IF port (looking only at the n × m = - 1 terms) of

$$I_{IF} = -2g_{\pm 1}\, v_{R\mp 1} \exp\left(j(n(\pm\omega_L t \mp \omega_R)\right). \quad (7)$$

Assuming a load resistance R, if we rewrite the exponential in equation (7) in trigonometric form, keeping only the real part, the result is

$$V_{IF} = -2Rg_{\pm 1}\, v_{R\mp 1} \cos\left(\pm\Phi_L \mp \Phi_R\right) \quad (8)$$

or

$$V_{IF} = -2Rg_{\pm 1}\, v_{R\mp 1} \cos\left(\Delta\Phi + \pi\right) \quad (9)$$

which indicates that the voltage at the IF port will be dc and will vary as the cosine of the phase difference between the LO and RF signals. Null readings for V_{IF} are thus obtained whenever the phase difference ΔΦ between the LO and RF signals is equal to nπ/2 with n = ±1, ±3, ..., while maximum and minimum readings are obtained for ΔΦ = nπ where n = 0, ±1, ±2, ...

PEAK OUTPUT, SENSITIVITY, AND LINEARITY

Figure 2 shows V_{IF} varying as the cosine of the phase difference ΔΦ between the LO and RF signals, with maximum negative voltages occuring at ΔΦ = 0 and maximum positive voltages occuring at ΔΦ = π. While that is the most common form of phase detector output, it is also possible to obtain maximum positive voltages at ΔΦ = 0 and maximum negative voltages at ΔΦ = π by means of relatively minor internal wiring changes to the mixer.

The response of V_{IF} to changes in ΔΦ is fairly linear over the region in phase space corresponding to

$$\Delta\Phi = \pi/2 + \delta\Phi.$$

It is in this pseudo-linear response region that the sensitivity of the phase detector to changes in ΔΦ (i.e., $dV_{IF}/d\Delta\Phi$) is maximum. However, as seen in Figure 2, the actual value of this maximum sensitivity is strongly affected by changes in the maximum voltages seen at ΔΦ equal to 0 or π.

Assume that the phase detector output is described by

$$V_{IF} = V \cos\left(\Delta\Phi + \pi\right) \quad (10)$$

where V is the amplitude of the maximum voltage seen at ΔΦ = 0 or π. Now superimpose a straight line on top of V_{IF} which passes through the point (π/2, 0) i.e.,

$$V_2 = A\left(\Delta\Phi - \pi/2\right). \quad (11)$$

In order for V_2 to be approximately equal to V_{IF} over the linear response region, it must follow that the slope of V_{IF} and V_2 are equal at ΔΦ = π/2. Thus, equation (11) can be rewritten as

$$V_2 = V\left(\Delta\Phi - \pi/2\right) \quad (12)$$

which indicates that within the linear response region, phase detector sensitivity varies linearly with maximum output voltage.

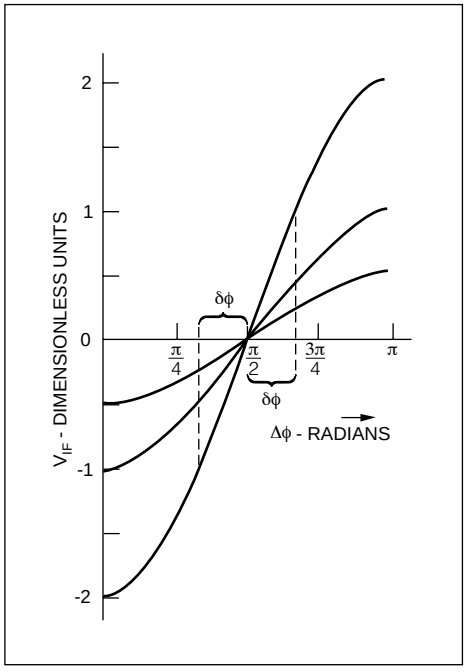

Figure 2. Typical phase detector response curve varies as cos (ΔΦ + π). Detector response is fairly linear over ΔΦ = π/2 + δΦ. Detector sensitivity increases as maximum V_{IF} increases.

The question now remaining is: What exactly is the range of linear response, i.e., what is ΔΦ? Of course, V_{IF} and V_2 are never exactly equal except at ΔΦ = π/2, and so the response is only approximately linear. Thus, the above question should more correctly be: What is the range around ΔΦ = π/2 that the percentage deviation of V_{IF} from linearity will be less than or equal to d, where

$$d = \left(\frac{V_2 - V_{IF}}{V_2}\right) 100. \quad (13)$$

Substituting equations (10) and (12) into (13) and evaluating at

$$\Delta\Phi = \pi/2 + \delta\Phi^*$$

results in

$$d = \left(\frac{\delta\Phi - \sin\delta\Phi}{\delta\Phi}\right) 100. \quad (14)$$

If we now expand sin ((in a power series and keep only the first two terms in the series, we get

$$d = \left(\frac{\delta\Phi^2}{3!}\right) 100. \quad (15a)$$

or

$$\delta\Phi = \sqrt{\frac{6d}{100}} \quad (15b)$$

where δΦ is in radians. Figure 3 plots equation (15a) versus both δΦ and ΔΦ. The range of linear response is thus seen to depend on how much deviation from linearity can be tolerated. For example, if a 10% deviation from linearity can be tolerated, then the linear response region will extend approximately from ΔΦ = 45° to 135°; i.e., δΦ = ±45°.

NONIDEAL CHARACTERISTICS

The theory presented in the previous section assumed an "ideal" mixer, i.e., the circuit was perfectly balanced. However, this is often not possible or practicable, with the

*Evaluation at ΔΦ = π/2 - δΦ would simply result in a value of -d.

Author: Stephan R. Kurtz

result that when practical mixers are used as phase detectors they often display some characteristics which differ from those of idealized mixers.

The characteristics of most interest are dc offset and/or mixer-induced phase shift of the signals due to circuit imbalance. The design engineer is interested in how these characteristics may change as various elements affecting mixer performance are changed (e.g., frequency, LO and RF drive levels, load resistance, and temperature).

DC OFFSET

Theoretically, when $\Delta\Phi$ is equal to $\pi/2$, the dc voltage measured at the I port of the phase detector should be zero. DC offset is the deviation from 0 Vdc that is seen when $\Delta\Phi = \pi/2$. If only one signal (LO or RF) is applied to the mixer, the dc offset is then simply the dc component of that portion of the applied signal which is measured at the I port, implying that dc offset is inversely related to isolation. The impact of a non-zero dc offset voltage is shown in Figure 4. Both the actual phase angle at which a null reading is obtained and the minimum and maximum voltages at the I port are affected.

The origin of dc offset voltages is a combination of diode imbalance and transformer asymmetry and can come from either or both input signals. Let us consider now the case for which only the LO signal is applied to the mixer. If the LO transformer is perfectly symmetrical on either side of the center tap, then at any instant in time, the voltage V_{LO} at point A is exactly equal in magnitude (although opposite in polarity) to that applied at point D (see Figure 1). The voltage drop from B to C, and, consequently, the voltage that will be at the RF and IF ports, is determined by the degree of diode balance in the circuit. With only an LO signal applied, the circuit in Figure 1 is basically an ac bridge. Thus, in order to have zero voltage drop from B to C, the following condition must hold:

$$Z_{D1}\, Z_{D3} = Z_{D2}\, Z_{D4} \qquad (16)$$

where Z_{Dj} is the complex impedance of diode j. Equation (16) requires that each diode have the same v,i curve and that the stray capacitance and inductance on each side of the bridge also be matched. The impossibility of ever perfectly satisfying equation (16) is reflected by the fact that no mixer has infinite isolation.

The effect of transformer asymmetry can be shown if it is assumed that somehow equation (16) has been perfectly satisfied but that now the LO transformer is not perfectly symmetrical with respect to the center tap. Satisfying equation (16) only guarantees that the voltage at B is the same as that at C. However, it does not guarantee that the voltage at B and C is equal to that at the center tap of the LO transformer. Suppose that the transformer is asymmetrically wound so that 1.1 V_{LO} is applied to point A and -0.9 V_{LO} is applied to point B (i.e., the center tap is at a voltage of +0.9 V_{LO} with respect to ground). The total voltage drop across diode pairs D1, D2 and D3, D4 will be $2V_{LO}$. If the diodes are perfectly balanced, the voltage at points B and C will be V_{LO} with respect to ground. The I-port connects points B and C to the center tap of the LO transformer through a load resistor. There is thus a dc voltage of 0.1 V_{LO} that will be seen across this load resistor due to the transformer asymmetry alone.

MINIMIZING DC OFFSET

If the dc offset is known, its effect can be negated, or at least minimized, by simply applying an appropriate dc bias to the I port. Of course, the ideal way to minimize the effect of dc offset voltage is to select a mixer having minimum dc offset in the first place. But, most mixer data sheets do not provide this information. They do, however, provide isolation information which can be used to get a rough approximation of the dc offset. This follows from the fact that dc offset is simply the dc component of that portion of the applied LO (or RF) signal which is seen at the I port. For example, if a signal is applied to the L port at a power level of LO dBm, the power in dBm dissipated in a 50-ohm load at the I port is

$$IF = LO - IS \qquad (17)$$

where IS is the L-to-I isolation expressed in db. Expressing the power at the I port in watts we get

$$P_{IF} = 10^{\left(\frac{IF}{10}-3\right)} = 10^{\left(\frac{LO-IS}{10}-3\right)} \qquad (18)$$

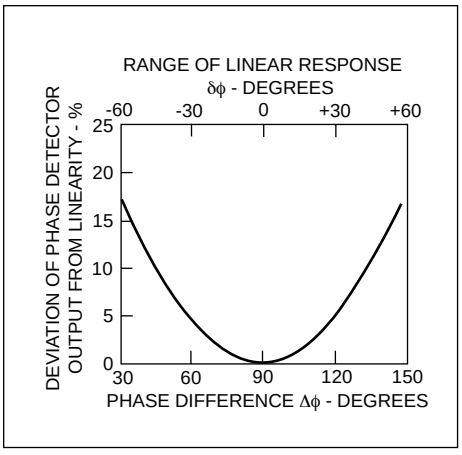

Figure 3. Phase detector output is a pseudo-linear function of phase difference.

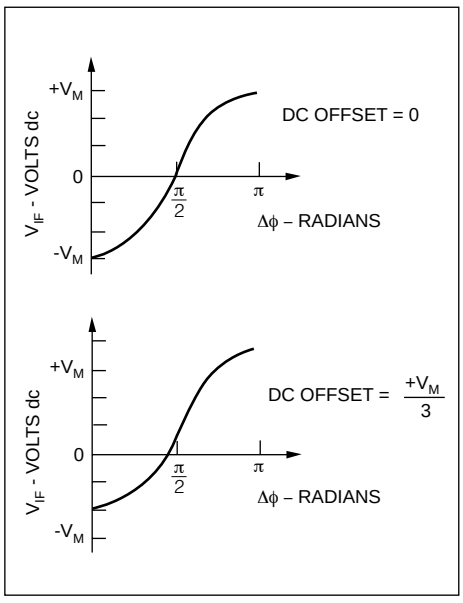

Figure 4. Non-zero dc offset voltage affects both the value of $\Delta\Phi$ at which a null reading is obtained and the voltage measured for any given $\Delta\Phi$.

Author: Stephan R. Kurtz

If we assume a 50Ω load resistance, we can calculate that the magnitude of the voltage measured at the I port must be

$$V_{IF} = \sqrt{50\ P_{IF}} = (50)^{1/2}\ 10^{\left(\frac{LO - IS - 30}{20} - 3\right)} \quad (19)$$

The average, or dc, value of the I port voltage (in volts) is given by $2/\pi\ V_{IF}$; thus,

$$V_{DC} = 2/\pi\ (50)^{1/2}\ 10^{\left(\frac{LO - IS - 30}{20} - 3\right)} \quad (20a)$$

or, more simply,

$$V_{DC} = (4.5)\ 10^{\alpha} \quad (20b)$$

where

$$\alpha = \frac{LO - IS - 30}{20}$$

Although equation (20) makes no reference to the polarity of the dc offset, it can be used to get a rough idea of the magnitude of the offset voltage. It is also useful in estimating the effects of changes in LO drive level and/or isolation (see Table I). Figure 5 compares the results of equation (20) with data taken on three separate diode mixers. It is seen that the magnitude of the offset voltage at any given frequency can differ from unit-to-unit of the same mixer. This is because the isolation is not identical between the units. Using typical isolation values for this model mixer, equation (20) gives results consistent with the spread of data from the three mixers. Using guaranteed isolation values, equation (20) gives the maximum dc offset voltage that would be expected for such a device. This is also shown in Figure 5. The jagged nature of the data in Figure 5 is due to the fact that the L-to-I isolation is not really a smooth function of frequency.

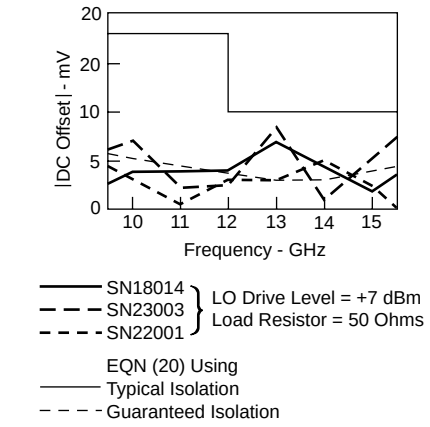

Figure 5. Magnitude of dc offset voltage as a function of frequency for three different WJ-M14A mixers. Also shown are results from equation 20 when typical and guaranteed isolation values for the M14A are used.

Figure 6 shows the effect of varying the LO drive level upon dc offset voltage for typical diode mixers.

In addition to isolation and LO drive level, dc offset is also affected by load resistance and temperature. Figure 7 shows that increasing the load resistance of the I port of a mixer results in an increase in dc offset. This effect is most pronounced for initial increases above 50 ohms and can be explained because a mixer used as a phase detector is acting as a current source. Thus, increasing the load impedance results in a larger voltage drop across the load. Also, increasing the load impedance upsets the isolation of the mixer. Mixer isolation is specified for (and measured with) the I port terminated into 50 ohms. Any other load resistance results in part of the output being reflected back into the mixer, thereby upsetting its balance.

Figure 8 shows that variations and temperature also affect dc offset voltage.

Temperature affects dc offset by virtue of its

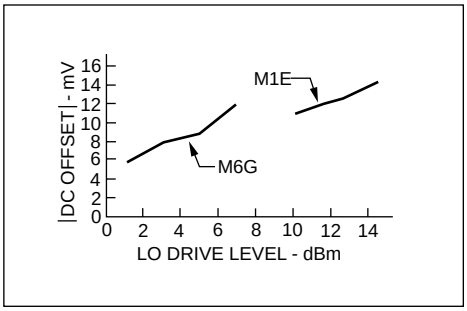

Figure 6. Magnitude of dc offset as a function of LO drive level of the WJ-M1E and M6G mixers. (Data on the M1E mixer were taken at a frequency of 210 MHz, with a load resistance of 1000Ω. Data on the M6G mixer were taken at a frequency of 1.5 GHz, with a load resistance of 50Ω.)

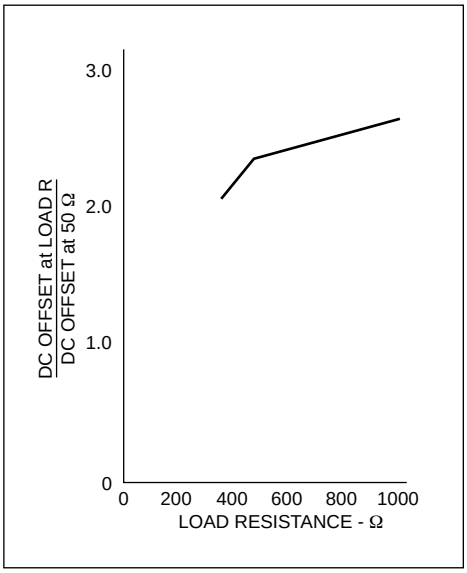

Figure 7. Increasing load resistance affects dc offset. (Data shown were taken using a mixer at a frequency of 210 MHz and an LO drive level of +14.6 dBm.)

		LO DRIVE LEVEL - dBm						
		0	+3	+7	+10	+13	+17	+20
ISOLATION - dB	15	25.3	35.8	63.7	90.0	127.1	226.0	319.2
	20	14.2	20.1	35.8	50.6	71.5	127.1	179.5
	25	8.0	11.3	20.1	28.5	40.2	71.5	100.9
	30	4.5	6.4	11.3	16.0	22.6	40.2	56.8
	35	2.5	3.6	6.4	9.0	12.7	22.6	31.9
	40	1.4	2.0	3.6	5.1	7.1	12.7	17.9
	45	0.80	1.1	2.0	2.9	4.0	7.1	10.1
	50	0.45	0.64	1.1	1.6	2.3	4.0	5.7

Table I. DC offset voltage in millivolts for various combinations of LO drive level and isolation.

Author: Stephan R. Kurtz

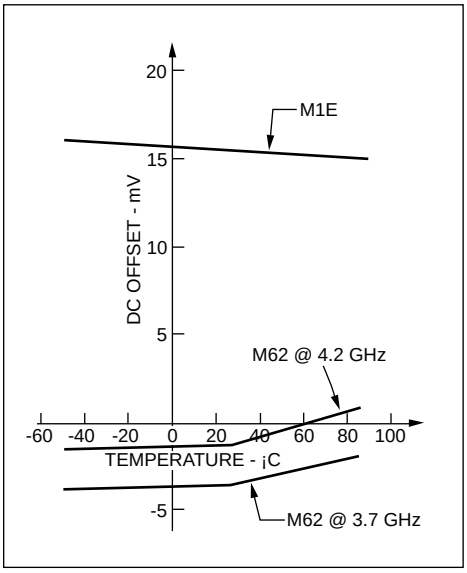

Figure 8. Changing temperature affects dc offset. (Data on the WJ-M1E mixer were taken at a frequency of 210 MHz, and LO drive level of +14.6 dBm, and a load resistance of 1000Ω. Data shown for 3 different units. These data were taken using an LO drive level of +6 dBm and a load resistance of 50Ω.)

effect upon the conductance characteristics of the diodes. As each diode reacts differently to the temperature change, the balance of the mixer is upset and, as a result, isolation changes.

MIXER-INDUCED PHASE SHIFT

Even after the effects of dc offset have been minimized, it is still possible that a null reading will be obtained at some relative phase other than π/2. This is because the mixer itself may change the relative phase of the two input signals; i.e., signals input at a relative phase difference ΔΦ may produce a dc output voltage at the I port corresponding to a relative phase ΔΦ + Θ. This incremental phase shift Θ results from the fact that the electrical length from the L-to-I port is not identical to that from the R-to-I port. Some mixers are purposely designed with nonsymmetrical circuits in order to couple and match the diodes and to provide the correct impedance matching to the R and L ports. These circuit asymmetries result in a different phase shift being imposed on the LO signal than that which is imposed on the RF signal. Figure 9 shows the effect of a mixer-induced phase shift on the phase detector output. Both the actual phase angle at which a null reading is obtained and the voltage seen at any give ΔΦ are affected by mixer induced phase shifts. The minimum and maximum voltages seen at the I port are not affected, however.

MINIMIZING MIXER-INDUCED PHASE SHIFT

Just as for dc offset, most mixer data sheets do not provide any information with respect to mixer-induced phase shift Θ. Unfortunately, unlike dc offset, Θ is not easily related to any of the standard mixer parameters which are reported. The design engineer thus has no guidance whatsoever as to which mixer to use in order to minimize Θ. The best he can do is specify a mixer with as symmetric a circuit layout as possible and then measure Θ once he has the mixer in hand. Minimizing the effects of Θ are relatively simple once the value of Θ is known. All that is required is that the electrical lengths of the lines leading to the L and R ports be adjusted appropriately to compensate for the different electrical lengths from the L-to-I ports and the R-to-I ports.

Figure 10 shows data taken on a mixer in

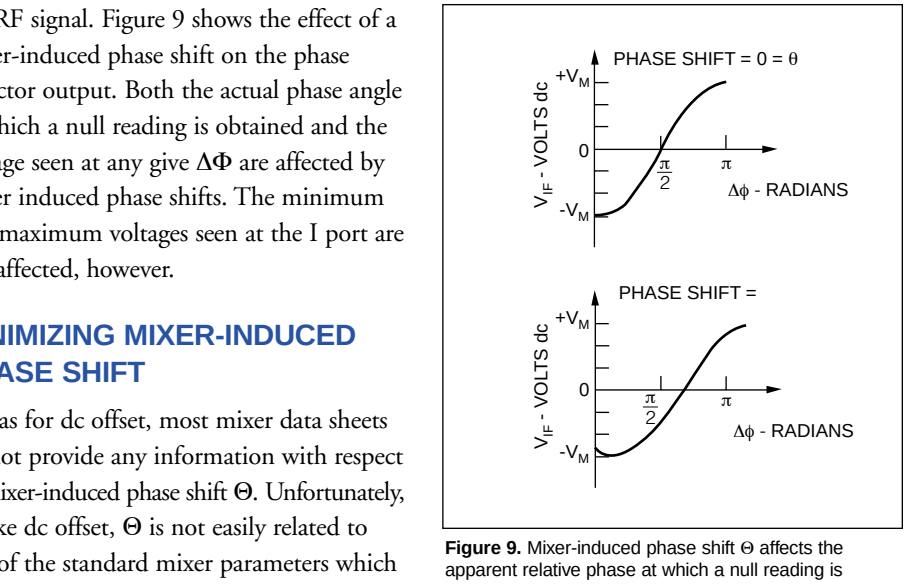

Figure 9. Mixer-induced phase shift Θ affects the apparent relative phase at which a null reading is obtained. Minimum and maximum voltages are not affected, however.

which the effects of both dc offset and mixer induced phase shift are evident. The data as originally taken would indicate a null output voltage at ΔΦ equal to 164°, a maximum positive voltage of +73 mV at 258° and a maximum negative voltage of -64 mV at 78°.

These results obviously do not agree with the theoretical performance described earlier in this article. The dc offset can be obtained by taking one half of the difference between the magnitudes of the maximum output

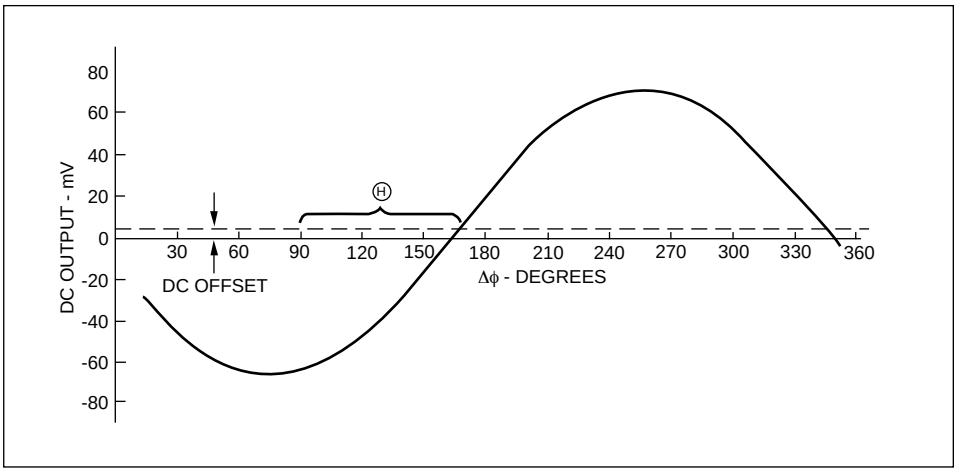

Figure 10. Data on dc output vs taken on a diode mixer demonstrates the effects of both dc offset and mixer-induced phase shift. The dashed line shows the effect of the dc offset. (Data were taken using a frequency of 1.5 GHz, an LO drive level of +6 dBm, an RF level of -9 dBm, and an IF load of 50.

Author: Stephan R. Kurtz

voltages; i.e., dc offset = 1/2 (|+73| - |-64|) = +4.5 mV. If the horizontal axis is shifted upward by 4.5 mV the data would now indicate a null reading at ΔΦ equal to 168°, a maximum positive voltage of +68.5 mV at 258° and a maximum negative voltage of -68.5 mV at 78°. The locations of the null and maximum output readings are all shifted from their theoretical locations by the mixer-induced phase shift of 78°. This indicates an electrical path length difference of 3.52 cm (i.e.,

$$\delta 1 = \frac{\Theta}{360} \times \frac{c}{f} = \frac{78°}{360°}\left(\frac{3 \times 10^{10}\ \text{cm/sec}}{1.85 \times 10^{9}\ \text{cycles/sec}}\right)$$

= 3.52 cm). Increasing the length of the line leading to the R port by 3.52 cm and applying two signals 90° out of phase resulted in a null reading, just as theory would predict.

FACTORS AFFECTING PHASE DETECTOR RESPONSE

When a mixer is used in a phase detector application, all of the standard rules and precautions for mixer use are still in effect. Thus, even after the nonideal characteristics and their effects have been minimized, the design engineer still must concern himself with how variations in frequency, drive levels, load and temperature will influence the mixer's response as a phase detector.

FREQUENCY

The frequency must be within the bandwidths of the L and R ports. More subtle effects of frequency include its influence upon dc offset, upon maximum output voltage and upon the detector's sensitivity to changes in phase angle.

Frequency affects dc offset by virtue of its effect upon isolation as shown in Figure 5. It changes maximum output voltage and sensitivity by virtue of its effect upon conversion loss. Assuming that the LO signal is of a level sufficient to completely turn on the diodes and assuming infinite L-to-I isolation, the output signal level V_{IF} will be essentially equal to the RF signal level minus the conversion loss. Thus, as conversion loss decreases, maximum output voltage increases. And, as shown previously, this results in increased sensitivity of the phase detector to changes in ΔΦ near π/2.

DRIVE LEVELS

Drive levels of the signals applied to the L and R ports must be within the specified limits for the mixer being used. The LO signal must be of a level sufficient to turn on the diodes while the RF signal should be below the 1dB compression point. Again, this much is basic. Of more interest is how varying the LO and/or RF signal levels within the above specified limits will affect the output of the phase detector.

Normally, the LO signal level is sufficiently high to completely turn on the mixer. This results in variations in LO signal level having a relatively minor effect on output voltage. Figure 11 bears this out with data taken two types of diode mixers. It also must be kept in mind that variations in LO drive level can affect the dc offset of the phase detector. This follows directly from equation (20) and was shown in Figure 6.

If it is assumed that the LO signal has completely turned on the mixer, then the output signal level will be the RF signal level minus the conversion loss. This is valid until compression begins to take place. Figure 12 shows how the output of diode mixer is affected by variations in RF drive level. The data in Figure 12 corresponding to the RF = +25 dBm curve represent output taken with an RF level above the 1 dB compression point. This is a possible and often desirable mode of phase detector operation. Increasing the RF level above the 1 dB compression point does produce an increase in maximum output voltage. And, it is again noted that anything which affects the maximum output voltage also affects the sensitivity of the phase detector.

IF LOAD

Most double balanced mixers are designed to operate in a 50-ohm system and the I port expects to work into a 50-ohm load impedance. However, many dc and low frequency impedance levels are much higher than 50 ohms. In Figures 13 and 14 we show the effects of varying the load resistance on phase detector output. The results can be

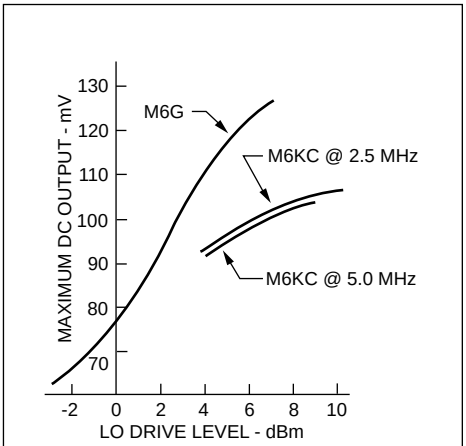

Figure 11. Maximum dc output voltage increases as LO drive level increases. (Data on the WJ-M6G were taken at 1.5 GHz using an RF level of -3 dBm, and a load resistance of 50Ω. Data on the WJ-M6KC were taken at frequencies of 2.5 and 5.0 MHz using an RF level of 0 dBm, and a load resistance of 50Ω.

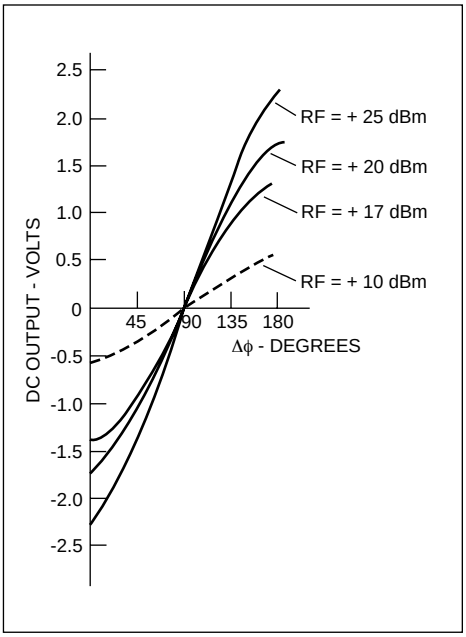

Figure 12. Increasing the RF level increases the maximum output voltage. (Data were taken at 30 MHz using an LO level of +27 dBm, and a load resistance of 50Ω.)

Author: Stephan R. Kurtz

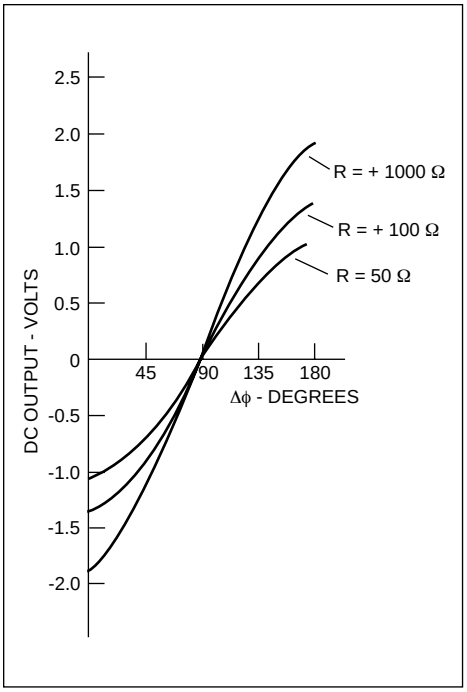

Figure 13. Increases in load resistance result in increased maximum output voltage. (Data were taken at a frequency of 30 MHz using an LO drive level of +27 dBm, and RF level of +17 dBm.)

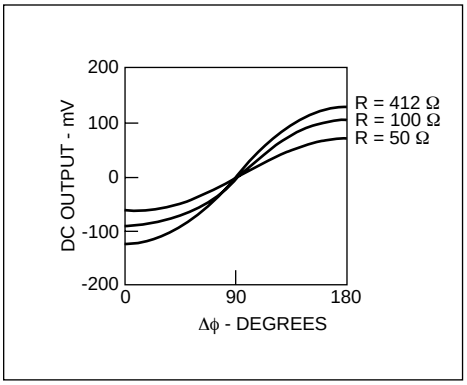

Figure 14. Increases in load resistance result in increased maximum output voltage. (Data were taken on a WJ-M6G mixer at a frequency of 1.85 GHz using an LO level of +6 dBm, and an RF level of -9 dBm. Increasing load from 412Ω to 825Ω did not appreciably change the results.

summarized by noting that as load resistance increases, so does peak output voltage. As in the case of dc offset, this effect is explained by the fact that a mixer used as a phase detector acts as a current source. And, again, increasing the peak output voltage increases the sensitivity of the phase detector.

Varying the temperature of the environment in which the phase detector is being used primarily affects the conductance characteristics of the diodes. These effects are reflected by variations in the mixer's isolation and conversion loss characteristics. Figure 8 shows the effect of temperature variation upon dc offset voltage. Figure 15 shows the effect of temperature variation upon phase detector output voltage.

SELECTING THE RIGHT MIXER

This section presents some general guidelines which can be followed when selecting a mixer for use as a phase detector. For any particular application, more than one mixer may satisfy the given guidelines; or one or more of the guidelines may need to be violated.

SINGLE VS DOUBLE BALANCE

In principle, any mixer with a dc coupled port (even a single diode) can be used as a phase detector. In practice, phase detectors are most commonly double balanced mixers. The reason behind this is that double balanced mixers often have better isolation characteristics (and better dc offset) than do single balanced mixers. This is particularly

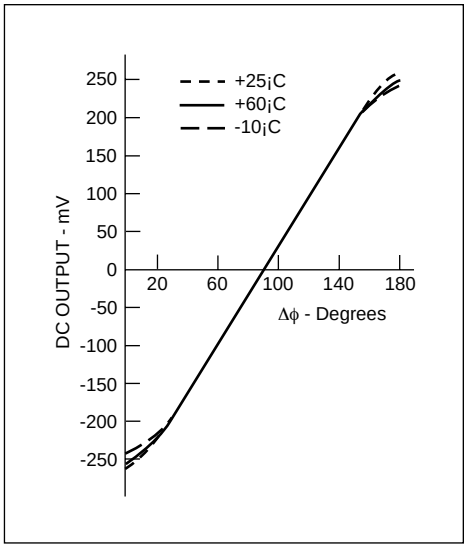

Figure 15. Effects of temperatre variation on phase detector output. (Data using an LO level of 0 dBm, an RF level of 0 dBm, a load resistance of 1000Ω, and a frequency of 14,258 MHz.)

true at low frequencies. Another benefit offered by double balanced mixers over single balanced mixers is that fewer undesired frequencies are appearing at the I port.[3]

LOW LEVEL VS HIGH LEVEL

The choice as to whether a low or high level mixer needs to be used is often dependent upon the specific application being considered. A couple of points are worth mentioning.

First, high level mixers have inherently more complex circuits than do low level mixers (see Figure 16).[1] Low level mixers are of a Class I type, typically having only a single diode in each leg. High level mixers are of either Class II or Class III and have multiple elements in each leg. Class II, Type I mixers have two diodes in each leg; Class II, Type 2 mixers have a series precision resistor and a diode in each leg; and Class III mixers have a capacitor in parallel with a series resistor and a diode in each leg. The result of this increased complexity in high level mixers is that they are more difficult to balance. This can result in lower isolation and higher dc offset and mixer-induced phase shift.

A second point to keep in mind is that at any given frequency, it is common that there will be available a smaller selection of high level mixers than low level mixers. This is particularly true at higher frequencies (i.e., ≥ 1 GHz). An option to be kept in mind then, is to attenuate the incoming signals and use a low-level mixer to compare their phases.

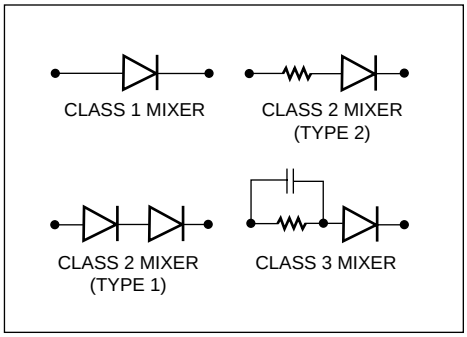

Figure 16. The various classes of mixers have different elements.

Author: Stephan R. Kurtz

LOW FREQUENCY VS HIGH FREQUENCY

As with signal level, the frequency of the incoming signal is dependent upon the specific application being considered. In principle, there is no reason why a microwave mixer should behave any differently than a low frequency mixer when used as a phase detector. In practice, however, there are a few facts worth considering.

First, as frequency increases, the number of mixers available to select from decreases. Second, as frequency increases, isolation decreases and as a result, dc offset increases. This follows from the fact that as frequency increases, wiring capacitance, transformer winding capacitance, and physical location of components all act to upset the balance of the mixer. An option to be kept in mind that would minimize these problems would be to downconvert the incoming signals before comparing their phase.

DISCRETE VS QUAD

Whether it is better for a mixer to use discrete diodes or a monolithic quad depends on the specific application. A quad will offer better temperature stability than will discrete diodes. A quad also offers excellent circuit balance because the diodes in the quad all come from the same silicon chip and have the same conductance characteristics. However, at low frequencies, it is possible to select discrete diodes so that their balance is superior to that of a quad.

GENERAL GUIDELINES

Shown below are some general rules-of-thumb to be followed when selecting a mixer for a specific phase detector application:

1) Determine whether a high or low level mixer is needed. High level means the total combined input power is above +10 dBm.

2) Select those mixers of the appropriate level whose bandwidth is such that the frequency range over which phase detection is to take place lies well within the bandwidth. This follows from the fact that it is desirable to maximize isolation (in order to minimize dc offset) and minimize conversion loss (in order to maximize the sensitivity of phase response). Both of these characteristics are degraded near the ends of the bandwidth. Deviations from this rule may be possible when specific data on isolation and conversion loss vs frequency is available for the frequency range in question.

3) From the group of mixers of appropriate level and bandwidth, select those mixers having maximum isolation in the frequency range over which phase detection is to take place. This will minimize dc offset. If any information is available at this point, it is also desirable to select those mixers having minimum mixer-induced phase shift.

4) From those mixers having maximum isolation and minimum mixer-induced phase shift, select those having minimum conversion loss. This will maximize the sensitivity of phase response.

In addition to the above guidelines, other criteria that affect mixer selection include size, package type, connector type, and price.

REFERENCES

1. Cheadle, D.L. “Selecting Mixers for Best Intermod Performance,” Microwaves, Vol. 12, Nos. 11 and 12 (November, December, 1973), pp. 48-54, 58-62.

2. Cochrane, J.B. and F.A. Marki. “Thin-Film Mixers Team Up to Block Out Mixer Noise,” Microwaves, Vol. 16, No. 3 (March 1977), pp. 34-40.

3. Pappenfus, EW., W.B. Bruene, and E.O. Schoenike. Single Sideband Principles and Circuits, New York: McGraw-Hill, 1964, p. 130.

Vol. 5 No. 1 January/February 1978