The RFDAC (Radio Frequency Digital to Analog Converter) Breakthrough and Advantages

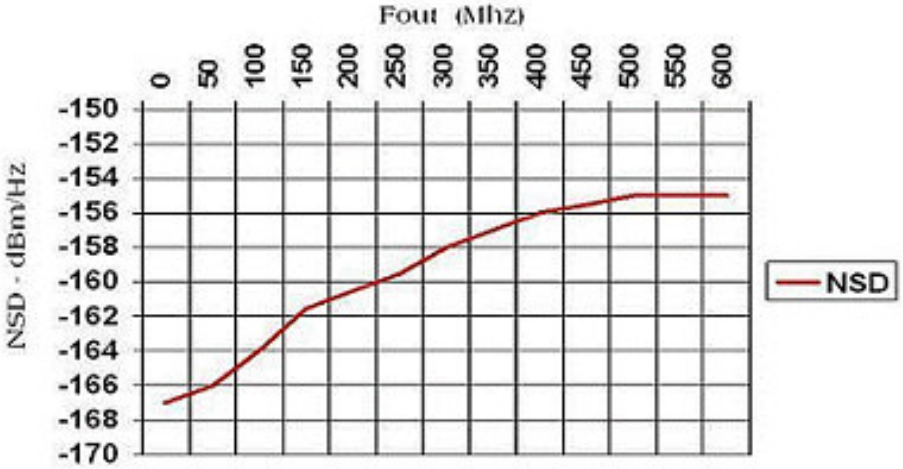
Desgning true Nyquist rate DACs that meet theoretical noise and linearity limits is a daunting task, even for the most seasoned designer. In the author's survey of the marketplace, one comes to an inescapable conclusion. Many have tried, most have fallen short of the theoretical mark.

This is particularly true of high speed, high resolution DACs. No one, to date, has produced a true 14 or 16 bit Nyquist Rate DAC, even at modest sampling rates. Given this, the design of high performance, Giga-sample rate DACs becomes even more difficult and elusive, if conventional design techniques are employed.

To set a benchmark, the author has chosen to analyze the highest performance, highest resolution Nyquist DACs in the industry, the AD97xx Tx DACs from Analog Devices. This is done to set a “State of the Art” benchmark and to help illustrate the RFDAC advantage.

Noise

Analog Devices typically specifies their noise performance as noise spectral density (NSD) in units of dBm/Hz. A plot to their NSD is shown below:



AD9736 Noise Spectral Density vs Fout at 1.2 GSPS
Figure 1

One will observe that given a 1.2GSPS clock rate, as the DAC output frequency increases, the noise spectral density increases. Taking the endpoints of the single tone curve, -166 dbm/Hz at about 50Mhz and -155 dbm/Hz at 550Mhz, and doing some math, one arrives at a DAC SNR of about -75dBc at 50Mhz and about

-61dBc at 550Mhz. This sets the AD9736 at 12 bit performance at 50Mhz and under 10 bits at 550Mhz.

Going further, since clock jitter is clearly dominating the DAC noise floor, if one solves for the time jitter, Tj, using equation 1

$$\text{Eq 1.} \quad \underset{\text{dBc}}{\text{SNR}} = 20\log\left[\frac{1}{\pi f_c T_j}\right]$$

Where: f_c = DAC sampling rate
T_j = total system time jitter

one will arrive at total Tj of 47fs at 50Mhz, and 236fs at 550Mhz. If theoretical 14 bit performance were to be achieved with the AD9736 design, a total rms time jitter reduction by a factor of 5, to around 9fs, would need to be realized and maintained to Nyquist.

If a Nyquist rate DAC were needed to provide output frequencies in the 3700Mhz range, a sampling rate greater than 7400Mhz would need to be realized. If one wanted to maintain the SNR that the AD9736 currently possesses at 50Mhz to a new Nyquist limit of 3700Mhz (assuming thermal and shot noise did not dominate the DAC noise floor), a factor of 6 reduction in time jitter to 7.5fs would need to be achieved.

Sampling rates greater than 7400Mhz and factors of five and six reductions in clock jitter from an already low 47fs are clearly impractical if DAC operating power is to be preserved. What is needed is a breakthrough methodology to get around this physical bottleneck.

The RFDAC

The RFDAC developed by CurrentRF provides this breakthrough. Two versions exist and are shown below:

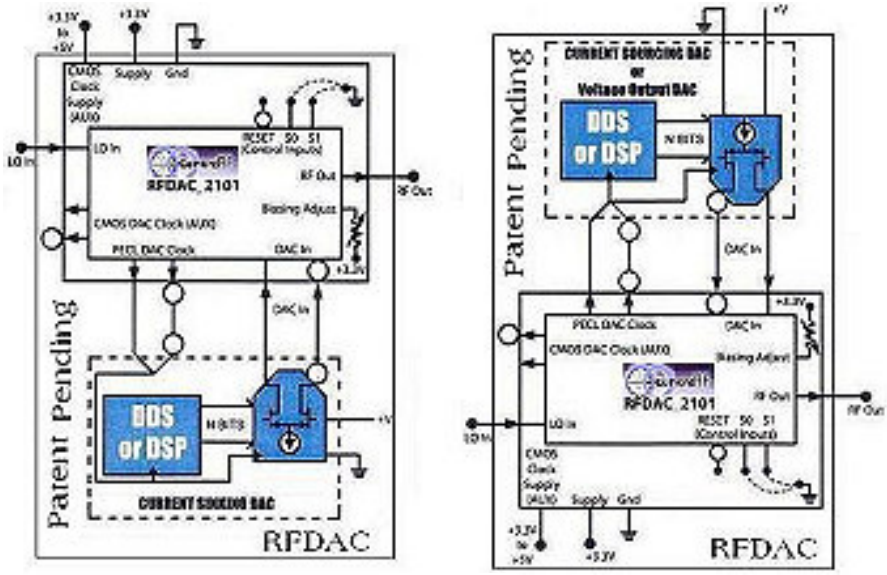
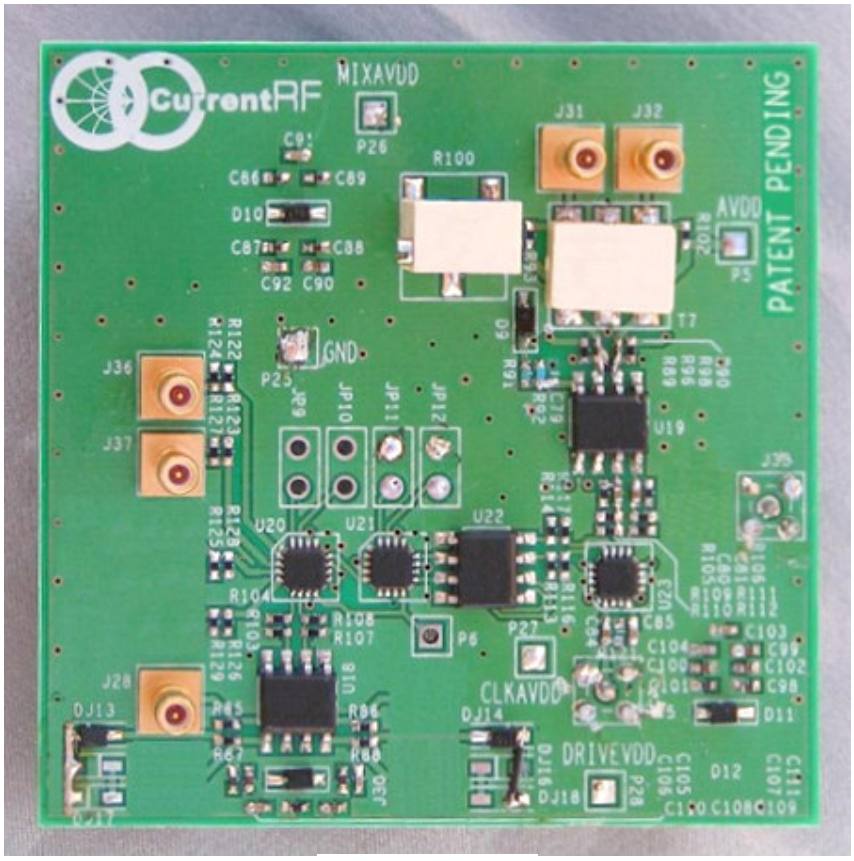


Figure 2

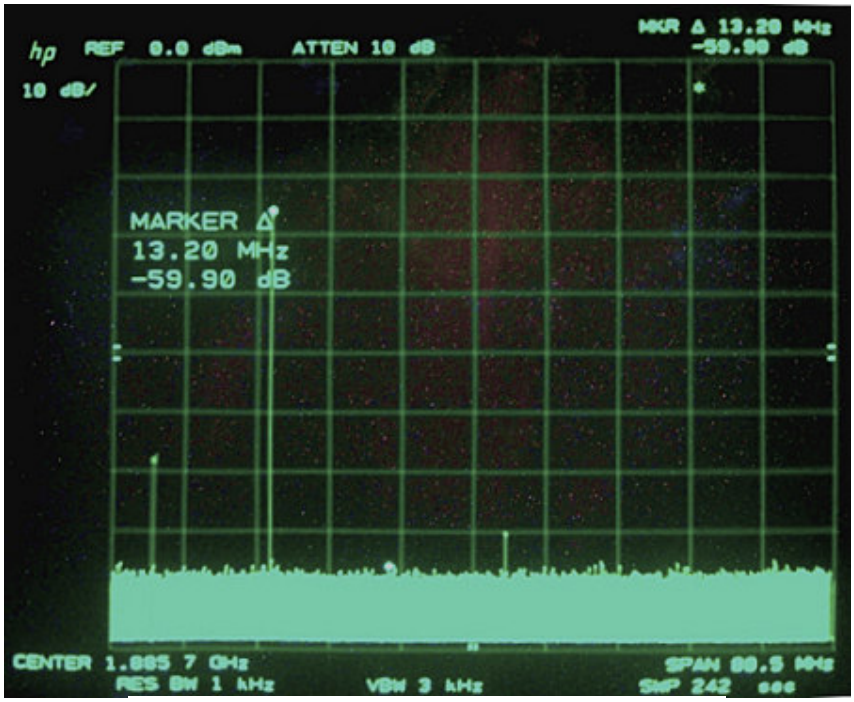


RFDAC_2101
Figure 3

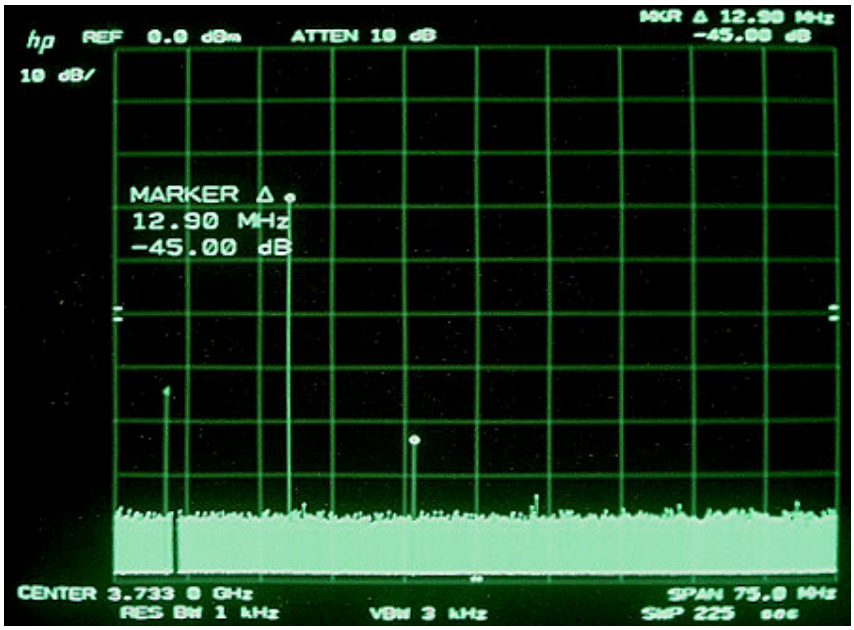
The RFDAC_2101 module is designed to directly interface to the output of any baseband DAC. The module replaces all upconversion circuitry from the baseband DAC outputs to the input of the system final power amplifier by reusing, current mode amplifying, and reconverting baseband DAC output currents. With the RFDAC_2101 module, baseband DAC anti-alias filtering is eliminated, thus eliminating the group delay distortion such filters produce in modulator systems. The relatively high distortion RF mixers and amplifiers that are presently utilized in upconversion systems are replaced, as well as baseband DAC clock generation circuitry. The chosen baseband DAC and the RFDAC_2101 module form a new entity, the RFDAC.

The RFDAC_2101 module adds only 2.3as $(2.3\text{X}10^{-18}\text{s})$ of additional time jitter to the final baseband DAC output signal. Coupled with the AD9736, for instance, the RFDAC_2101 module time jitter is root sum of squared with the time jitter produced by the AD9736 at 50Mhz, creating an RFDAC with12 bit SNR at 3700Mhz.

The advantages of this practically jitter free device manifests itself in the RFDAC noise floor and Noise Spectral Density(NSD).



Noise Spectral Density=-164dbm/Hz
SFDR= -55dBc (Third Harmonic)
Figure 4



Noise Spectral Density=-164dbm/Hz
SFDR=-45dBc (Second Harmonic)
Figure 5

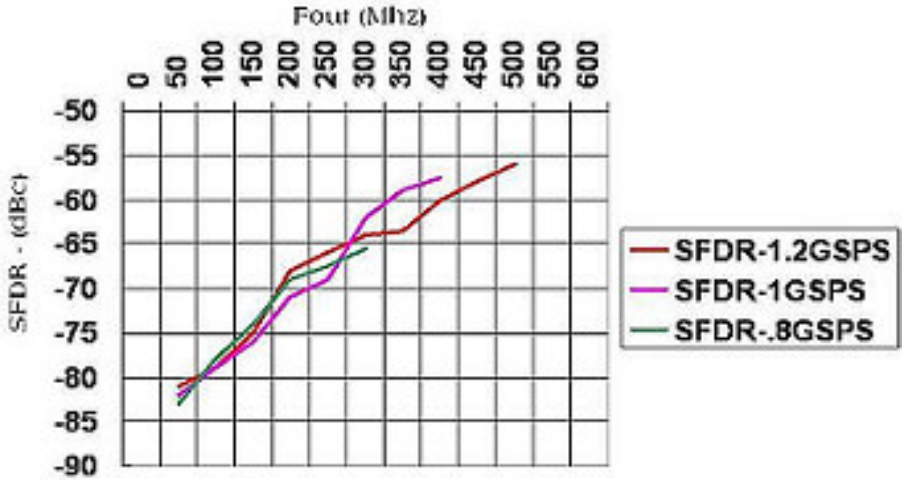
As is demonstrated by the spectral plots of the RFDAC operating at 1.85Ghz(figure 4) and 3.7Ghz(figure 5), the Noise Spectral Density for the RFDAC is baseband DAC limited.

Utilizing the AD9851(a 180 Mhz DDS synthesizer), with it's 10 bit DAC and DDS synthesizer as a baseband source, the DAC noise floor and noise spectral density (-165 dBm/Hz) is virtually unchanged through RFDAC processing to 1.85Ghz and 3.7Ghz(-164 dBm/Hz). If one were to use the AD9736(or any other DAC) as the baseband source, with a sampling clock rate at 1.2GSPS (or less), the noise characteristics seen in the RFDAC output spectrum would be virtually unchanged

from that of the AD9736. Baseband DAC operation with the lowest possible sample rate and operating within it's lowest possible output frequency range will allow optimal noise performance from the baseband DAC, and ultimately, from the RFDAC.

Linearity and Intermodulation Distortion

DAC linearity is generally specified in terms of Spurious Free Dynamic Range (SFDR) and Intermodulation Distortion(IMD) in units of dBc. Plots of the AD9736 SFDR and IMD variation as DAC output frequencies approach Nyquist are shown below:



AD9736 In Band SFDR vs Fout (20 mA FS)
Figure 6

One will observe in figures 6 and 7, that given any clock rate, as the DAC output frequency increases, the SFDR and IMD decrease, at a much greater rate than could be accounted for by nominal, zero order hold, sinx/x roll-off. Although the mathematics are statistical and complex, involve second and third order effects, and are difficult to model accurately, this SFDR and IMD degradation as Nyquist is approached is predictable through Equation 2.

EQ 2.

$$I(f_o)=\left[\sum_{b}\sum_{k} W(f_b) * \delta(f_b - k(f_c \pm f_{jb}))\right] \times \left[\frac{\frac{\sin \pi f_o}{f_c}}{\frac{\pi f_o}{f_c}}\right]$$

Where: f_o = the DAC output frequency

f_c = the clock frequency of the DAC

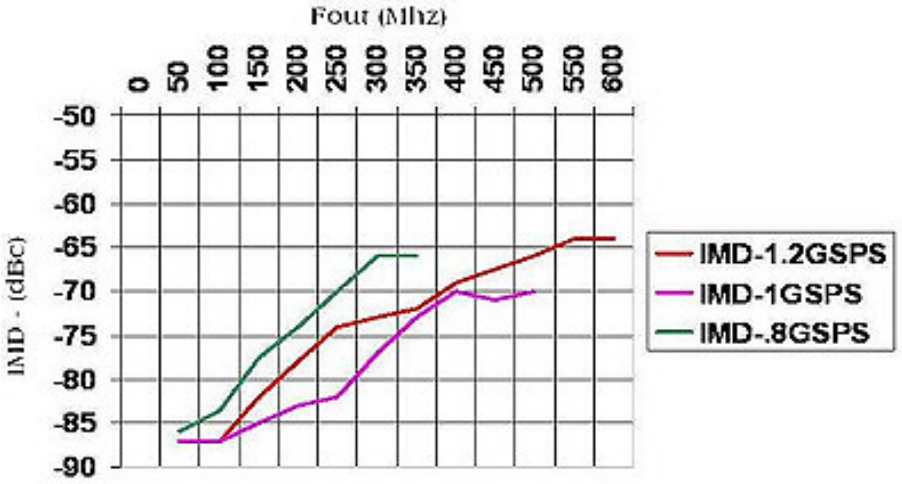
f_{jb} = the frequency jitter of each DAC switch path

$W(f_b)$ = the binary pattern of each switch path

$I(f_o)$ = the output of the DAC

K = multiples of the clock frequency
b = each DAC switch

The author has had some success modeling this behavior with simulation tools during the development of the AD9858 and AD9859 DACs at Analog Devices and the HDAC4 at Northrop Grumman. Generally, the lower the allowable noise and jitter(f(jb) from equation 2) in the path from the DAC clock input to the final output of the DAC, the lower the SFDR and IMD distortion becomes as Nyquist is approached.



AD9736 3rd Order IMD vs Fout (20 mA FS)
Figure 7

As it was with noise requirements for DACs with Nyquist limits at 3700Mhz, maintaining the SFDR and IMD at performance levels comparable to the AD9736 at 50Mhz to a new, 3700Mhz Nyquist limit requires a sampling rate greater than 7400Mhz with a factor of 6 reduction in time jitter to 7.5fs.

Sampling rates greater than 7400Mhz and a factor of six reduction in clock jitter from an already low 47fs are clearly impractical if DAC operating power is to be preserved. The RFDAC approach in this case, is clearly an attractive alternative.

The RFDAC Advantage

The RFDAC_2101 produced by CurrentRF clearly provides output frequency advantages to conventional Nyquist rate and Delta-Sigma DACs. By making **ANY** DAC output frequency possible, the Nyquist limit in conventional DAC designs is no longer an issue. **The Nyquist barrier has been broken.**

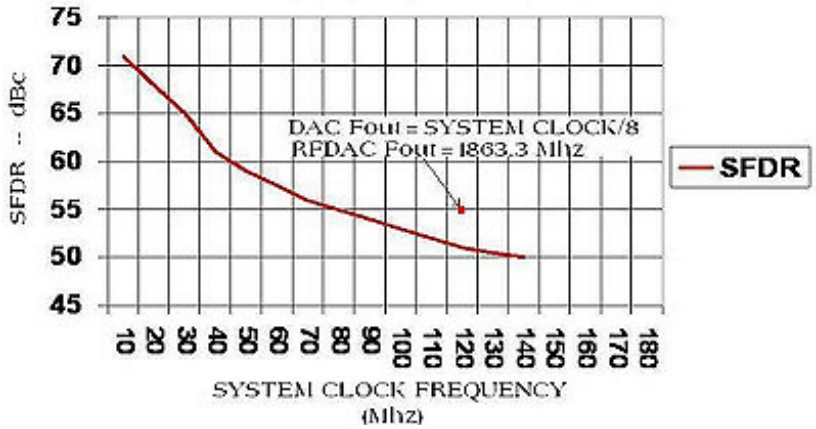
Further, the RFDAC_2101 adds very little additional SFDR and IMD distortion to the RFDAC output signal(see figures 4, 5, and 8).

Lastly, this approach allows optimization of baseband DAC noise, SFDR, IMD, and power performance as never before by allowing baseband DACs to operate at lower clock rates and outputs, thus providing cleaner inputs for the RFDAC_2101, and ultimately, cleaner, purer RFDAC outputs.

Figure 8, a plot of worst case SFDR for the AD9851 DDS synthesizer illustrates this phenomenon. The AD9851 was utilized as a baseband source for the RFDAC_2101 spectral plots in Figures 4 and 5. The clock rate for the AD9851 was set to about 120MSPS. From the figure 8 plot, worst case SFDR is about -51dBc for a DAC output frequency of 40Mhz.

Allowing the AD9851 baseband DAC to operate at an output frequency of 13 Mhz instead of 40Mhz, causes the SFDR to in the baseband DAC to increase, allowing the SFDR from the RFDAC to increase to -55dBc in the 1.85Ghz band(third order distortion limited-see figure 4). Also, because even order cancellation is preserved in the path from the baseband DAC(no low pass filter present) to the RFDAC_2101 module, even order harmonics are suppressed to noise floor limits.

Operation of the RFDAC at 3.7Ghz(see figure 5) reveals some even order degradation, as the second harmonic rises to reduce the SFDR to -45dBc. This is due to layout non-idealities(RF insertion/return loss, settling at 3.7Ghz, etc.), but performance still acceptable for WLAN applications.



AD9851 Worst Case SFDR Fout=System Clock/3
Figure 8

Power Consumption/Efficency

The AD9736, operating at 1.2GSPS, with an output frequency of 330Mhz, consumes 380mW of power. These specifications give the AD9736 an efficiency of 868Mhz/W.

Allowing for the load capacitance and power supplies to remain fixed, and solving for power consumption using 7400Mhz as a clock base, one obtains an alarming prediction of 8.5Watts of power required to reach an Nyquist bandwidth of 3700Mhz, if CMOS is used. This is clearly impossible, given packaging constraints, overall system power constraints, and technology constraints.

The RFDAC_2101 utilizing the AD9736 as a baseband DAC, with a sampling rate of 1.2GSPS, with an output frequency of 330Mhz, consumes 891mW of power. These specifications give the RFDAC a clear advantage with an efficiency of 4150Mhz/W, effectively, 10 times better than the projected efficiency of CMOS.

Conclusions:

The RFDAC clearly is a breakthrough in Digital to Analog Conversion. Breaching the Nyquist barrier, any output frequency is now possible from low frequency digital data. The RFDAC allows optimal baseband DAC noise and AC performance, clearing the way for true 12, 14, and 16 bit performance at any output frequency. The RFDAC provides the avenue for giga-hertz operation without the power penalty demanded with other designs and techniques. Similar to the transition from discrete electronic systems to integrated circuits, the RFDAC provides clear speed, performance, and power advantages over it's predecessor, the Nyquist Rate DAC.

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