# Accurate Phase Noise Prediction in PLL Synthesizers

Part 2: Here is a method that uses more complete modeling for wireless applications

**By Lance Lascari**
Adaptive Broadband Corporation

As discussed in part one of this article, published in the April issue of *Applied Microwave & Wireless*, phase noise characteristics of the frequency synthesizer contribute greatly to system performance. In this concluding section, we will show and discuss experimental results for the op-amp in loop filter.

| Design goals | Value | Comments |
|---|---|---|
| Output Frequency | 865 MHz | |
| Reference Frequency | 200 kHz | |
| Frequency Step Size | 12.5 kHz | |
| PLL Loop bandwidth | 750 Hz | Get as close as possible with available components |
| Phase Margin | 55 degrees | |
| Additional Reference Frequency Attenuation Required from the Third Pole | 10 dB | |

▲ **Table 2. Design goals for the example loop filter design.**

## Op-amp in loop filter

While the cases using the passive loop filter (no op-amp) are simply a matter of circuit analysis, the case using the active filter requires some explanation. This case will only be described here; the accompanying analysis can be found in the supporting MathCad documents.

With the op-amp in the loop, and the filter configuration shown in Figure 1, four different noise sources and important factors exist within the loop itself: $R_2$, the op amp itself, the gain of the op-amp, and $R_3$.

The noise within $R_2$ is the same as the cases previously mentioned. However once this noise is determined, the gain of the amplifier needs to be applied to it (amp_gain in Figure 1). The output of the op-amp is again filtered by $R_3$ and $C_3$. A schematic of this is pictured in Figure 2a.

The op-amp itself contributes noise, and this is one reason to place the op-amp after the second order filter section but before the third pole. The third pole can then provide some attenuation of the broadband noise. Manufacturer's data sheets will usually specify the input noise of the op-amp in nV/$\sqrt{Hz}$ . This noise voltage is simply multiplied by the amplifier's gain (amp_gain), and then passed through the filter formed by $R_3$ and $C_3$.

Op-amps are usually regarded as very low-output-impedance devices. For this reason, the analysis of the noise due to $R_3$ can be greatly simplified if an op-amp is in the loop as shown in Figure 1. If it is assumed that the op-amp output impedance is virtually a short (which would be accurate, even if the op-amp output were a few hundred ohms), then the noise voltage generated in $R_3$ is simply connected to ground, then filtered through $R_3$ and $C_3$.

## Practical design example

To show the effect of the resistor noise, two different loop filters were designed to meet the basic specifications outlined in the goals section of Table 2. The only differences between the filters were their implementation of the third

pole. The values used in each of the designs were typical of what one designer might choose over another.

## Experimental setup

Equipment used in the lab setup included a Hewlett-Packard 8563E spectrum analyzer with the phase noise utility software (P/N HP85671A) installed; a PC running a custom application developed to gather tabular data after the phase noise utility was run; and the PLL synthesizer under test (modified standard product produced by Adaptive Broadband Corporation).

The results presented in Figures 9 and 10 represent five averages of each phase noise measurement. In order to show the limitations of the measuring system, (i.e. the spectrum analyzer), the phase noise of the extremely low noise HP 8642B signal generator was plotted for comparison purposes. At higher offset frequencies where the measurements and models begin to disagree, it is clear that that the noise floor of the spectrum analyzer is contributing to measurement error.

| Component/Specification | Value | Comments |
|---|---|---|
| Synthesizer IC, National LMX2350 Fractional-N PLL | Allows 1/16th Fractional mode | |
| Phase Detector Noise Floor (Npd_ref from Equation 6) | –200 dBc/Hz | Data supplied by National Semiconductor. |
| Phase Detector Gain | 1.6 mA/cycle | Set to maximum for this design. |
| VCO Tuning Sensitivity, $K_{vco}$ | 27 MHz/volt | Custom vendor supplied component, measured at frequency of interest. |
| VCO Phase Noise | –103 dBc/Hz at 10 kHz offset | Measured for this particular device using a very narrow and quiet loop. |
| TCXO reference oscillator Frequency | 12 MHz | |
| TCXO reference oscillator Phase Noise (Ntxco_ref from Equation 7) | –125 dBc/Hz at 100 Hz offset | This number was estimated from measurement data from many PLLs. This is roughly 10 dB worse than published data on a similar product from the TCXO vendor. Measurements for the model used were unavailable. |

▲ **Table 3. Specifications for the components available.**

## Discussion of experimental results

Figures 9 and 10 show excellent agreement between the modeled phase noise of the synthesizers and the measured results. The conclusion that must be drawn is resistor noise can be a very significant contributor to synthesizer phase noise, and thus needs to be considered in all low-noise synthesizer designs. For the case of these experiments, and others performed by the author, the models presented accurately predict this noise, allowing the analysis of all of these degradations at the time the loop is designed [1].

| Loop Filter Component Values | Value for Case 1 | Value for Case 2 |
|---|---|---|
| C1 | 0.1 $\mu$F | 0.1 $\mu$F |
| R2 | 500 ohms | 500 ohms |
| C2 | 1 $\mu$F | 1 $\mu$F |
| R3 | 1 kohm | 10 kohm |
| C3 | 1000 pF | 100 pF |

▲ **Table 4. Component values for the two loop filters studied.**

The loop filters for case 1 and case 2 both meet the basic requirements of the design but have drastically different phase noise characteristics. For instance, at the 10 kHz offset points, the two synthesizers differ in phase noise by almost 10 dB. For narrowband systems with channels spaced at this interval, this would equate to a difference in adjacent channel rejection of 10 dB when comparing case 1 to case 2. Although the resistors are much smaller in the case 1 analysis, the noise contribution should not be ignored.

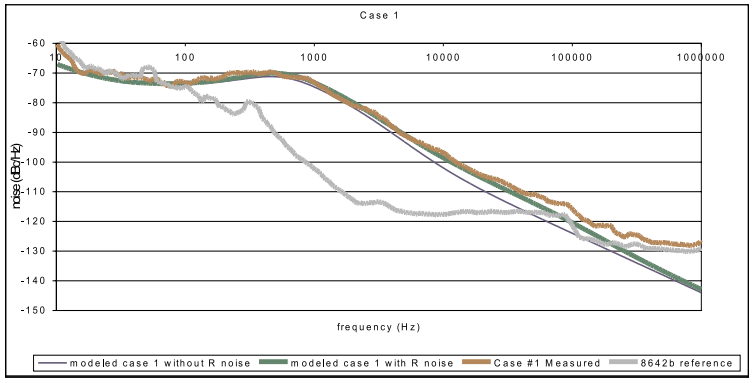
Even more significant than the agreement well outside of the loop bandwidth is the agreement near the loop bandwidth. Since the magnitude of the noise that falls near the loop corner is much larger than the noise far outside of the loop bandwidth, it contributes significantly to the RMS phase error and residual FM metrics. These metrics are very indicative of the performance degradations caused by frequency synthesizers in QAM and FM/FSK systems respectively. If the synthesizer noise were modeled without resistor noise, the results would be dramatically different, especially for case 2.

## Reducing resistor and op-amp noise contributions

When designing a frequency synthesizer, there are

often several degrees of freedom that can be exercised in order to minimize the system phase noise. If there are no degrees of freedom, up-front design analysis will at least show an accurate prediction of the phase noise. This prediction may help to make system tradeoffs rather than sticking to a more stringent synthesizer specification.

In most synthesizer designs, it seems that R3 is typically the single most significant contributor to the resistor noise. This begs the question, "Is the third pole really needed?" If the reference suppression within the loop is sufficient without the third pole, it is in the designer's best interests to leave these parts out of the design. If this pole is required, the value of $R_3$ should be kept as small as possible without upsetting the basic filter response.




▲ **Figure 9. Measured and modeled phase noise of the example synthesizer, case 1.**

Some VCO designs themselves use resistors to supply the tuning voltage to the varactor (the similarity to the $R_3$ analysis is staggering). In many published VCO designs, large resistors are used to feed the varactor. This is a good choice for simple, and low-cost designs since resistors are inexpensive, resonance-free, and they don't typically degrade resonator Q if they're large relative to the other shunt resistances in the circuit. Resistors are hardly a good choice, however, if the tuning sensitivity (VCO gain) is high. The noise contribution by this resistor is proportional to its value alone in this case; a small resistor in series with a choke may be a good choice in many applications.

Op-amps, even if chosen carefully, represent significant contributions to phase noise. The synthesizer designer should be careful to determine whether an op-amp is truly required in order to meet the system requirements. If increased voltage is required, consider using an external charge pump with higher supply voltages (some synthesizer ICs still support the connections required for using an external charge pump). Obtaining good balance in an external charge pump can be difficult, leading to increased reference spurs and power supply noise at the reference frequency. A low noise charge pump potentially offers reduced noise over the op-amp, as the tuning voltage range can be increased with a designer-chosen charge pump current. This represents two degrees of freedom: lower tuning sensitivity and reduced resistor values due to potentially increased current. It would be excellent if the available synthesizer chips allowed for higher tuning voltages or specifically allowed for simple implementations of well-balanced external charge pumps.

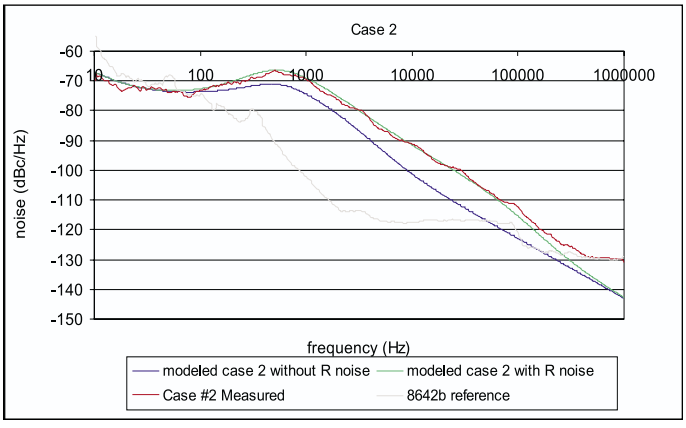
Reducing the VCO tuning sensitivity is another way to reduce the overall noise. This needs to be analyzed on a case-by-case basis, however, since the loop filter resistor values will increase with reduced tuning sensitivity. Any fixed magnitude noise sources in the loop will also drop proportionally with the VCO tuning sensitivity.

One particular option the author feels worthy of exploration is increasing charge pump current. With increased charge-pump current, the impedance (hence resistance) in the loop drops. If your synthesizer has a programmable charge pump current setting, leaving it at maximum is best in order to reduce the resistor noise contribution.

Each of the suggestions presented carries with it some design implication that needs to be carefully evaluated before tradeoffs are made. In some designs, simply increasing charge-pump current or eliminating the 3rd pole used for reference attenuation could yield dramatic improvement.

## Conclusion

In order for designs to meet the increasingly demanding performance requirements in the wireless arena, a detailed understanding of every component is critical. While relatively simple, the models presented have demonstrated excellent accuracy when compared to experimental data. These circuit models represent new tools that enable the designer to make important tradeoffs during the initial synthesizer design phase, rather than on the bench using empirical and time-consuming techniques. ■




▲ **Figure 10. Measured and modeled phase noise of the example synthesizer, case 2.**

## Acknowledgements

I would like to thank John Barenys of Adaptive Broadband for writing the phase noise curve acquisition program for the PC, which were invaluable in the preparation of this article. Thanks also to Dean Banerjee of National Semiconductor for providing many insightful email discussions and critiques of the work presented here. The support of Adaptive Broadband and numerous discussions with my fellow employees were very valuable during the preparation of this work. I also appreciate the efforts of the many people who helped by reviewing this article.

## References

1. Complete MathCAD Analysis used in this article is available in MathCAD and PDF formats at http://home.rochester.rr.com/lascari/lancepll.zip.

2. W.P. Robins, *Phase Noise in Signal Sources: Theory and Applications*, W.P. Robins, 1984.

3. James A. Crawford, *Frequency Synthesizer Design Handbook*, Artech House, 1994.

4. Dean Banerjee, *PLL Performance, Simulation, and Design*, http://www.national.com/appinfo/wireless/deansbook.pdf.

5. A. Bruce Carlson, *Communication Systems: An Introduction to Signals and Noise in Electrical Communication*, McGraw-Hill, 1986.

6. William O. Keese, "An Analysis and Performance Evaluation of Passive Filter Design Technique for Charge Pump Phase-Locked Loops," Application Note 1001, National Semiconductor.

7. Jeff Blake, "Design of Wideband Frequency Synthesizers," *RF Design*, May 1988.

8. "Noise Specs Confusing?" Application Note 104, National Semiconductor.

## Author information

Lance Lascari is a Principal Engineer at Adaptive Broadband Corporation in Rochester, NY. He has been working as an RF designer on the company's QAM Point-Point and FSK Point-Multipoint products for the past five years. He earned a BSEE from the Rensselaer Polytechnic Institute in 1995. His professional interests include low-noise synthesizer and VCO design, design for high linearity, and low-cost transceiver design. He may be reached via email at llascari@adaptivebroadband.com, or through his web page: http://home.rochester.rr.com/lascari.