Simulating a discrete GaAs FET power amplifier

The last decade has brought great improvements in non-linear circuit simulation software and economical desktop computers to support it. It would seem that power amplifier designers have benefited less from this than the IC community: due to the lack of available models the design is forced to the prototype phase sooner than is desirable. This paper describes an experiment to avoid the empirical approach by using a new source of device models.

In an ideal world there would be no need for the use of empirical design techniques for power amplifiers: PAs are notorious for "tweaks", which can lead to both schedule uncertainty and designer stress. When the design takes place on the test bench it is impossible to predict how long it will take to change the design for a new function. The ideal would be to make PA (multiplier, mixer, oscillator) design more like LNA and filter design, where early success is not accompanied by the frustration typically seen with PAs.

First of all, we know that the modelling techniques exist and are used quite successfully. Without them there wouldn't be as many MMIC/RFIC designs around. It really boils down to discipline, data, and tools. Sound design practices, quality data/models, and flexible tools that allow easy integration are the most important elements. In the IC design world the process is tightly controlled and a great deal of time is spent developing and verifying good device models. With the support of vendors, peers, and management, it is possible to bring board level design much closer to the precision of IC design. In medium volume production environments we stand to gain a great deal.

Device models

Searching for device models over the years and trying to pressure device vendors to provide them has yielded very little. The recently-discovered Excelics Semiconductor website [1] shows a line of low cost power GaAs FETs in plastic surface mount packages, provided with non-linear models. It was decided to carry out an evaluation experiment where the goal was to provide quality inputs and measure the results, comparing them to the model.

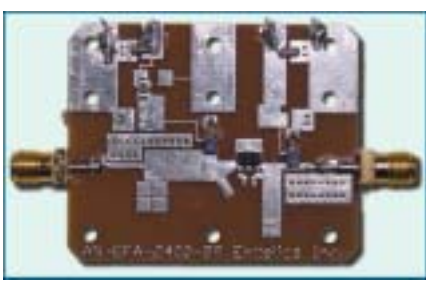

Figure 1: Evaluation boardsuperheterodyne receiver

Inputs:
- Device: Excelics EFA240D-SOT90 1W class GaAs FET
- Evaluation platform: Evaluation board from the vendor
  - Given board material
  - Given component values
  - Artwork pattern measured manually
- Device model(s)
  - S-parameters at the bias point of interest
  - Non-linear Curtice cubic model
- Curtice cubic model parameters
- SOT-89 package parasitic model parameters/schematic

Measurable outputs used:
- Wideband S-parameters and derived measurements
- Single tone harmonic level tests near the output P1dB
- Manual 1dB compression point measurement
- Two tone intermodulation tests

Other simulated parameters:
- Harmonic levels vs. drive
- AM-PM conversion
- Intermodulation distortion at constant drive & tone spacing vs. frequency

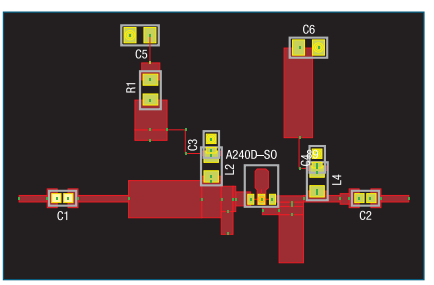

Figure 2: Eagleware Genesys layout approximating evaluation board layout

No actual design work was carried out. Eagleware Genesys was used to analyse the circuit and to gather the data from the instruments. There was no "tweaking" done to the device or evaluation board models to enhance agreement, as this would have affected the integrity of the experiment.

EFA240D-SOT89 Model implementation

The Curtice Cubic GaAs FET model surrounded by the SOT-89 package parasitics is shown in Figure 3. All the details of this model were provided by Excelics [4]. S-parameters at the desired bias point have been provided as a second point of reference for linear circuit evaluation.

Evaluation circuit

The schematic for the evaluation board is shown in Figure 4. Advanced T/Line was used to add the majority of discontinuities quickly and accurately (parameters are automatically derived from adjacent lines). The voltage probe and ammeter were added at the drain to observe the waveforms during harmonic balance simulations using "named" variables rather than node numbers.

While the application note from Ex-

celics [4] shows the basics of this circuit, more detail was required to simulate the design accurately. For this reason the evaluation board was carefully measured using a calliper and reproduced within the simulator using linear circuit models for the traces and components. The coupling capacitors were replaced with known components so that the parasitics could be modelled accurately.

The amplifier design is elegant in its simplicity, since all matching is accomplished with series and shunt transmission lines. However, the circuit is not unconditionally stable.

Simulations

Each lumped component used in this amplifier was modelled using appropriate parasitics as shown on the schematic. The simulated input-matching network differs slightly from the evaluation board, mainly due to the unique geometry used in the design. Any questions about the quality of the approximation could be verified by using a planar EM simulator such as Eagleware's EMPOWER to simulate the match, however the agreement was reasonable deeming the EM simulation unnecessary for this first pass analysis.

The small signal agreement has been found to be poor if the non-linear model is used. The likely cause is that the model

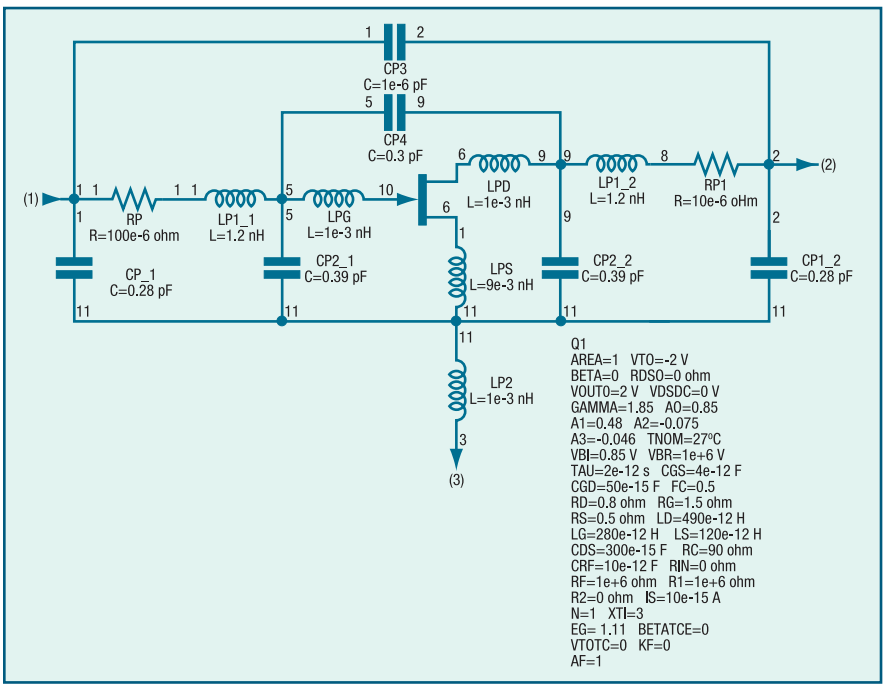

Figure 3: Curtice cubic FET model with Excelics SOT-89 package parasitics.

was optimised for analysing efficiency and linearity. Further details on this topic can be found in literature [2]. The main cause of disagreement is a lower drain-source conductance that is observed in the measurements and S-parameter based model. Reducing the "RC" parameter in the Curtice cubic model shown in Figure 3 greatly improves the small signal agreement at the expense of the non-linear agreement. The "additional" AC drain-source conductance for the Curtice cubic model can be thought of as a series R-C circuit with the resistance parameter equal to RC and the capacitance parameter equal to CRF using the Genesys nomenclature. It should be

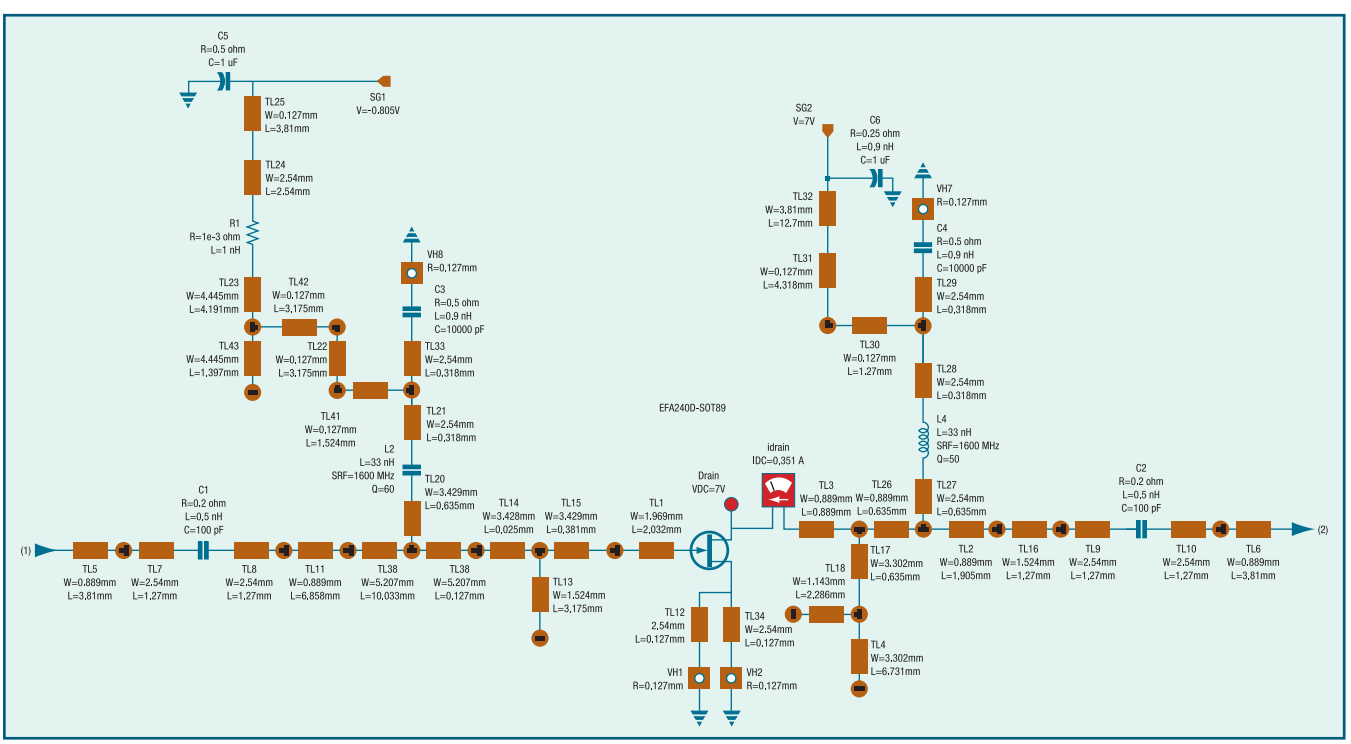

Figure 4: Schematic derived from Excelics applications note [4] and measurements of the evaluation board

noted that this is one method of improving agreement, as suggested after reviewing [2].

Excellent agreement between small-signal analysis and measurement was found when using the vendor-supplied S-parameters. Similarly, the non-linear agreement was impressive when the Curtice cubic model was used. While it would be desirable to have a single model that adequately handled both domains, the effort required to change between models for different types of analysis is very low. Hopefully device vendors will continue to improve their models such that they provide better agreement across the board.

The only inconvenience this model discrepancy presented is that the output power levels need to be matched between the measurements and the simulations by adjusting input drive levels. This is typically required (at the bench or in the simulator) when making any comparison between non-linear parameters on circuits, as the non-linearities are by definition strong functions of absolute levels.

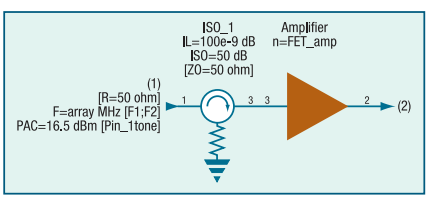

Figure 5: Single tone measurement set-up provides an example of reusing a schematic

Simulation configurations

There were a number of different simulations created to analyse the typical parameters of interest – small signal gain and impedances, stability, and non-linear performance. The hierarchical capabilities of Genesys allow the user to create different configurations for testing a given circuit with virtually no effort. Unlike the lab, here the circuit can be tested in multiple configurations after a change is made – with a single click.

These capabilities were used extensively to make the analysis flexible, complete, and fast. Once set up, the two-tone and single tone power sweeps could be configured individually so that the user can avoid manually changing the drive levels to the circuit depending on the test. The method for accomplishing this is simply to "reuse schematics" within the workspace.

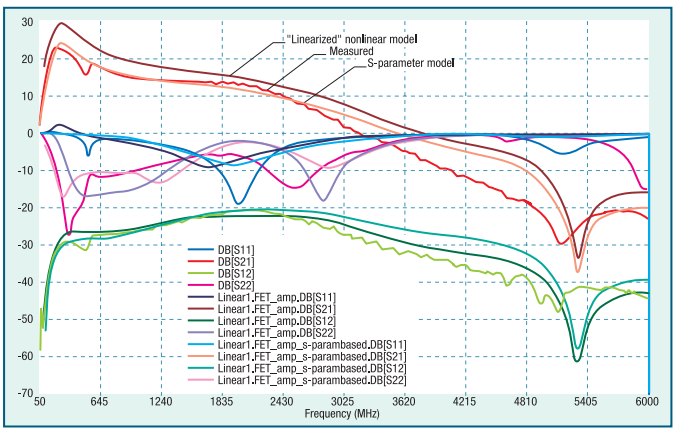

Figure 6: Small signal results for measured and both model options

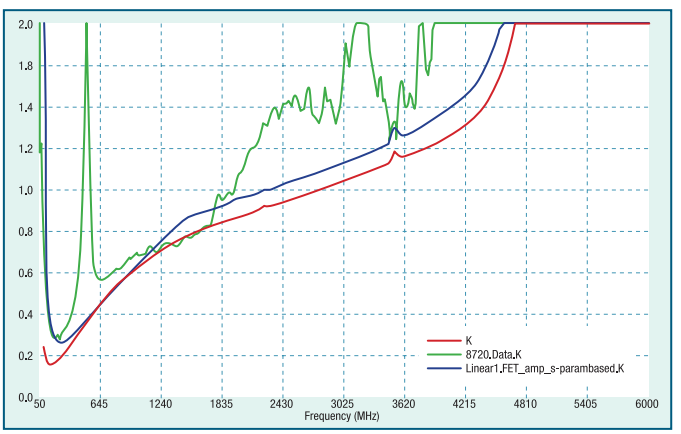

Figure 7: Stability factor K for both models and measured

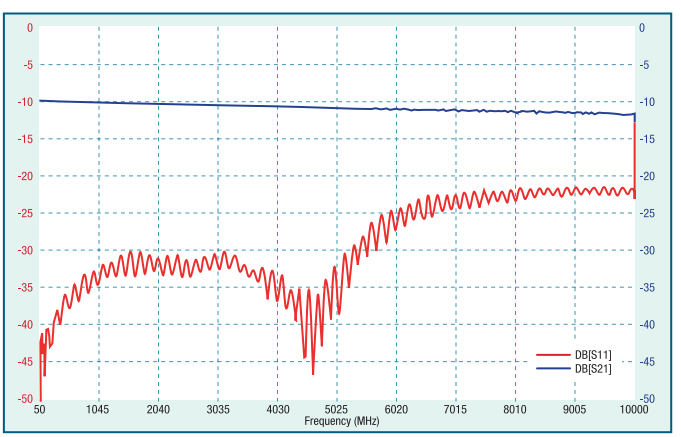

Figure 8: Measurement of test cable and attenuator for the purposes of "calibrating" them out of the TESTLINK data

Each "test" configuration becomes a new circuit that can be simulated with unique inputs and outputs.

The specific simulation types that require different test conditions are as follows:

- Linear simulation,
- Single tone Harmonic Balance (HARBEC) for examining harmonic levels (Figure 5 shows an example. An isolator is often desired for measuring power output vs. power input in poorly matched systems. The isolator would obviously prevent usable small signal input impedance measurements from being made on this circuit),
- Single tone harmonic balance for performing compression measurements (power sweeps), and
- Two tone harmonic balance simulation for evaluating third order intermodulation distortion.

Since our mission was the analysis of an almost "black box" amplifier (not something that we specifically designed), we compare the various simulations with

their measured counterparts. No special "tweaking" of the models was performed to enhance agreement.

Small signal/S parameters

The measured and simulated S-parameters are shown in Figure 6. As previously stated, the S-parameter based model yields much better agreement, especially when it comes to S21.

Device S-parameters were only provided to 6 GHz, so the comparison plots were limited accordingly. The stability factor "K" is plotted in Figure 7, showing encouraging agreement between the measured, the S-parameter based model, and the non-linear model.

Linear measurements were made using TESTLINK connected to an Agilent 8720ES 20GHz network analyser with high power test capabilities and quality test cables.

Non-linear analysis and measurements

These measurements were made using TESTLINK and an Agilent 8563E spectrum analyser. To protect the spectrum analyser from any accidental application of power greater than 1W, a 10dB attenuator was placed between the amplifier and the analyser. To compensate for the attenuator and a test cable, the cascade was measured using the network analyser and TESTLINK. The results are shown in Figure 8.

The importance of having this level of detail is shown through inspection of these results. Applying a constant factor for the loss introduced by the cable and attenuator would result in a fairly high error depending on the frequency.

To correct accurately for the frequency dependent loss of the set-up, all that is required is gathering the measured data and implementing the following equation:

Loss =.dbm(pa)-8720_cable_pad.Data.db(s21)

The equation simply adds the "negative loss" of the cable/pad to the measured result obtained through TESTLINK. The power of post processing to link the two data sets is an excellent application of core Genesys features, alleviating the need for any manual calculations or corrections. More powerful examples of post-processing are provided in the appendix.

Figure 9 shows the result for the fundamental and the first two harmonics. The output power level for this test is approximately the 1dB compression point. Note that the differences in frequency reported by the markers were due to the fact that the spectrum analyser sweep only allows for 601 points. The agreement is excellent for the second harmonic and the error is less than 8dB for the third harmonic. SMA connector discontinuities are possible causes for discrepancies at higher frequencies. If the exact connectors were available, they could be measured on a "standard" circuit board and "backed out" of the measurements just as the cable and attenuator were. For a more complete analysis, the connectors could be included in the circuit analysis, as the impedance interaction (non-linear effects) will have an effect on the performance beyond just mismatch and dissipative loss.

For bandwidth-efficient modulation schemes in crowded RF environments, linearity is becoming extremely important. OFDM, QAM, and to a degree CDMA (QPSK), systems all require high linearity for one reason or another. Some designers may quickly place this particular performance metric above all else.

The results of a two-tone test performed

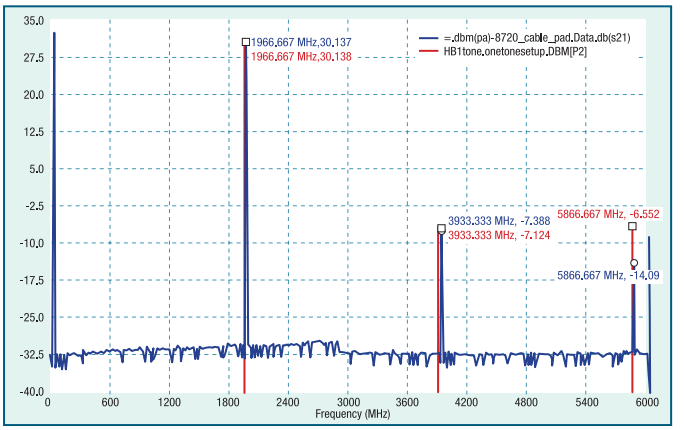

Figure 9: Single tone harmonic evaluations with the amplifier at or near its one dB compression point.

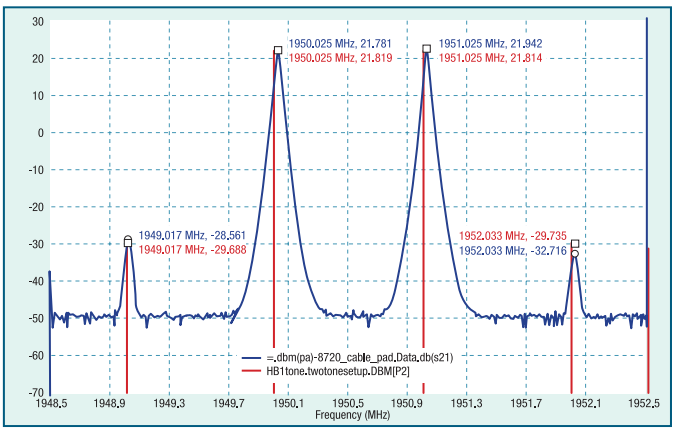

Figure 10: Class A two-tone test – this is a very healthy result for such a small device

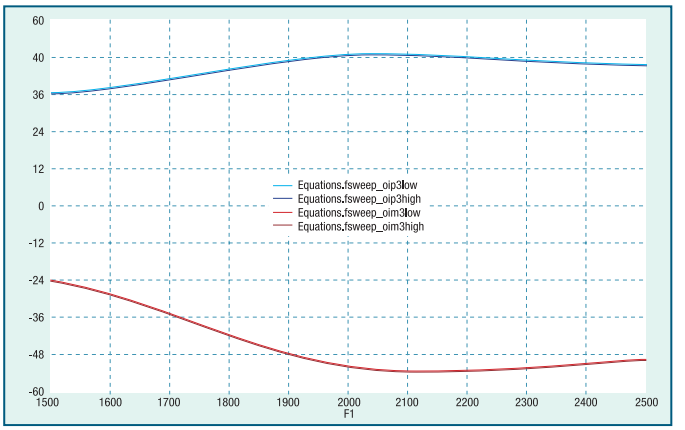

Figure 11: Sweep of OIP3 and OIM3 vs. frequency

at a Peak Envelope Power (PEP) level only 3dB below the 1dB compression point is shown in Figure 10. The agreement is impressive.

Anyone struggling to optimise a power amplifier on the bench for linearity should consider investing time in initial simulations. The accuracy is clear and there are no excuses. An example of using parameter sweeps with non-linear analysis is presented in Figure 11. The two-tone test signal is swept across the band while the OIP3 and relative IM3 products are computed as post-processed variables and displayed.

Lastly, it is always a good idea to know the peak power handling capability of an amplifier. A Genesys parameter sweep coupled with the enhanced graph-marker functionality in version 8.1 is an easy way to accomplish this.

Figure 12 shows the measured compression curve for the amplifier. Note that the marker can be set up to search automatically for the nearest value of computed "compression" to a value specified, -1dB in this case. For high order modulation such as 64 QAM, AM-PM is an important metric, so the phase shift vs. power output is shown as well. Figure 13 shows the GaAs FET drain voltage and current waveforms during the power sweep. The various shades seen for each measurement represent the discrete power levels of the sweep.

The power level of the first few harmonics during this power sweep is shown in Figure 14.

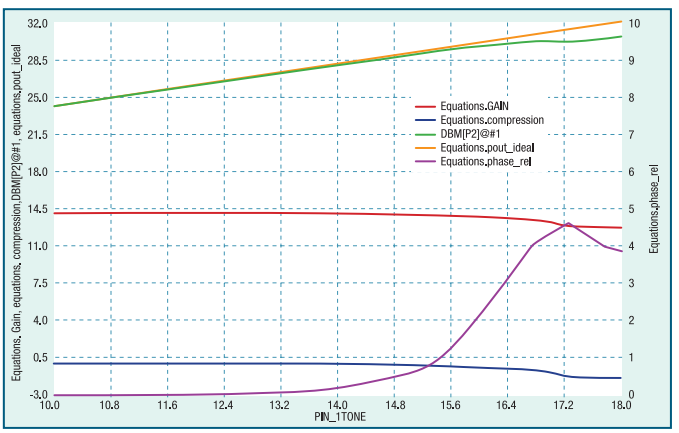

Figure 12: Compression and phase transfer curve (AM-PM conversion)

Conclusion

While this evaluation board is not a complete production-ready design, it has been shown that modelling power amplifiers with software familiar to most designers is a less daunting task than it used to be. Discrepancies observed between modelled and measured data are small, many of which could possibly be explained by details not yet examined (i.e. connector discontinuities, test equipment accuracy/repeatability and device-to-device variations). We think this result is quite usable, and at the very least can help the designer shave significant time off of the design cycle.

Taking the evaluation circuit design to the next level would involve refining the impedance matching and carefully addressing potential instabilities.

Acknowledgements

Special thanks go to Eagleware for sponsoring this work, Microwave Data Sys-

Post processing and non-linear measurements:

All HARBEC simulations have a discrete number of frequencies where the analysis is performed. For the purposes of post-processing and displaying results, there are various ways of accessing the simulation data. The discrete frequencies used for simulation can be accessed directly, or as a group.

Examples:

- Single tone simulation examples:
  - On a graph, dbm(p2) would display all discrete frequencies observed at port 2
  - If the input frequency was 1950 MHz, dbm(p2@#1) would yield the same answer as dbm(p2@1950), they would both show the power at the first frequency above DC that was used in the simulation.
  - dbm(p2@#0) is the RMS DC power that is delivered to port 2
  - dbm(p2@#2) is the RMS power of the 2nd tone, or the 2nd harmonic in the case of this single tone example.
  - The highest number of tones available is determined by the ORDER of the simulation
- Two tone examples
  - One difference in multiple tone simulations is that the "mixing order" becomes a factor. For the two-tone simulations presented in this document and the companion workspace, the maximum mixing order was set to 10. This means that each of the two tones intermodulation products up to an order of five were considered, i.e. a tenth order product is formed by two fifth order products.
  - Under the conditions described, the following explicit example is true:
    - F_input_1=1950 MHz
    - F_input_2=1951 MHz
    - Simulation frequencies (source)

      #0 = DC
      #1 = 1MHz (f2 – f1)
      #2 = 2MHz (2f2 – 2f1)
      #3 = 3MHz (3f2 - 3f1)
      #4 = 4MHz (4f2 - 4f1)
      #5 = 5MHz (5f2 – 5f1)
      #6 = 1946MHz (5f1- 4f2)
      #7 = 1947MHz (4f1 -3f2)
      #8 = 1948MHz (3f1 -2f2)
      #9 = 1949MHz (2f1 – f2)
      #10 = 1950MHz (fundamental input)
      #11 = 1951MHz (fundamental input)
      etc.

      Thus, computing the output IP3 based on the lower IM3 product would be computed using p2@#9 and p2@#10 as is shown in the equations below.

tems for allowing the test equipment to be used in the preparation of the article, and Excelics for the evaluation board and device models.

References

[1] www.excelics.com

[2] High Power GaAs FET Amplifiers, John L.B. Walker (Editor), 1993, ISBN: 0890064792 (Ref: Chapter 3)

[3] RF power amplifiers for wireless communications, Steve C. Cripps, 1999, ISBN: 0-89006-989-1

[4] AN-EFA-240D-SOT89-1 "Using the EFA240D-89 as a high intercept 2GHz linear power amplifier" (www.excel-ics.com). Model S-parameters, large signal model parameters, and package parasitic models available in the applications information section of the site.

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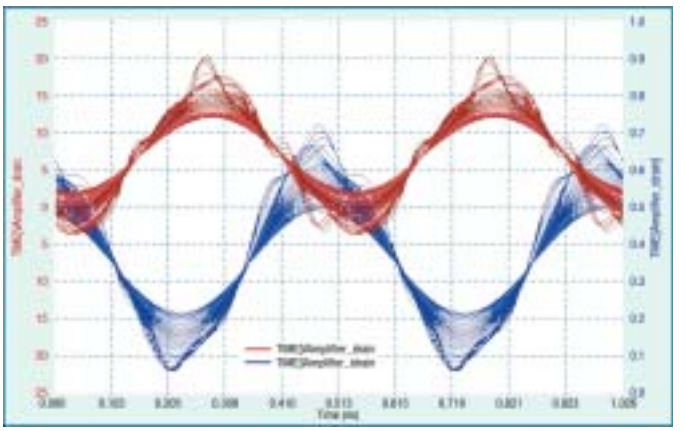

Figure 13: Drain voltage and current through the power level sweep

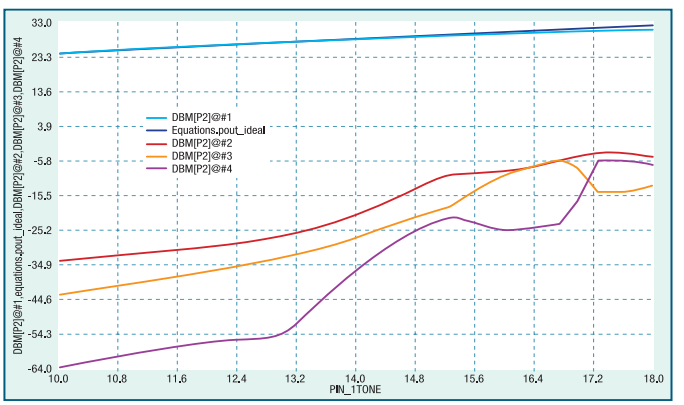

Figure 14: Harmonic levels vs. drive at one frequency

Example of post processing equations for compression, AM-PM conversion, and IP3 measurements

```
' POST PROCESSING
' for compression measurements
USING onetone_powersweep.onetonesetup ' specifies the simulation (onetone_powersweep) and the design
                                        (onetonesetup)
Gain=.DBM[P2@#1]-.DBM[P1@#1]          ' gain at each point in the power sweep
GainSS=getvalue(Gain,1;1)             ' small signal gain
Compression=Gain - GainSS             ' normalized compression
Pout_ideal=.DBM[P1@#1]+GainSS         ' "ideal" i.e. not compressed ideal output power that can be
                                        plotted next to actual
Phase_swp=.ANG360(P2@#1)              ' phase measurement at each point in the sweep
PhaseSS=getvalue(Phase_swp,1;1)       ' small signal phase
Phase_rel=Phase_swp-PhaseSS           ' relative phase ( similar to the normalized compression
above)

' IP3 calcs for various sweeps
'Note that the equations are broken up for readability
' also note that the frequency references (p2@#n) are setup for a maximum mixing order of 10.
'
' frequency sweep
USING hb2_freq_sweep.twotonesetup
fsweep_pplprod=.DBM(p2@#9)
fsweep_ppltone=.DBM(p2@#10)
fsweep_pputone=.DBM(p2@#11)
fsweep_ppuprod=.DBM(p2@#12)
fsweep_oim3low=-1*(fsweep_ppltone-fsweep_pplprod) ' IM3 in dBc from SCL
fsweep_oim3high=-1*(fsweep_pputone-fsweep_ppuprod) ' IM3 in dBc from SCL
fsweep_oip3low=fsweep_ppltone+(-1*fsweep_oim3low/2)
fsweep_oip3high=fsweep_pputone+(-1*fsweep_oim3high)/2
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