

# Board level design and verification with Genesys

Tips and tricks

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# Board level design and verification with Genesys

## Introduction

This is meant to be an informal, interactive session for Genesys users; please feel free to ask questions and contribute your perspective, war stories, tips!

The workspaces and circuits presented here will not be available for download, however I am happy to open them up live if you have questions. This is a very small sampling of the work I do with Genesys and simply represents some of the circuits I can show to demonstrate key design points.

If there are questions about other types of circuits I'm happy to discuss them as well (FET mixers, frequency multipliers, detectors, switches, oscillators).

# Board level design and verification with Genesys

## Agenda

To highlight some of our usage patterns with Genesys and share our techniques, the examples we've prepared are in the following areas:

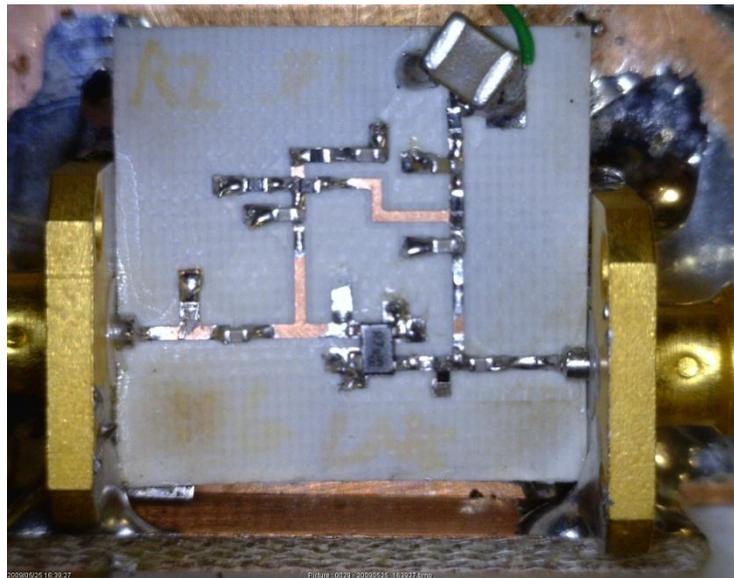
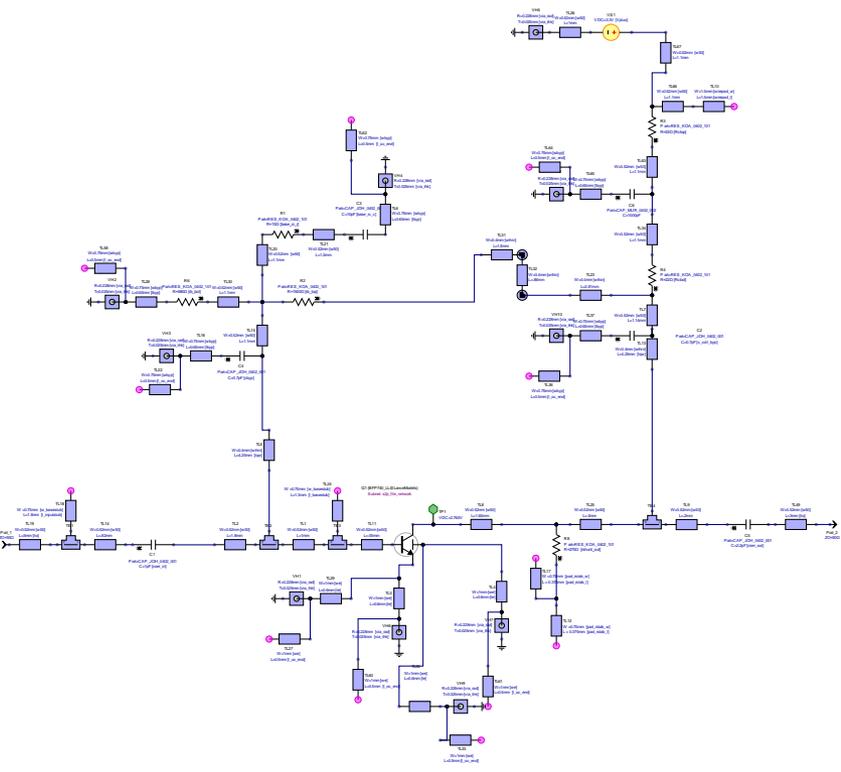
- Momentum (or EMPOWER) and linear or HB Cosimulation
- Amplifier stability analysis and verification
- Reference planes in EM simulation of active circuits
- Tolerance analysis in printed filters
- Patch antenna radiation patterns
- Unintentional radiation from microstrip structures

# Board level design and verification with Genesys Momentum and linear or HB Cosimulation

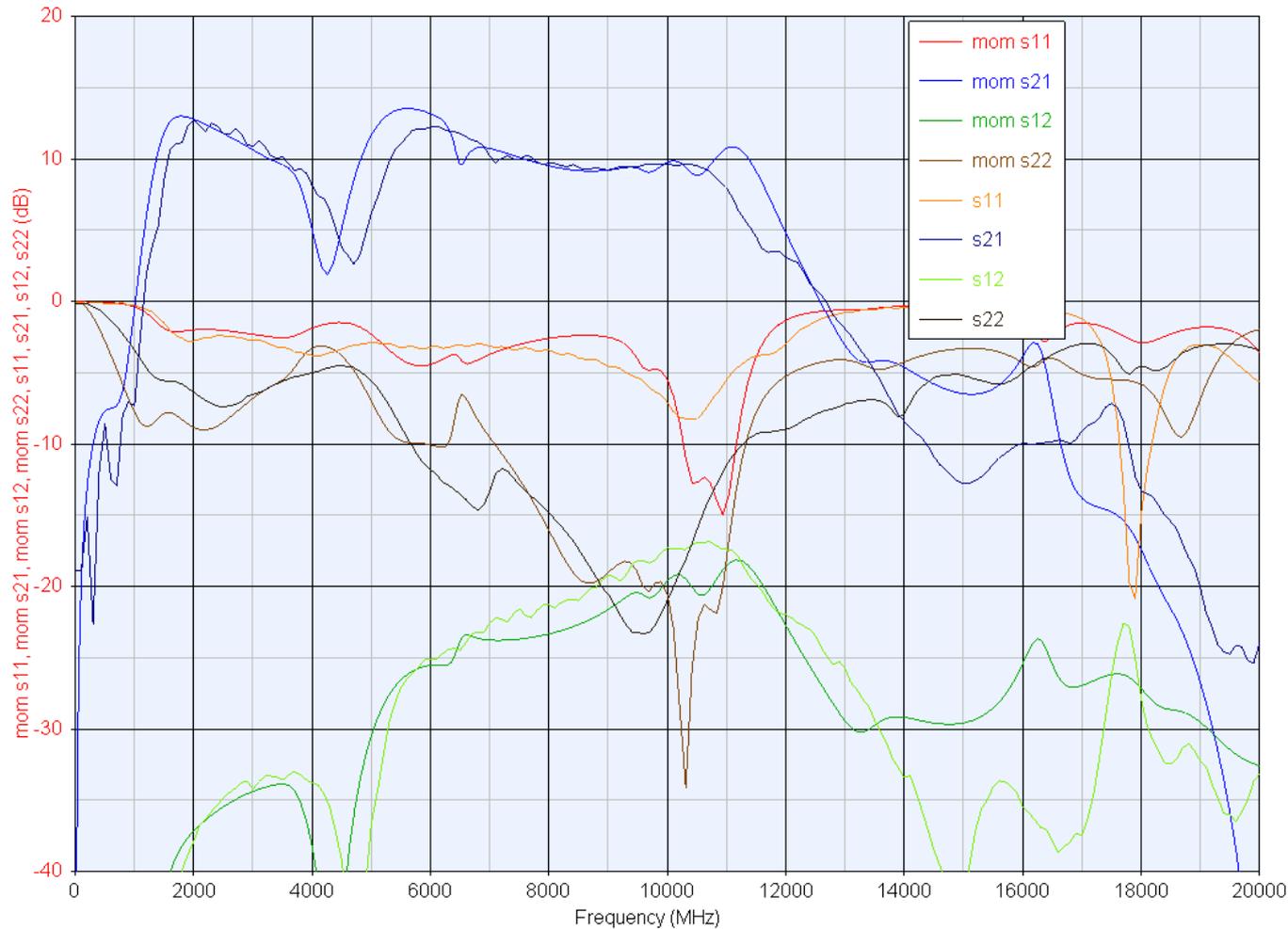
- Why do I use cosimulation or “EM simulation with active and lumped components” constantly?
  - Allows for more compact circuits – straight EM analysis of copper that does not conform to disco models available
  - “2<sup>nd</sup> opinion” on model based analysis
  - Speed has increased to the point that it is practical early in the design cycle
- Quick switching between transistor models with sub circuits and variables
- handling dual grounds with two port data and properly handling in EM simulation
- Fast tuning with lumped elements

Now an involved example to demonstrate these points

# Board level design and verification with Genesys Momentum and linear or HB Cosimulation: 11 GHz amplifier



# Board level design and verification with Genesys Momentum and linear or HB Cosimulation

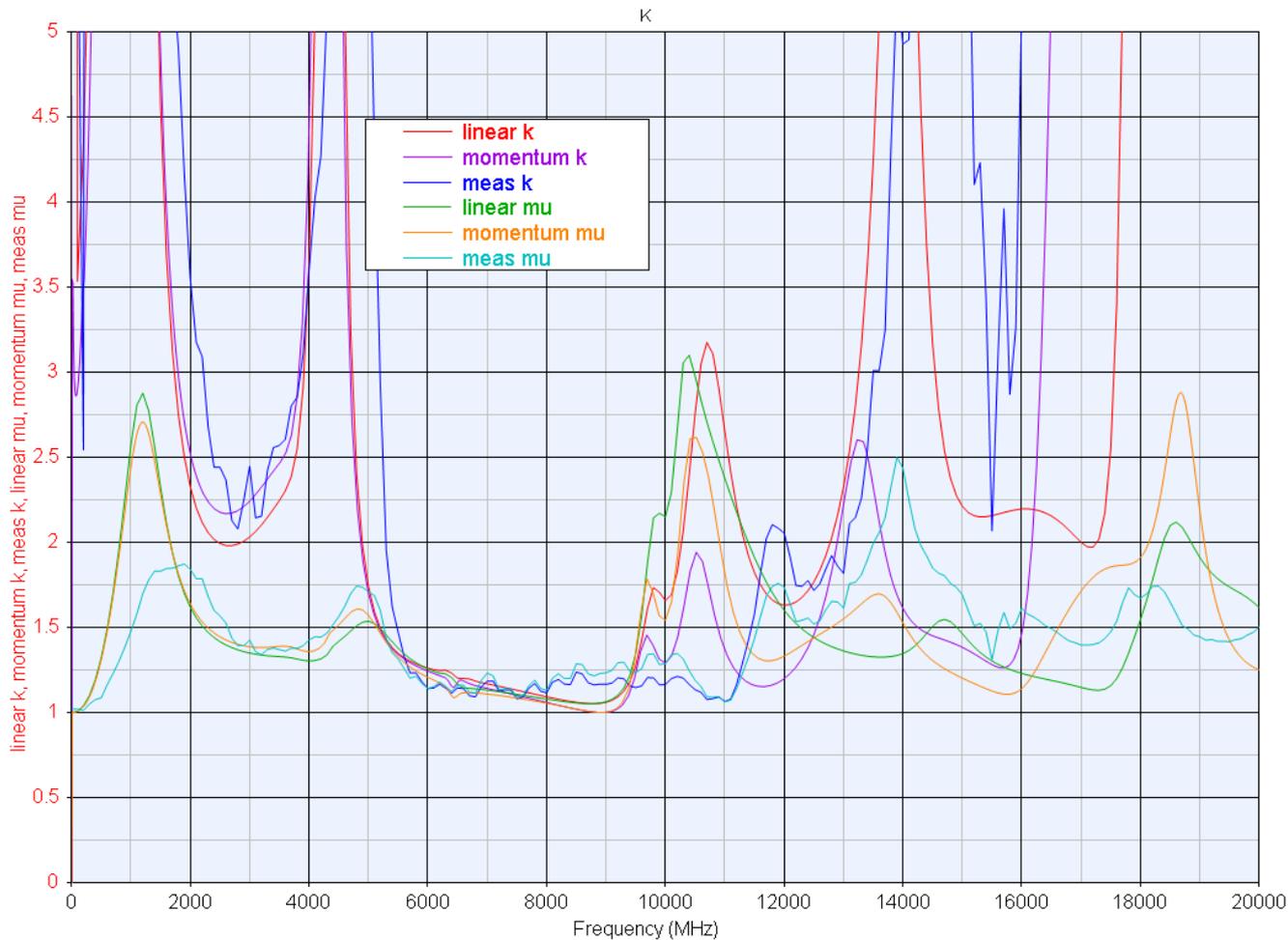


Agreement fairly decent for this example

“ripple” in Momentum results perhaps due to interpolation ?

Note: I used Modelithics models for the R's and C's here.

# Board level design and verification with Genesys Momentum and linear or HB Cosimulation



Stability factors  
for various  
analyses

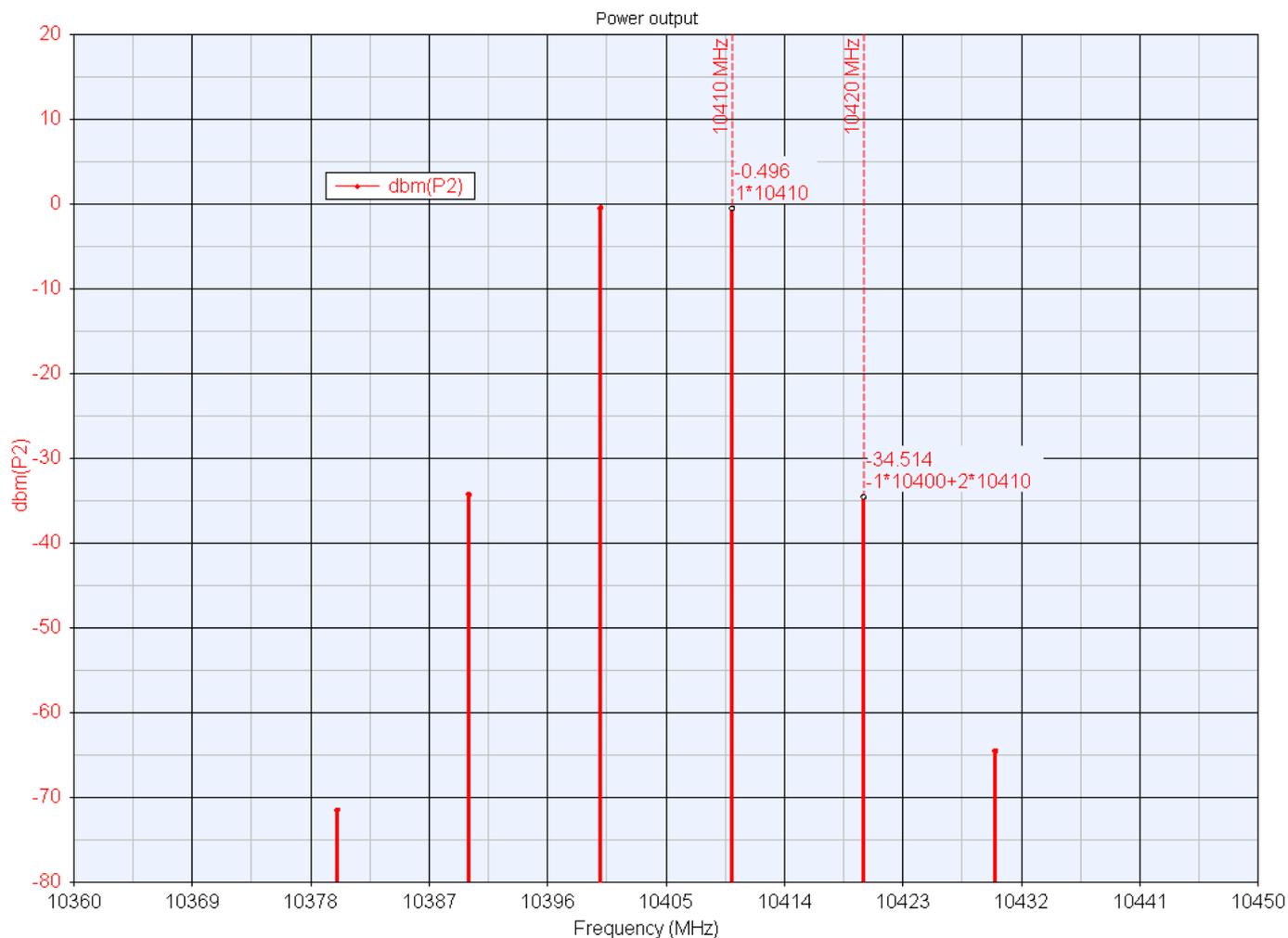
More discussion  
on this later

# Board level design and verification with Genesys Momentum and linear or HB Cosimulation

Momentum is fast, but minimizing runs is key to speeding your design cycle.

- Once the copper is settled (no touching the layout), the momentum dataset will remain valid without a new simulation run
- Use **variables** to tune lumped elements (R's, C's, L's) : this is the one point of reference for the values
  - Do not use the “tuned” option on the schematic elements (for R, L, C, or sources) as they will proliferate and become out of sync with a harbec cosimulation. Tying these to variables in an equation window removes the problem.
    - Reason this is a problem: creating a cosimulation design makes a copy of all non-copper elements on the schematic
- Tuning a value will leave the component type and footprint the same
- Another benefit to putting some of this information in equation blocks is that common parameters (bypass capacitor values for example) is that you can cut and paste them easily between workspaces for projects in the same technology/frequency range.

# Board level design and verification with Genesys Momentum and linear or HB Cosimulation



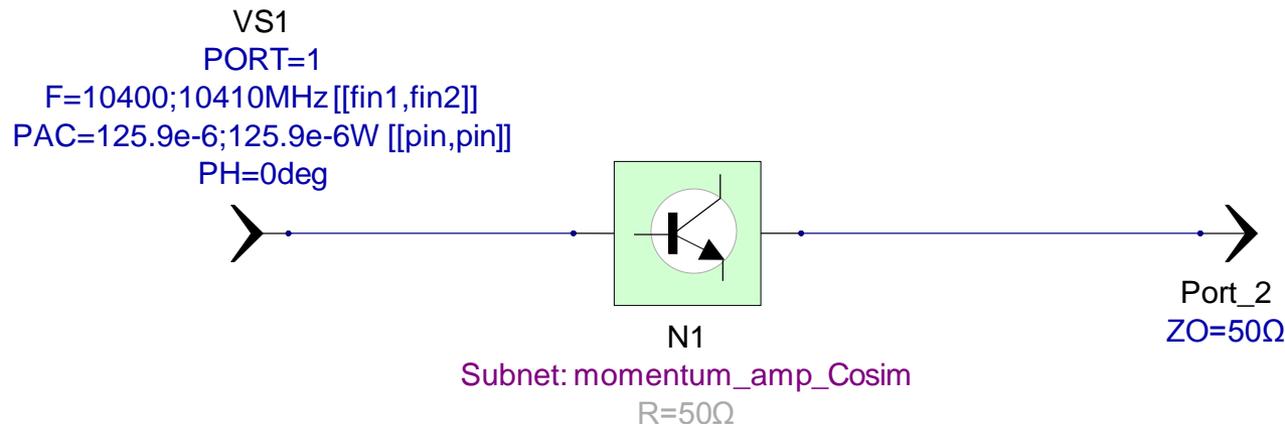
Two tone intermodulation test – this is done using a momentum cosimulation (EM analysis is run on the metal and reconnected to the lumped/nonlinear elements for HB simulation)

Cosim nice for nonlinear circuits since harmonic terminations can be accurately represented

# Board level design and verification with Genesys Momentum and linear or HB Cosimulation

For circuits that you may wish to run several types of analyses on (compression, two-tone intermodulation, etc), consider a “test bench” approach.

- Create a schematic that calls your circuit as a subsystem – your circuit can be a schematic or a momentum cosimulation.
  - Is it clear to users what a “cosimulation design” is?
- This way you can leave your circuit (and the input port connected to it) alone and setup the drive levels/frequencies in each testbench.



# Board level design and verification with Genesys Momentum and linear or HB Cosimulation

Quick switching between transistor models with sub circuits and variables

This is a great trick for reconfiguring circuits on the fly for different analyses: Basically one tuned variable controls the values of several resistors that are used as open or short circuits. In this case, tuning the “s2p” variable  $> 1$  will connect the S2P model data. When “s2p” is  $< 1$ , the nonlinear model is connected.

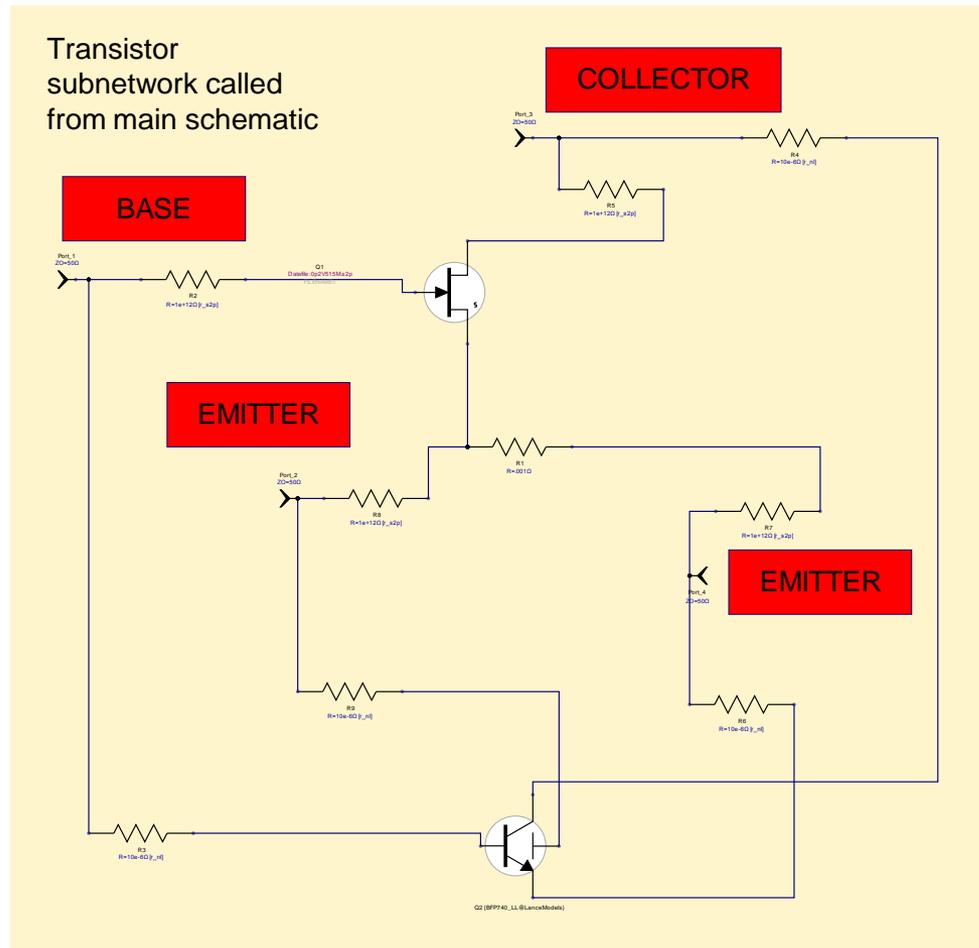
This also shows how the two emitters are connected.

*(workspace equation block)*

`s2p=?0.998`

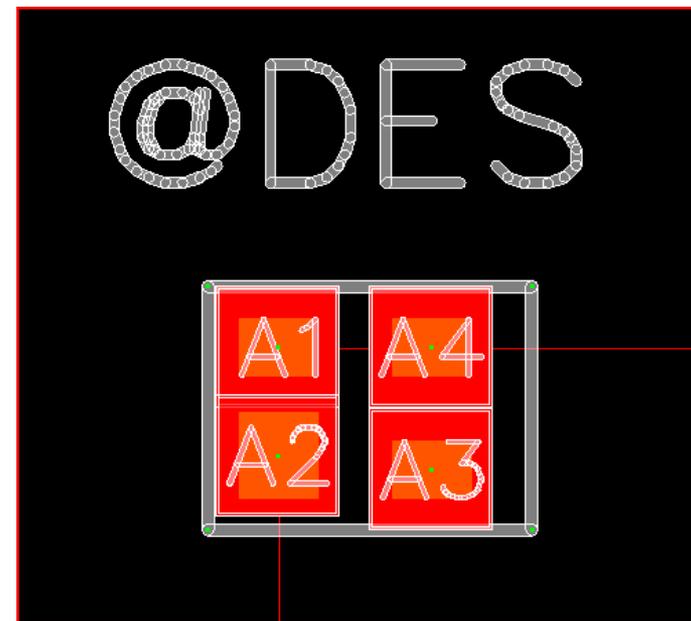
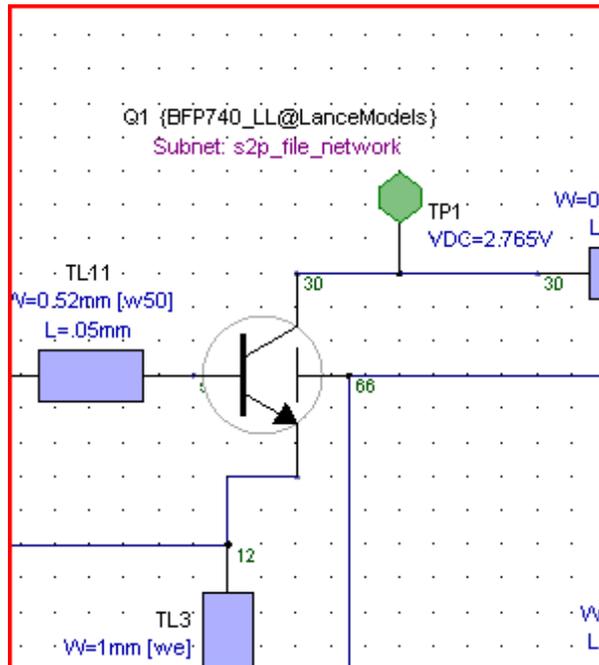
`r_s2p=iff(s2p>1, .00001, 1e12)`

`r_nl=iff(s2p>1, 1e12, .00001)`



# Board level design and verification with Genesys Momentum and linear or HB Cosimulation

- Schematic symbol and footprint below map the model between the schematic/subcircuit/EM data



# Board level design and verification with Genesys

## Amplifier stability analysis and verification

Circuit instability; especially for communications circuits such as Low noise amplifiers and power amplifiers which are exposed to antennas (LNA, PA) represent the largest group of **preventable** problems I see.

The “**it seems to work**” attitude masks so many of these types of problems.

- Testing units exclusively in 50 ohm environment at room temperature.
- You're lucky if you actually see an oscillation occur when looking for it
- Needle in a haystack (temperature, frequency, input/output impedance).
- We need to see roughly \*how\* stable our designs are

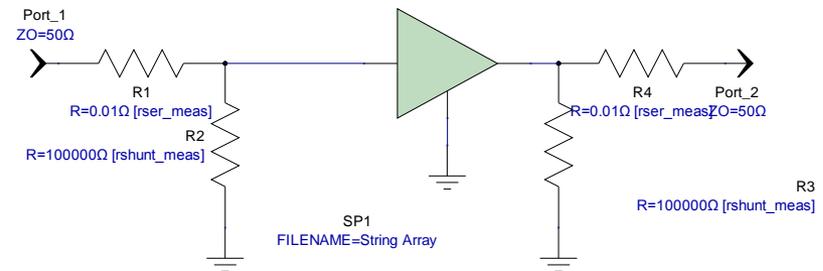
# Board level design and verification with Genesys

## Amplifier stability analysis and verification

I always use measured data as part of a verification step; mainly to compute the stability factors.

There are several ways to gather and use measured data, I prefer to create another linear simulation and subcircuit for the two port data for the following reasons:

1. One point of reference to the data file; all of your graphs and post-processing can “point” to the linear analysis dataset. I often measure and adjust several times so this saves a great deal of effort
2. With the simple schematic such as below you can perform various tests or deembedding. This schematic shows one of our favorite “Litmus” tests for measured data
3. My opinion on the matter is that this verification in situ can be done with coaxial pigtailed to facilitate the measurement of your final hardware; the key is to make an effort to catch stability problems before you ship! By all means, make the best measurement you can, but make the measurement!

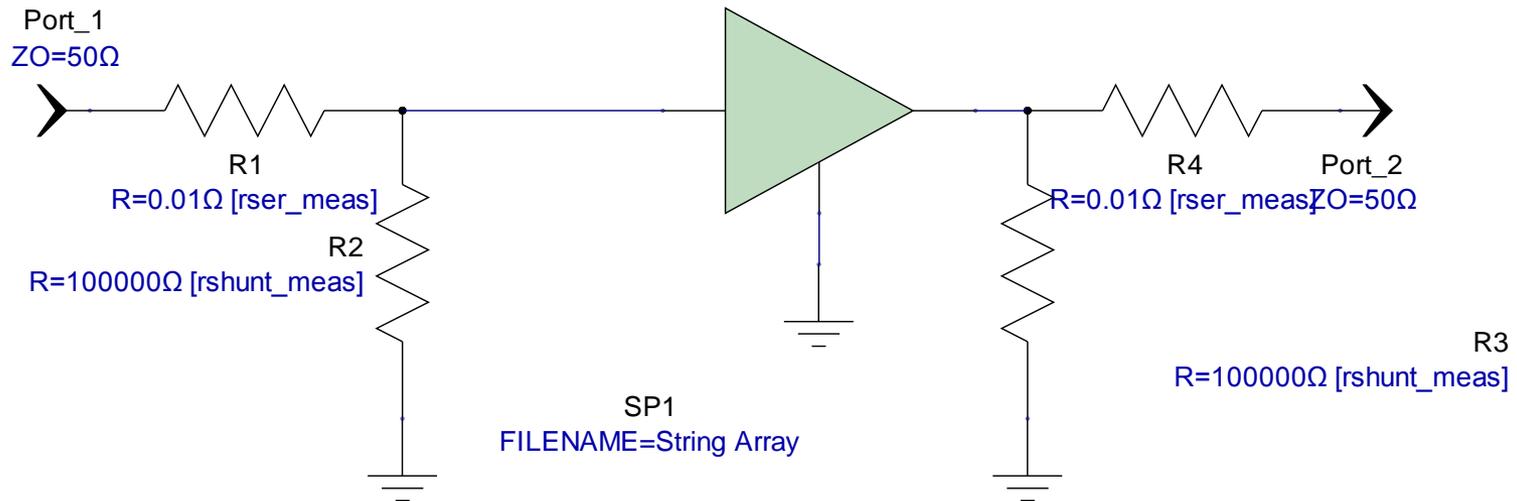


# Board level design and verification with Genesys

## Amplifier stability analysis and verification

Several years ago after insisting on measuring every amplifier built from DC-daylight I realized that noisy measured data could lead to unnecessary concern. For a wide sweep on a narrowband amplifier it is expected that the input and/or output impedance may appear almost completely reflective and with the inaccuracies and noise in measurements this could “compute” as potentially unstable. I’ve even measured barrel connectors that were unstable. So I wanted to come up with a way to sort out the “real” problems.

So my approach to “test” the measured data is to add a tiny bit of loss to see if this cleans up the result. My experience is that typically this does when the instability is far out of band and not “real” – but it rarely does much to any real instability present.

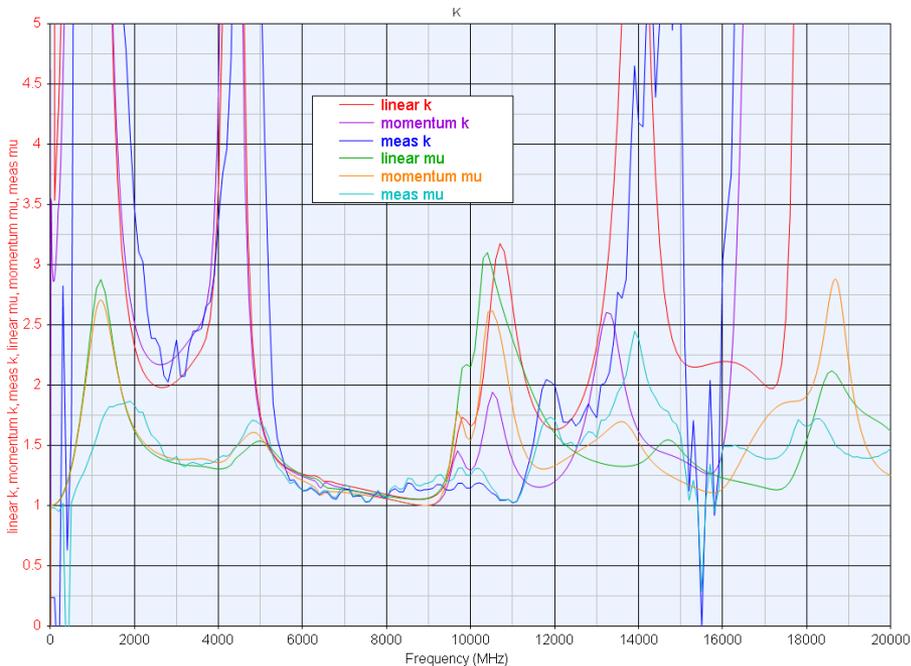


# Board level design and verification with Genesys

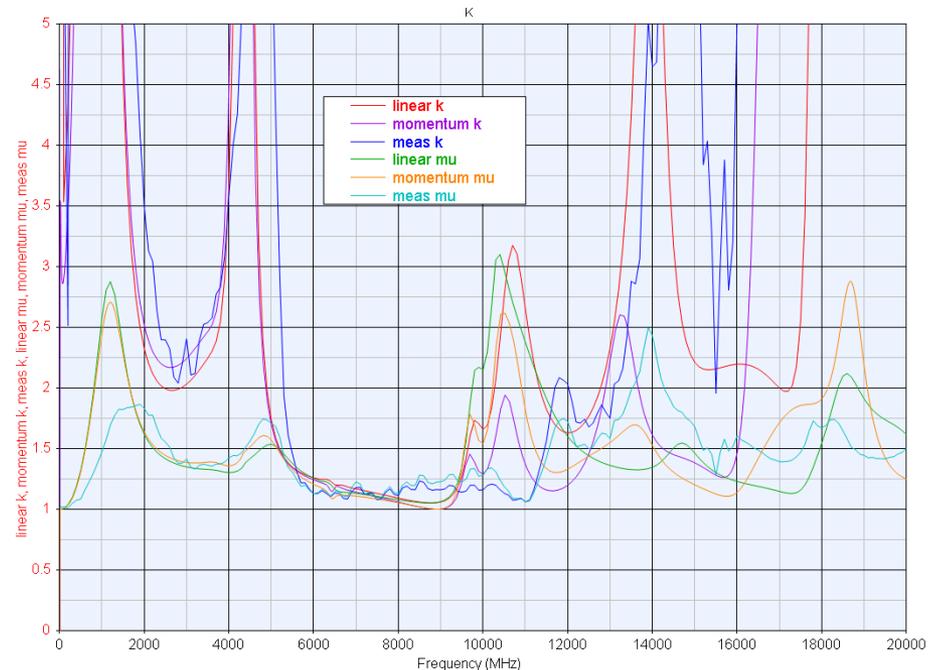
## Amplifier stability analysis and verification

Below is an example of the stability factors computed for a model based simulation, momentum cosimulation and a measured dataset. At first glance there seems to be a serious potential instability based on the measured data near 15 GHz and below 1 GHz. It doesn't take much shunt conductance to completely "stabilize".

Rshunt\_meas=50k



Rshunt\_meas=5k (< ~0.05 dB loss)



# Board level design and verification with Genesys

## Amplifier stability analysis and verification

$\mu$  (mu) is a handy stability factor that is not built into Genesys. It can be added as a equation in a library so it is available at all times. Below is an example implementation.

```
function mu(S)

delt=(S[1,1]*S[2,2])-(S[1,2]*S[2,1])

num=1-abs(S[1,1]*S[1,1])

den=abs(S[2,2]-(conj(S[1,1])*delt)) +abs(S[2,1]*S[1,2])

result=num/den

return result

end
```

# Board level design and verification with Genesys

## Amplifier stability analysis and verification

As long as the equation library is enabled, you can call the “mu” function as shown in the graph dialog to the right.

Note this is the new 2009.04 graph dialogs and shows some mixed (but compatible) syntax as a carry over from previous versions.

See the “Context” column is now separate from the Variable.

The screenshot shows the 'K Properties' dialog box. At the top, there are fields for 'Name: K' and 'Graph Type: Rectangular Graph'. Below that is a 'Graph Heading: K' field and a checked 'Show All Columns' checkbox. The main part of the dialog is a table with the following columns: Context, Variable, Label (Optional), On Right, Hide?, Color, and Type. The table contains six rows of data, with the row for 'mu(S)' selected. Below the table are tabs for 'X-Axis' and 'Y-Axis'. The 'Y-Axis' tab is active, showing options for 'Auto-Scale' (unchecked), 'Logarithmic' (unchecked), 'Min: 0', 'Max: 5', 'Units: None', and '# Divisions: 10'. At the bottom, there are buttons for 'Advanced...', 'OK', 'Cancel', and 'Help'.

		Context	Variable	Label (Optional)	On Right	Hide?	Color	Type
Edit...	Remove	Linear1_Data	k	linear k	<input type="checkbox"/>	<input type="checkbox"/>	Red	General
Edit...	Remove	momentum_amp_d	k	momentum	<input type="checkbox"/>	<input type="checkbox"/>	Purple	General
Edit...	Remove	Linear2_Data	k	meas k	<input type="checkbox"/>	<input type="checkbox"/>	Blue	General
Edit...	Remove	Linear1_Data	mu(S)	linear mu	<input type="checkbox"/>	<input type="checkbox"/>	Green	General
Edit...	Remove	momentum_amp_d	mu(momentum_amp_data	momentum	<input type="checkbox"/>	<input type="checkbox"/>	Orange	General
Edit...	Remove	Linear2_Data	mu(S)	meas mu	<input type="checkbox"/>	<input type="checkbox"/>	Cyan	General

# Board level design and verification with Genesys

## Amplifier stability analysis and verification

Let us discuss our favorite tricks for stabilizing small signal amplifiers. Here are a few of mine that we can show in the example design:

- “skimping” on the collector/drain bypass capacitor in a LNA
- Splitting resistors in the bias and feedback networks to remove the stub-effects
- Resistor to copper pad trick.
- Negative inductance in source/emitter leads -- discuss

# Board level design and verification with Genesys

## Reference planes in EM simulation of active circuits

Reference planes are basically the equivalent physical points on the device (footprint) where the electrical model connects. For many vendors this reference point is at the side of the package, for others it is the end of the leads. Basically we will need to ASK if it is not specified.

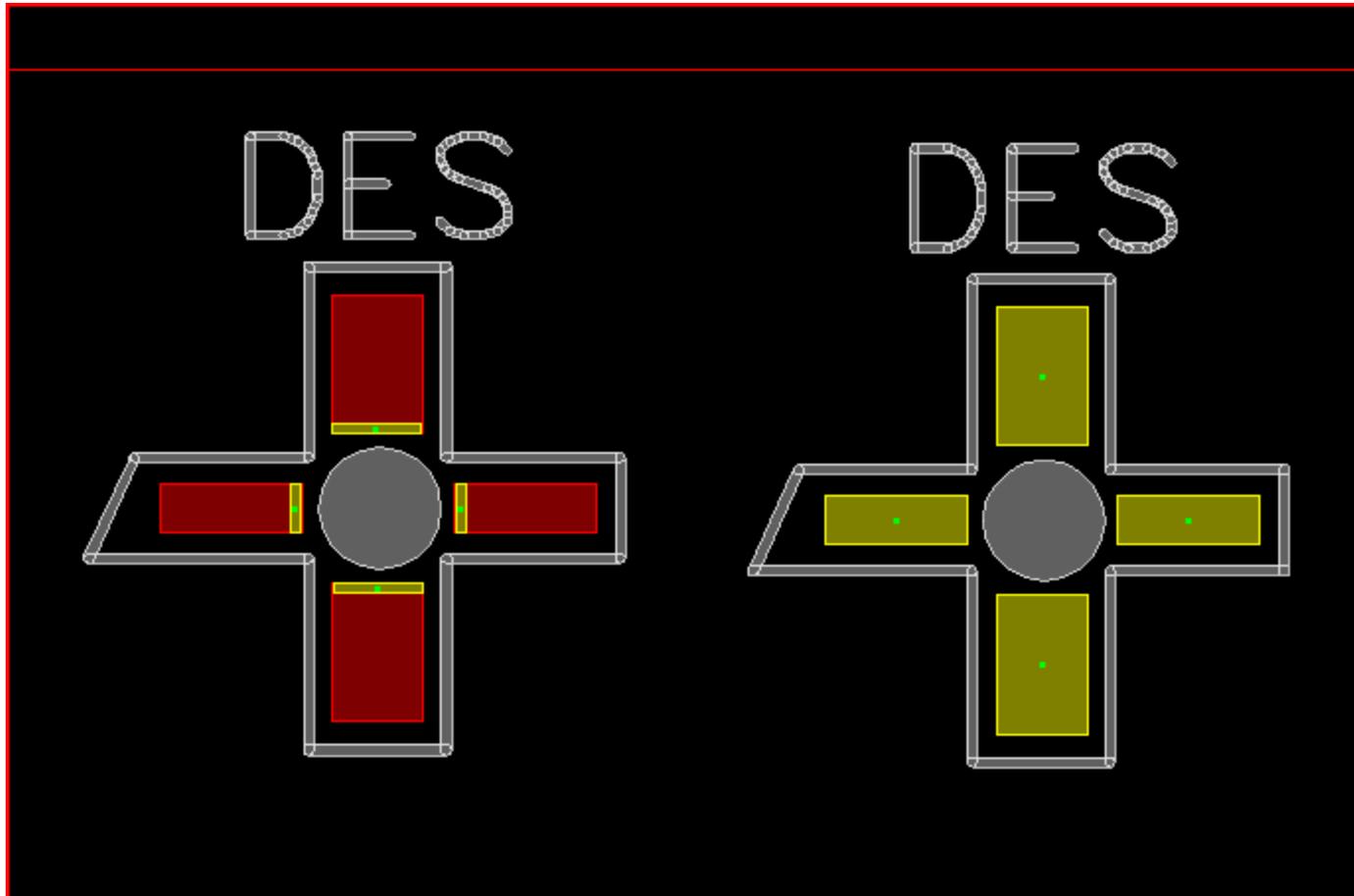
Making the wrong assumption here, as I did recently, can be fairly catastrophic.

In the next slide I'll show two footprints for the same device and we can discuss the differences. The default footprints provided with Genesys may not always be the best choices for your design.

- “Understanding Reference Planes for Device Packages” (Eagleware appnote from 2002 that I authored).
- <http://cp.literature.agilent.com/litweb/pdf/5989-8905EN.pdf>

# Board level design and verification with Genesys

## Reference planes in EM simulation of active circuits



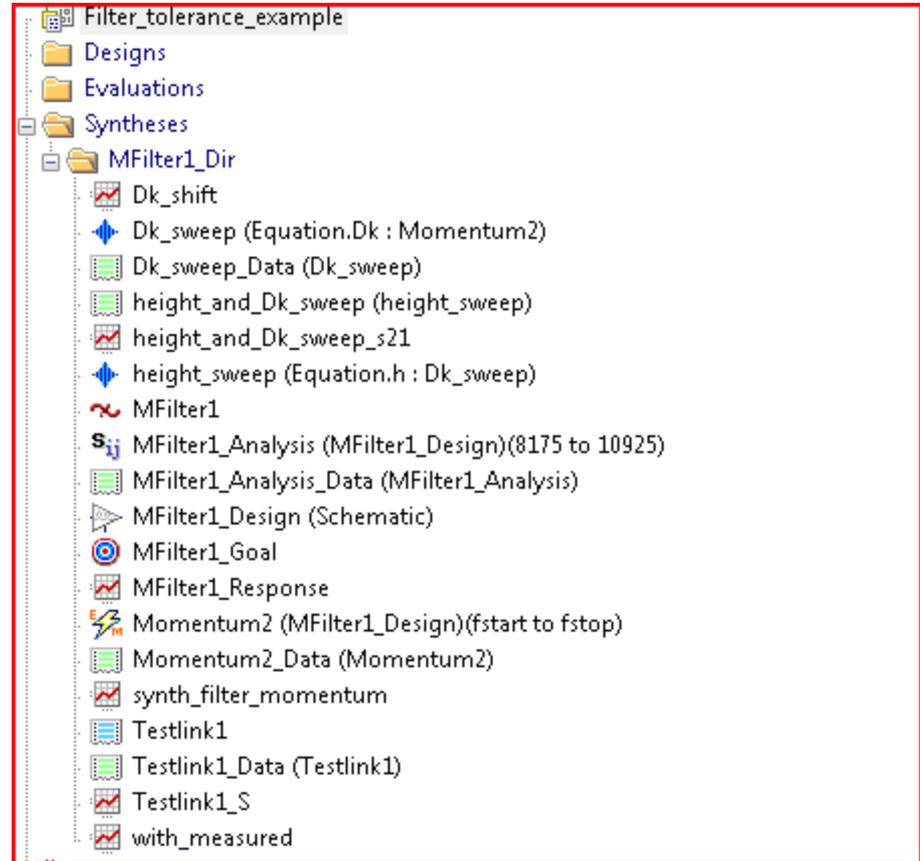
# Board level design and verification with Genesys

## Tolerance analysis in printed filters

Tolerance analysis for circuits is straightforward in Genesys. For circuits that model well with built-in models for coupling and discontinuities; a monte-carlo / yield analysis is probably best.

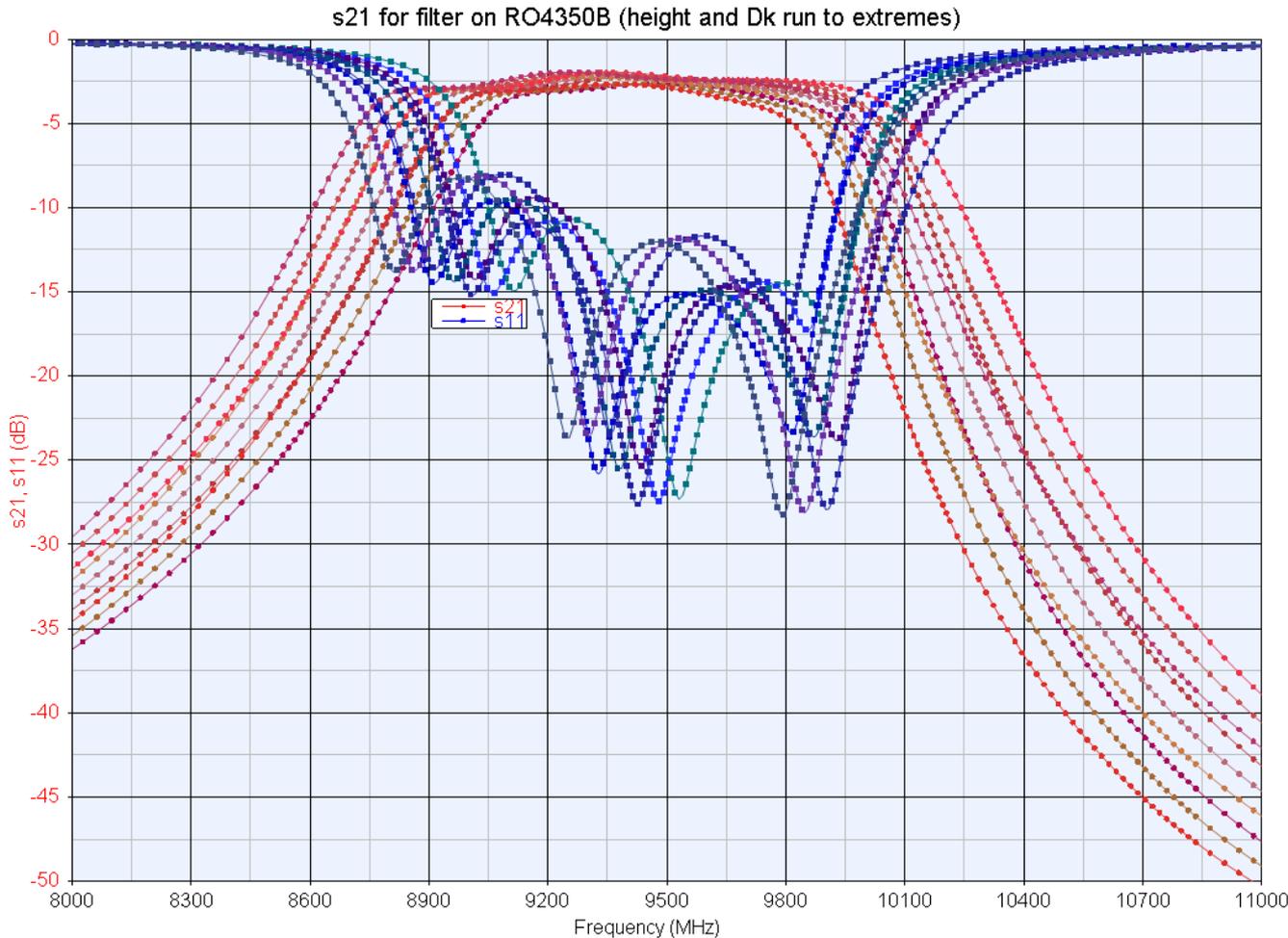
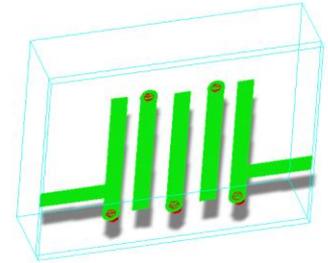
For “custom” and particularly EM-intensive filters, brute force may be the best way using parameter sweeps.

Parameter sweeps are like programming loops – very simple to use.



# Board level design and verification with Genesys

## Tolerance analysis in printed filters



This brute-force technique using nested parameter sweeps is probably the most efficient method for verifying the effect of material properties on the filter response. It could be expanded further to include the copper tolerances as well. This analysis was performed to look specifically at board material tolerance.

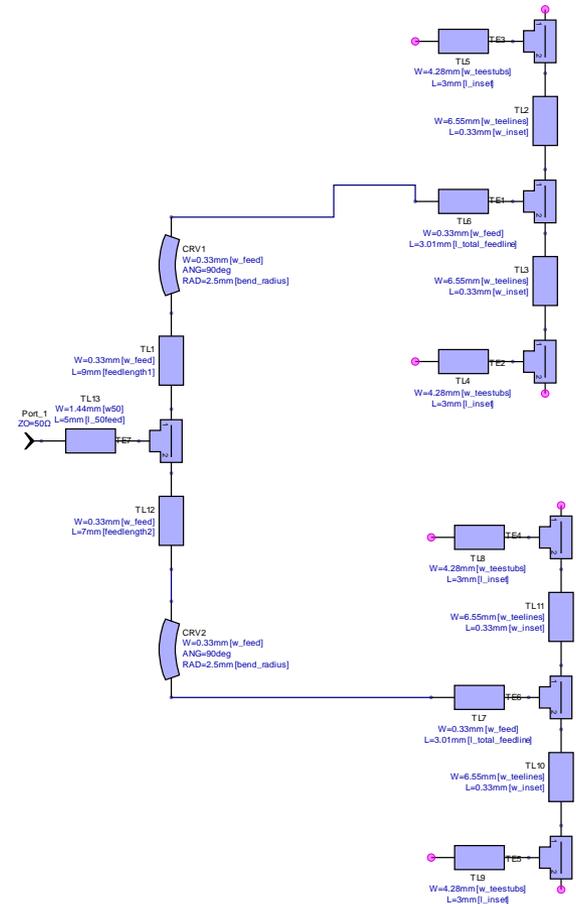
# Board level design and verification with Genesys

## Patch antenna radiation patterns

3D antenna patterns available with Momentum GX makes it much simpler to determine antenna performance.

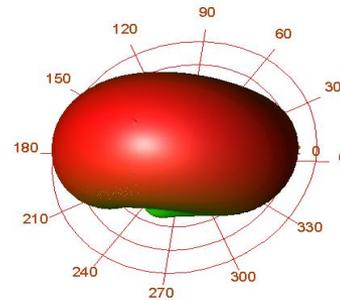
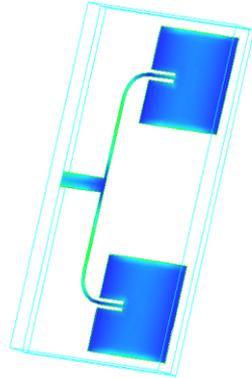
Very nice to be able to view the antenna structure in 3D with the same coordinate axes as the 3D radiation plot. This allows easier diagnosis of anomalies and is inherently more intuitive.

Next we'll discuss a very simple example of how we can identify simple defects in our antennas by viewing the patterns.

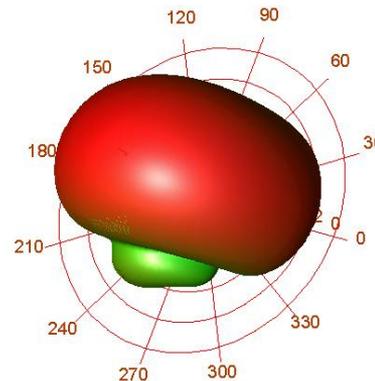
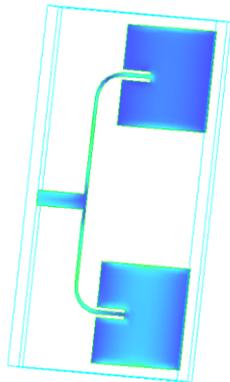


# Board level design and verification with Genesys

## Patch antenna radiation patterns: effect of asymmetry in feed of 7.5 GHz two patch array



The upper antenna is “normal”

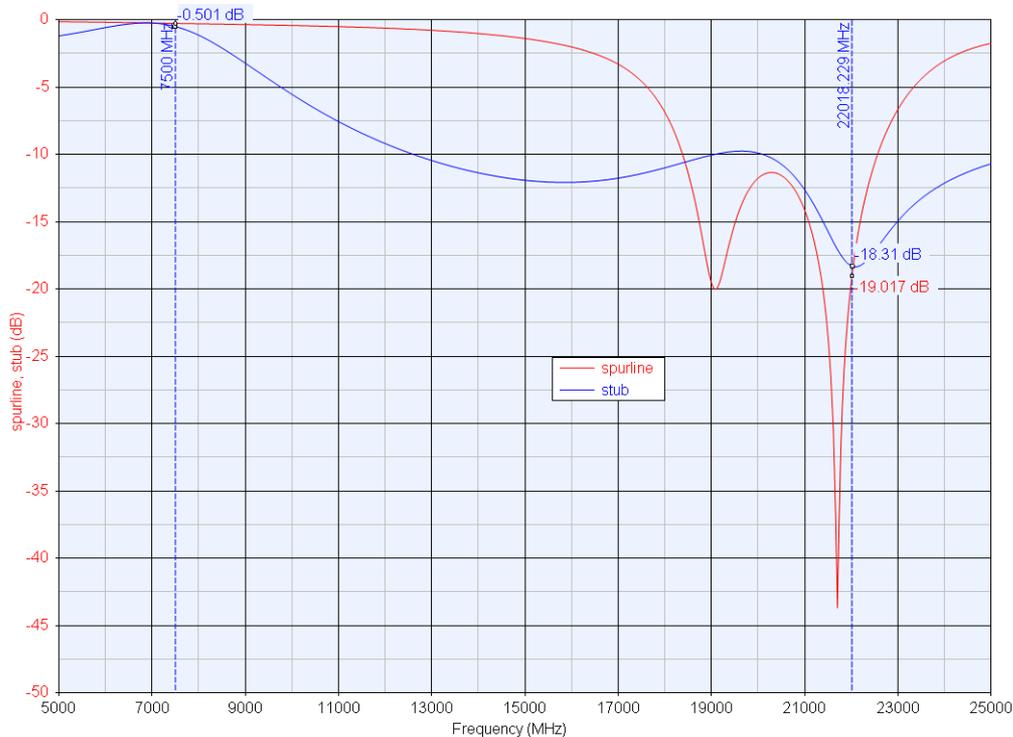


The lower antenna has a 1mm offset in the feed network, causing a slight uptilt with the side effect of a grating lobe

# Board level design and verification with Genesys

## Unintentional radiation from microstrip structures

Below is a plot of the response of two notch filters (not very good ones) with 18-19 dB of rejection at 22 GHz.



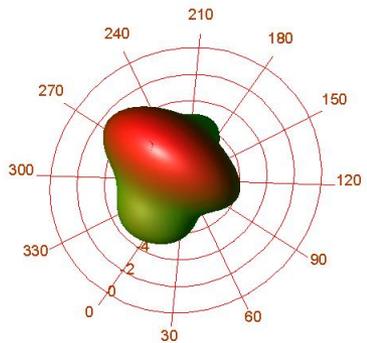
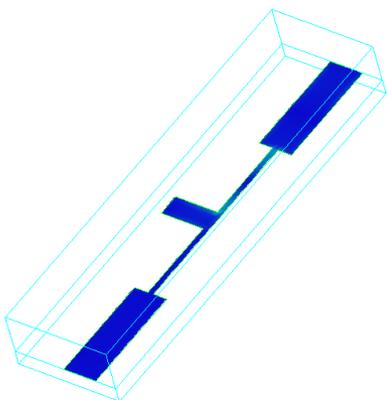
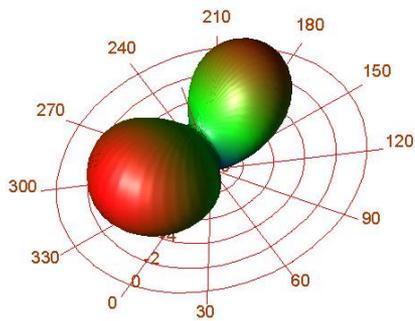
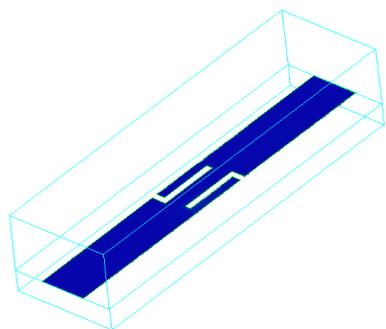
As far as containing spurious, if the conducted path through the filter is the only outlet for this energy, these two filters should perform quite similarly.

Now we'll look at how these filters interact with their environment.

# Board level design and verification with Genesys

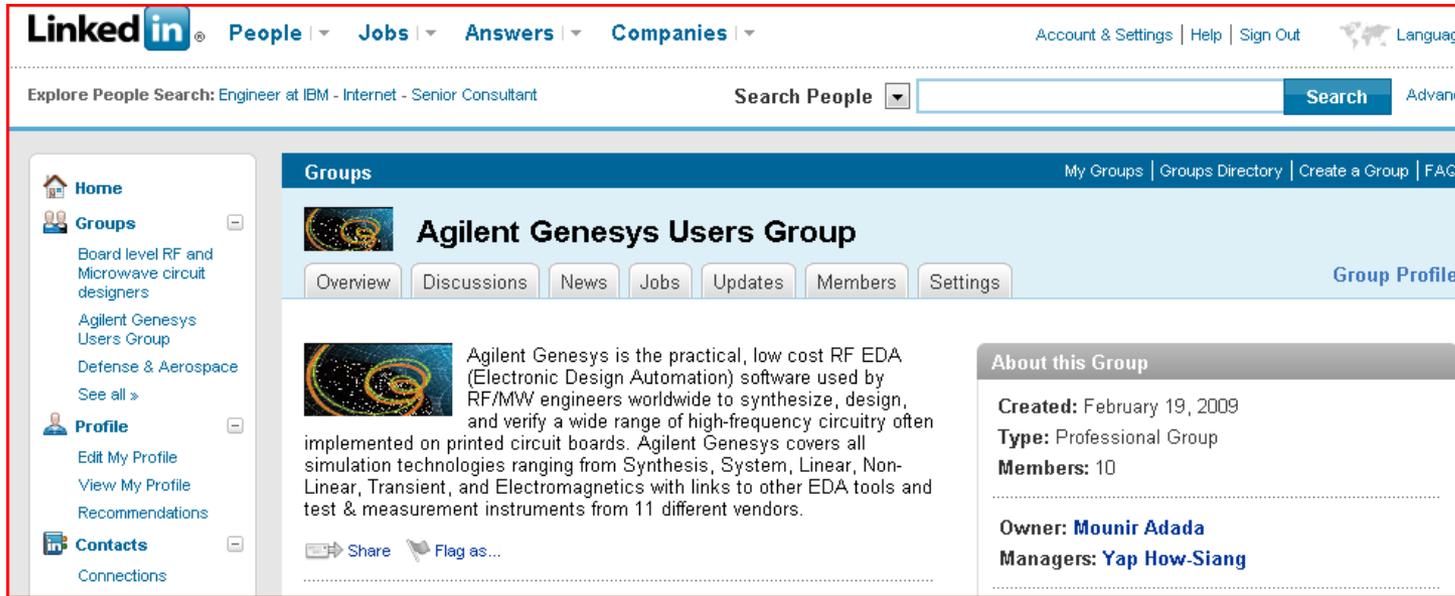
## Unintentional radiation from microstrip structures

Note the differences in radiation pattern (direction) for these filters (@22 GHz)



# Board level design and verification with Genesys

## Join our LinkedIn group!



The screenshot shows the LinkedIn interface for the "Agilent Genesys Users Group". The top navigation bar includes "People", "Jobs", "Answers", and "Companies". The search bar contains the text "Engineer at IBM - Internet - Senior Consultant". The group page features a navigation menu with "Overview", "Discussions", "News", "Jobs", "Updates", "Members", and "Settings". The main content area includes a description of Agilent Genesys as a practical, low-cost RF EDA software used by RF/MW engineers worldwide. The "About this Group" section lists the group's creation date (February 19, 2009), type (Professional Group), and members (10). The owner is Mounir Adada and the manager is Yap How-Siang.



[www.linkedin.com](http://www.linkedin.com)

Another group of interest that I started is  
“[Board level RF and Microwave circuit designers](#)”

# Board level design and verification with Genesys

## Summary & Follow-up

We hope that today's discussions have been useful and that MANY ideas have been shared both between Genesys users and with the Agilent team. User input has been a strong force in shaping Genesys over the years that I've used it – so do not hold back on your feedback!

Please do not hesitate to contact me if you have questions about the techniques presented here or about work that we might be able to help your company with in the future.

Thank you for participating!

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