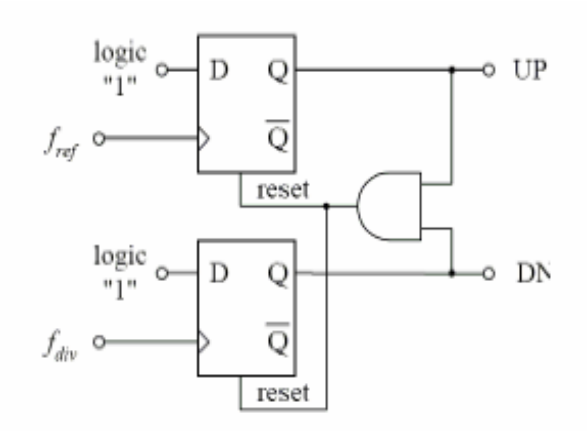
PHASE FREQUENCY DETECTOR (PFD) RIBFD01

Description

A low-power Phase Frequency detector (PFD) data-sheet is presented. The circuit's building blocks: two D Flip -Flop, inverter and NAND gate for reset Flip-Flop; were designed using high-performance Dead –Zone free circuit. The D Flip-Flop compare input frequency and Divided Frequency with phase and frequency. If input frequency is greater than divided frequency compare output is present at upper D Flip-Flop and lower D Flip-Flop output is "0". Similarly If input frequency is lower than divided frequency compare output is present at lower D Flip-Flop and upper D Flip-Flop output is "0".Phase frequency Detector was designed using the 0.18-um CMOS technology.

Functional Diagram



Applications

- PLL
- Frequency Synthesizers

Electrical Specification

Conditions: Vcc = 1.8 V & T_A=25 ^{0}C

Descriptions	Min.	Typ.	Max.	Units
Frequency Range	30	40	50	MHz
Power supply		1.8		V
Phase noise	< –160@10 KHz offset			dBc/Hz
Rise Time				ps
Fall Time				

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Simulated Results

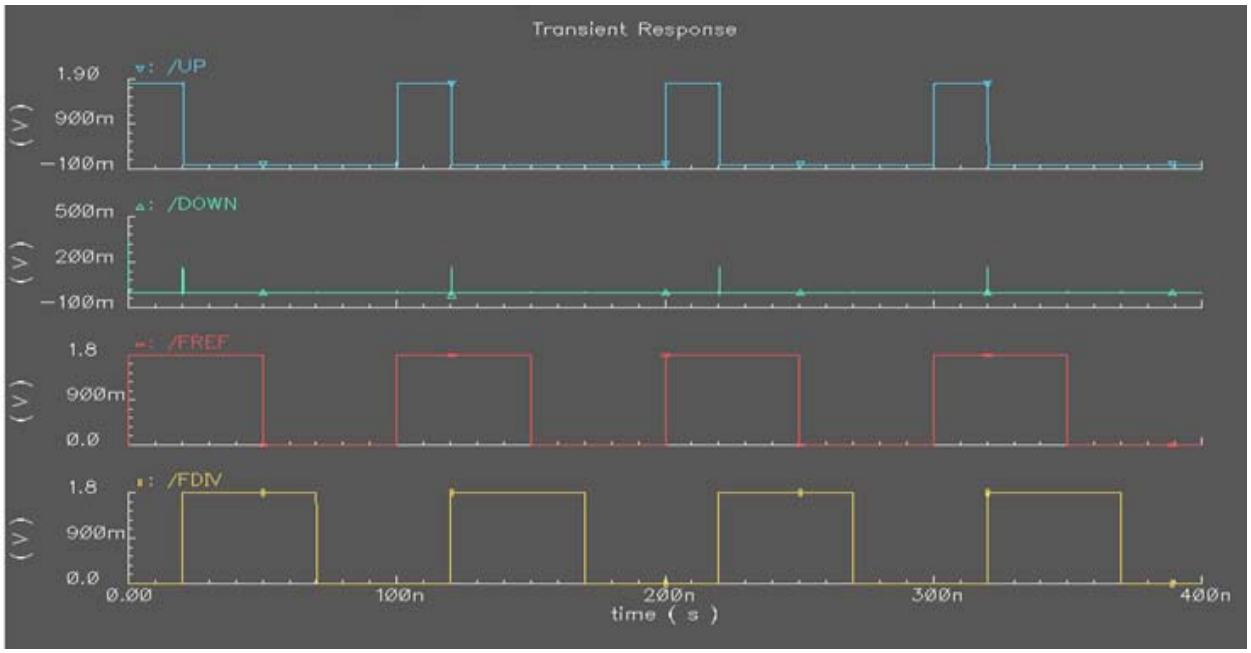

FIGURE: Phase Frequency Detector output with dead zone free (Fin > Fdiv)