Low Speed, low power Receiver IP

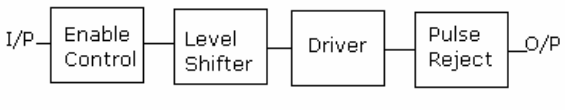
RCLRX01

Description

The RCLRX01 is low power, low voltage Receiver IP designed using 0.18um CMOS process. It can be configured and interfaced with other CMOS PHY IPs for performing the controlling functions. It can receive the low frequency control signals to various other PHY blocks.

The Low-Power Receiver is a slew-rate controlled push-pull driver. It supports **20Mbps** speed.

Functional Diagram



Applications

- Control signal Receivers in PHY
- Clock Drivers
- Data Tx/Rx PHY

Key Features

- Low Power CMOS Design
- Power down mode
- Reconfigurable for use in various high speed PHY designs for control signal reception.
- Easily portable to other CMOS foundries

DC Specifications:

Parameter	Description	Min	Nom	Max	Units
V_{IH}	Logic 1 input voltage	880			mV
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV