



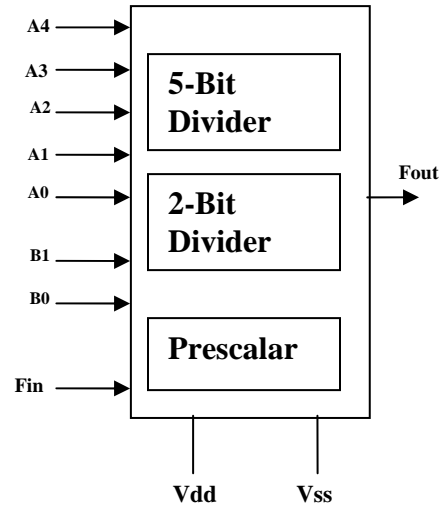
Dual Modulus Programmable Frequency Divider

RFPD01

Description

A low-power high-speed programmable dual modulus divider data-sheet is presented. The circuit's three building blocks: prescaler, 2-bit and 5-bit programmable dividers; were designed using high-performance single-phase clocking latchup circuits rather than the conventional latchup circuits widely used in digital systems. The dividers operate based on the modulus control and parallel loading concepts, capable of operating within the division ratio of 16 - 127. The programmable dual-modulus divider with 1.5 GHz maximum operating frequency was designed using the 0.18-um CMOS technology. Post parasitic-extracted layout results verify that the total power dissipation was 1.8 mW (at 1.5 GHz, 1.8 V).

Functional Diagram



Applications

- PLL
- Mobile Communication
- Frequency Synthesizers

Electrical Specification

Conditions: Vcc = 1.8 V & TA=25 °C

Name	Value
Power Supply	1.8 V
Maximum Power Dissipation	1.8 mW
Maximum Frequency Allowed	1.5 GHz
Technology	0.18 um CMOS
Division Ratio	16 to 127
Chip Size	244 X 115 um



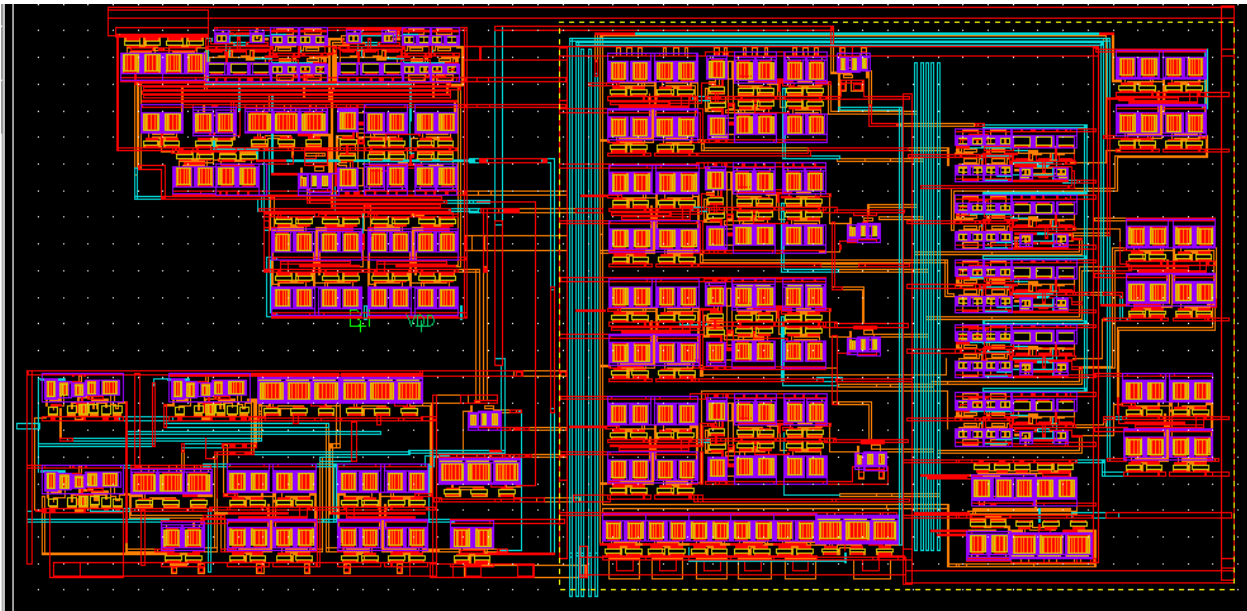
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Future Scope

Since RFIC has used True Single Phase Clock scheme to design the latchup circuits used in the 2-bit, 5-bit programmable dividers and the prescaler, RFIC can extend the maximum frequency allowed for high speed operation as required.

Chip Layout





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The Programming Table for Dual Modulus Programmable Frequency Divider

Note:- A constraint in the two programmed input values is that N1COUNTER (A4,A3,A2,A1,A0) value must always be greater than N2COUNTER (B1,B2) value.

5 Bit Programming Word					Decimal (A)	2 Bit Programming Word		Decimal (B)	Prescaler P/P+1	Overall Division Ratio N=A.P +B		
A4	A3	A2	A1	A0		B1	B0					
0	1	0	0	0	8	0	0	0	4	32		
						0	1				1	33
						1	0				2	34
						1	1				3	35
0	1	0	0	1	9	0	0	0	4	36		
						0	1				1	37
						1	0				2	38
						1	1				3	39
0	1	0	1	0	10	0	0	0	4	40		
						0	1				1	41
						1	0				2	42
						1	1				3	43
0	1	0	1	1	11	0	0	0	4	44		
						0	1				1	45
						1	0				2	46
						1	1				3	47
0	1	1	0	0	12	0	0	0	4	48		
						0	1				1	49
						1	0				2	50
						1	1				3	51
0	1	1	0	1	13	0	0	0	4	52		
						0	1				1	53
						1	0				2	54
						1	1				3	55
0	1	1	1	0	14	0	0	0	4	56		
						0	1				1	57
						1	0				2	58
						1	1				3	59
0	1	1	1	1	15	0	0	0	4	60		
						0	1				1	61
						1	0				2	62
						1	1				3	63
1	0	0	0	0	16	0	0	0	4	64		



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						0	1	1		65
						1	0	2		66
						1	1	3		67
1	0	0	0	1	17	0	0	0	4	68
						0	1	1		69
						1	0	2		70
						1	1	3		71
1	0	0	1	0	18	0	0	0	4	72
						0	1	1		73
						1	0	2		74
						1	1	3		75
1	0	0	1	1	19	0	0	0	4	76
						0	1	1		77
						1	0	2		78
						1	1	3		79
1	0	1	0	0	20	0	0	0	4	80
						0	1	1		81
						1	0	2		82
						1	1	3		83
1	0	1	0	1	21	0	0	0	4	84
						0	1	1		85
						1	0	2		86
						1	1	3		87
1	0	1	1	0	22	0	0	0	4	88
						0	1	1		89
						1	0	2		90
						1	1	3		91
1	0	1	1	1	23	0	0	0	4	92
						0	1	1		93
						1	0	2		94
						1	1	3		95
1	1	0	0	0	24	0	0	0	4	96
						0	1	1		97
						1	0	2		98
						1	1	3		99
1	1	0	0	1	25	0	0	0	4	100
						0	1	1		101
						1	0	2		102
						1	1	3		103
1	1	0	1	0	26	0	0	0	4	104
						0	1	1		105
						1	0	2		106
						1	1	3		107
1	1	0	1	1	27	0	0	0	4	108
						0	1	1		109
						1	0	2		110
						1	1	3		111



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1	1	1	0	0	28	0	0	0	4	112
						0	1	1		113
						1	0	2		114
						1	1	3		115
1	1	1	0	1	29	0	0	0	4	116
						0	1	1		117
						1	0	2		118
						1	1	3		119
1	1	1	1	0	30	0	0	0	4	120
						0	1	1		120
						1	0	2		122
						1	1	3		123
1	1	1	1	1	31	0	0	0	4	124
						0	1	1		125
						1	0	2		126
						1	1	3		127



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Simulated Results

Divide by 32

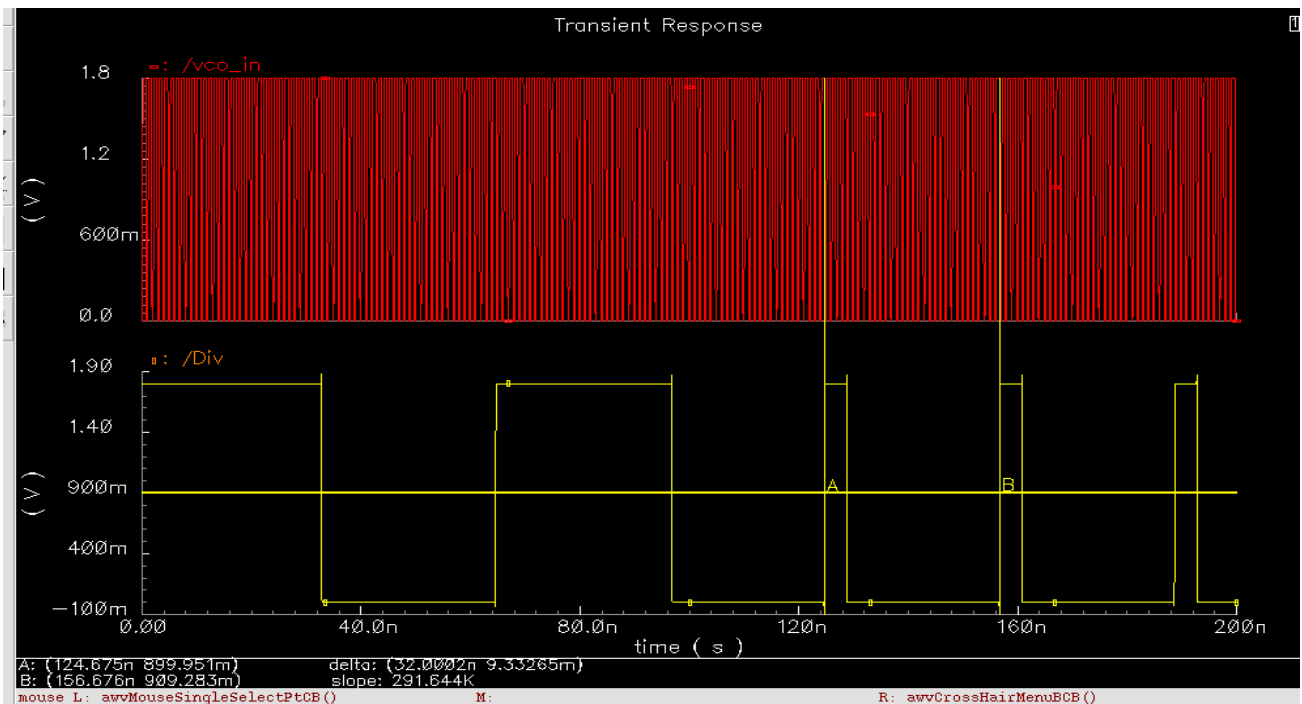


Figure 1: Divide by 32

Figure 1 shows the simulation result for divide by 32.

The values programmed are A4 = 0, A3 = 1, A2 = 0, A1 = 0, A0 = 0, B1 = 0, B0 = 0, as can be referenced from the programming table for the dual modulus programmable divider.



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Divide by 67

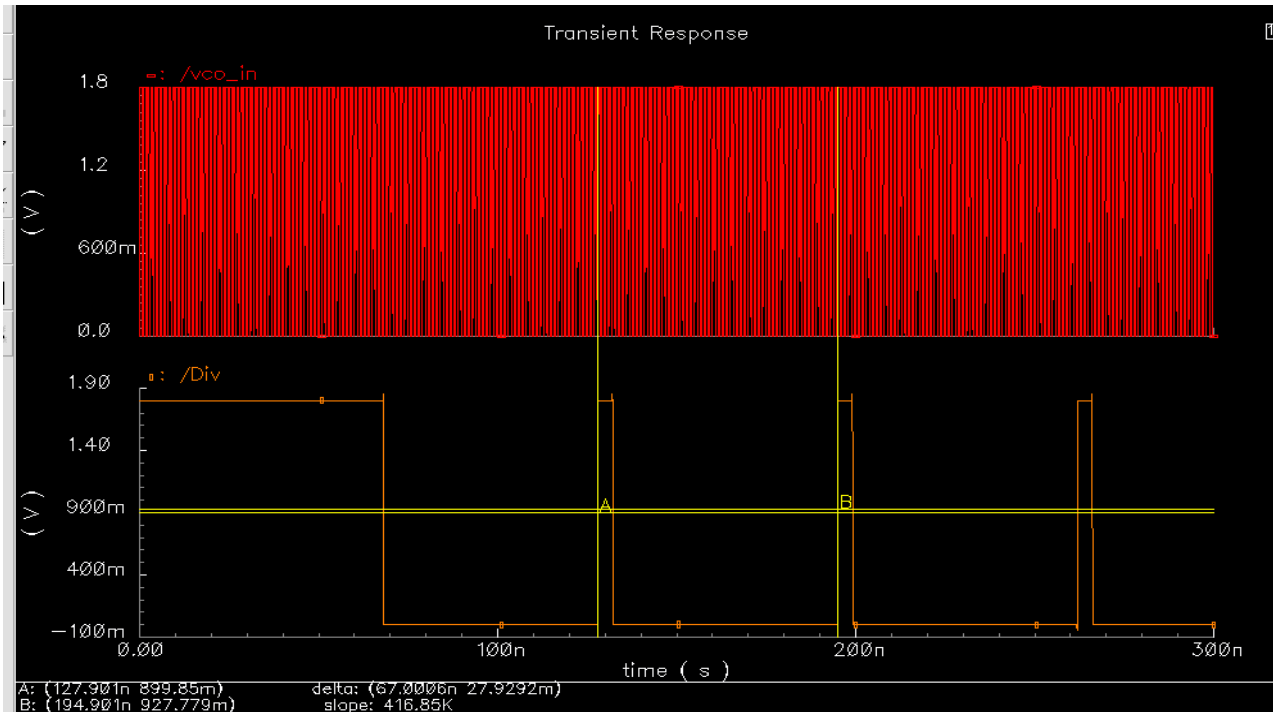


Figure 2: Divide by 67

Figure 2 shows the simulation result for divide by 67.

The values programmed are A4 = 1, A3 = 0, A2 = 0, A1 = 0, A0 = 0, B1 = 1, B0 = 1, as can be referenced from the programming table for the dual modulus programmable divider.