**TECHNICAL DATA**
**Data Sheet 4098, Rev. D.1**

# Three-Phase IGBT BRIDGE, With Gate Driver and Optical Isolation

**DESCRIPTION:** A 600 VOLT, 80 AMP, THREE PHASE IGBT BRIDGE

**ELECTRICAL CHARACTERISTICS PER IGBT DEVICE** ($Tj=25^0C$ UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **IGBT SPECIFICATIONS** | | | | | |
| Collector to Emitter Breakdown Voltage<br>$I_C$ = 250 μA, $V_{GE}$ = 0V | $BV_{CES}$ | 600 | - | - | V |
| Continuous Collector Current $T_C$ = 25 °C<br>$T_C$ = 90 °C | $I_C$ | - | - | 80<br>70 | A |
| Pulsed Collector Current, 1mS | $I_{CM}$ | - | - | 170 | A |
| Gate to Emitter Voltage | $V_{GE}$ | - | - | +/-20 | V |
| Gate-Emitter Leakage Current , $V_{GE}$ = +/-20V | $I_{GES}$ | - | - | +/- 100 | nA |
| Zero Gate Voltage Collector Current<br>$V_{CE}$ = 600 V, $V_{GE}$=0V $T_i$=25°C<br>$V_{CE}$ = 480 V, $V_{GE}$=0V $T_i$=125°C | $I_{CES}$ | - | - | <br>1<br>10 | <br>mA<br>mA |
| Collector to Emitter Saturation Voltage, $T_C$ = 25 °C<br>$I_C$ = 60A, $V_{GE}$ = 15V, | $V_{CE(SAT)}$ | - | 1.7 | 2.0 | V |
| Maximum Thermal Resistance | $R_{\theta JC}$ | - | - | 0.45 | °C/W |
| **Brake IGBT SPECIFICATIONS** | | | | | |
| Continuous Collector Current $T_C$ = 25 °C<br>$T_C$ = 90 °C | $I_C$ | - | - | 40<br>25 | A |
| Pulsed Collector Current, 0.5mS | $I_{CM}$ | - | - | 120 | A |
| **Brake Resistor SPECIFICATIONS** | | | | | |
| Maximum Continuous power dissipation | Pd | | | 2 | watt |
| Impulse Energy | | | | 80 | Joules |
| Maximum operating Junction Temperature | $T_{jmax}$ | -40 | - | 150 | °C |
| Maximum Storage Junction Temperature | $T_{jmax}$ | -55 | - | 150 | °C |

| Over-Temperature Shutdown | | | | | |
|---|---|---|---|---|---|
| Over-Temperature Shutdown | Tsd | 100 | 110 | 120 | $^{o}$C |
| Over-Temperature Output | Tso | | 10 | | 10mV/$^{o}$C |
| Over-Temperature Shutdown Hysteresis | | | 20 | | $^{o}$C |

| ULTRAFAST DIODES RATING AND CHARACTERISTICS | | | | | |
|---|---|---|---|---|---|
| Diode Peak Inverse Voltage | PIV | 600 | - | - | V |
| Continuous Forward Current, $T_C$ = 90 $^{O}$C | $I_F$ | - | - | 60 | A |
| Forward Surge Current, $t_p$ = 10 msec | $I_{FSM}$ | - | - | 300 | A |
| Diode Forward Voltage, $I_F$ = 60A | $V_F$ | - | 1.4 | 1.7 | V |
| Diode Reverse Recovery Time ($I_F$=60A, $V_{RR}$=300V , di/dt=200 A/μs) | $t_{rr}$ | - | 90 | 160 | nsec |
| Maximum Thermal Resistance | $R_{\theta JC}$ | - | - | 0.8 | $^{o}$C/W |
| **Gate Driver** | | | | | |
| Supply Voltage | VCC | 10 | 15 | 20 | V |
| Input On Current | HIN, LIN | 2 | | 5.0 | mA |
| Opto-Isolator Logic High Input Threshold | $I_{th}$ | - | 1.6 | - | mA |
| Input Reverse Breakdown Voltage | $BV_{in}$ | 5.0 | - | - | V |
| Input Forward Voltage @ $I_{in}$ = 5mA | $V_F$ | - | 1.5 | 1.7 | V |
| Under Voltage Lockout | VCCUV | 11.5 | - | 12.5 | V |
| ITRIP Reference Voltage (1) | Itrip-ref | 2.9 | 3.0 | 3.1 | V |
| Input-to-Output Turn On Delay | $t_{ond}$ | - | | 800 | nsec |
| Output Turn On Rise Time | $t_r$ | - | | 100 | |
| Input-to-Output Turn Off Delay | $t_{offd}$ | - | | 1000 | |
| Output Turn Off Fall Time @ VCC=300V, IC=50A, $T_C$ = 25 | $t_f$ | | | 100 | |
| Input-Output Isolation Voltage | - | 1000 | - | - | V |

(1) ITRIP Cycle-by cycle current limit is internally set to 70A peak. The set point can be lowered by connecting a resistor between Itrip-ref and Gnd. The set point can be increased by connecting a resistor between Itrip-ref and +5V ref

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## Pin Description

| Pin Number | Function | | Pin Number | Function |
|---|---|---|---|---|
| 1 | Isolated Input for Low-side IGBT of Phase A | | 17 | +15V Rtn (Signal Ground) |
| 2 | Return for Input at 1 | | 18 | Fault Output (3) |
| 3 | Isolated Input for High-side IGBT of Phase A | | 19 | Fault Clear Input (3) |
| 4 | Return for Input at 3 | | 20 | +5V Output |
| 5 | Isolated Input for Low -side IGBT of Phase B | | 21 | Over-Current Trip Set point (3) |
| 6 | Return for Input at 5 | | 22 | DC Bus Current Output with Total Gain of 0.0365 V/A |
| 7 | Isolated Input for High-side IGBT of Phase B | | 23 | Case Temperature Output with a gain of 0.010 V/$^{o}$C |
| 8 | Return for Input at 7 | | 24 | Brake IGBT Gate Input |
| 9 | Isolated Input for Low-side IGBT of Phase C | | 25 | Brake IGBT Emitter Input. This input is internally connected to Signal Ground |
| 10 | Return for Input at 9 | | 26 to 30 | DC Bus return |
| 11 | Isolated Input for High-side IGBT of Phase C | | 31 , 32 | Brake Resistor Terminal. Brake Resistor Shall be Connected Between These Terminals and +VDC |
| 12 | Return for Input at 11 | | 33 to 37 | DC Bus “+VDC” input |
| 13 | NC | | 38 to 42 | Phase C output |
| 14 | NC | | 43 to 47 | Phase B output |
| 15 | SD (3) | | 48 to 52 | Phase A output |
| 16 | +15V Input | | Case | Isolated |

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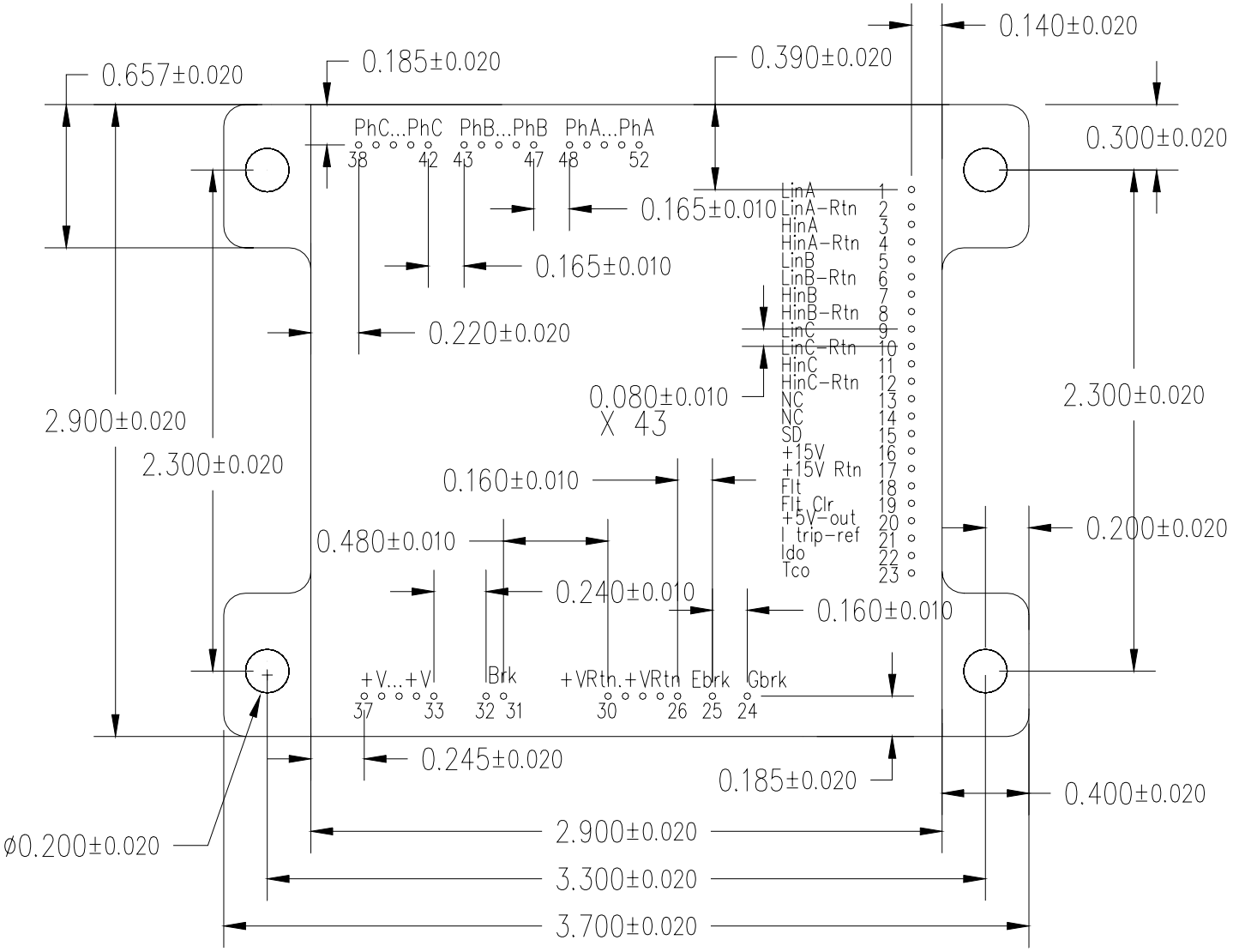
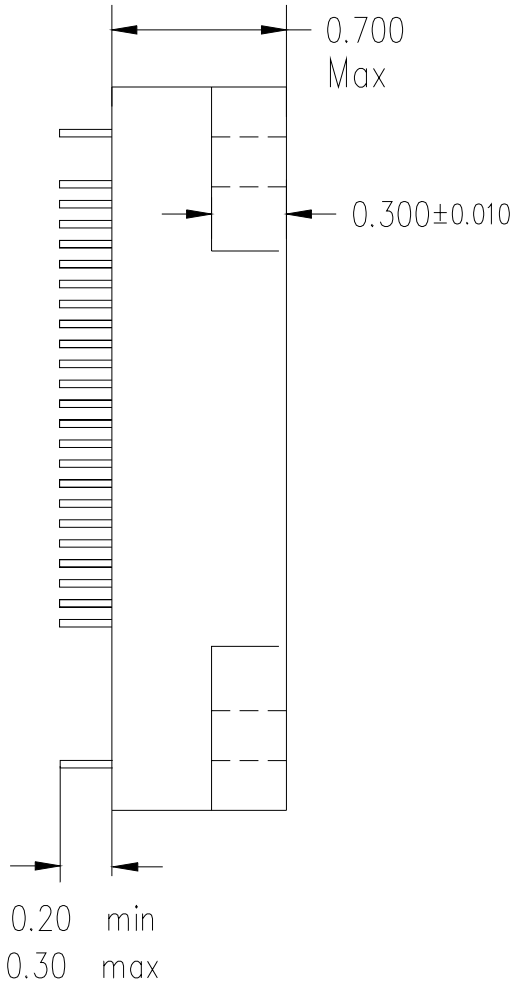
**Package Drawing Top View:**



**Package Drawing Side View:**



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**Application Notes:**

**a- Shutdown Feature:**

**1-** SD is a dual function input/output, active low input. It is internally pulled high. As a low input shuts down all IGBTs regardless of the Hin and Lin signals.
**2-** SD is also internally activated by the over-temperature shutdown, over-current limit, under-voltage shutdown, and desaturation protection.
**3-** Over-temperature shutdown, and over-current limit are not latching features.
**4-** Under-voltage shutdown is automatically reset after 300 msec once the VCC rises above the threshold limit.
**5-** Desaturation shutdown is a latching feature and internally reset after 300 msec.
**6-** When any of the internal protection features is activated, SD is pulled down.
**7-** SD can be used to shutdown all IGBTs except the brake IGBT by an external command. An open collector switch shall be used to pull down SD externally.
**8-** Also, SD can be used as a fault condition output. Low output at SD indicates a fault situation.

**b- Fault Output Feature:**

**1-** Pin 18 Flt is a dual function pin. It is internally pulled high. If pulled down, it will freeze the status of all the six IGBTs regardless of the Hin and Lin signals
**2-** Pin 18 as an output reports desaturation protection activation. When desaturation protection is activated a low output for about 9 μsec is reported.
**3-** If any other protection feature is activated, it will not be reported by Pin 18.

**c- Fault Clear Output:**

**1-** Pin 19 is a fault clear input. It can be used to reset a latching fault condition, due to desaturation protection.
**2-** Pin 19 is internally pulled down. A latching fault due to desaturation can be cleared by pulling high this input.
**3-** An internal fault clear is activated after 300 msec delay. If desired to clear the fault earlier, this input can be used.

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**Cleaning Process:**
Suggested precaution following cleaning procedure:
If the parts are to be cleaned in an aqueous based cleaning solution, it is recommended that the parts be baked immediately after cleaning. This is to remove any moisture that may have permeated into the device during the cleaning process. For aqueous based solutions, the recommended process is to bake for at least 2 hours at 125$^{o}$C.
Do not use solvents based cleaners.

**Recommended Soldering Procedure:**
Signal pins 1-24: 210C for 10 seconds max
Power pins 25 to 52: 260C for 10 seconds max. Pre-warm module to 125C to aid in power pins soldering.