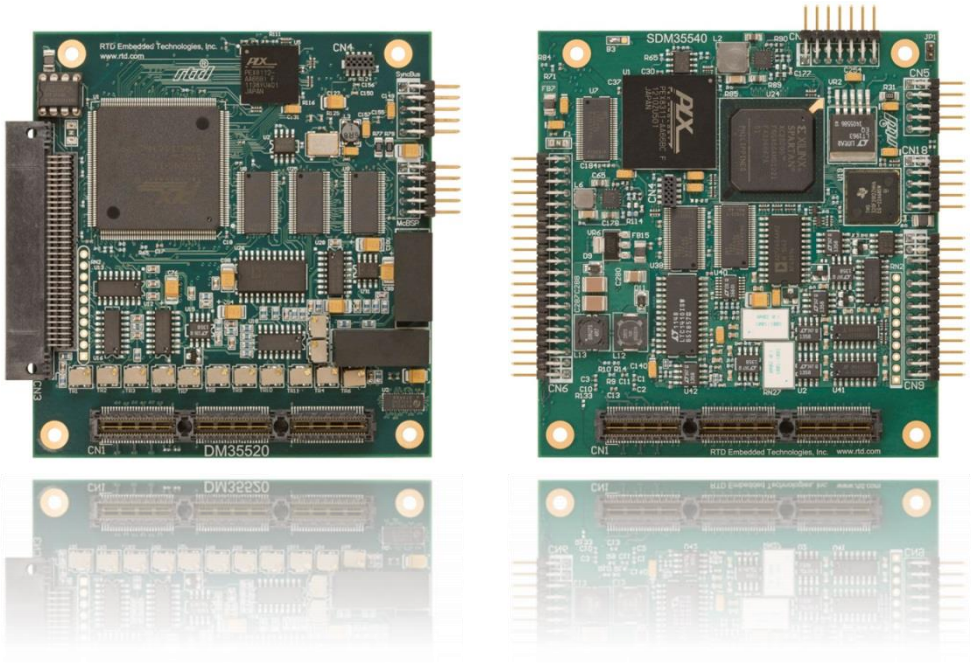
DM35520HR/SDM35540HR

12-Bit Analog I/O dataModule

User's Manual

BDM-610010042 Rev. D



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Revision History

Rev A	Initial Release
Rev B	Added Information for the SDM35540
Rev C	Added DM35520 picture to front cover
Rev D	Pin 1 of McBSP Pin-outs was changed to No Connect SDM35540 IDAN Pin-outs listed incorrect SDM35540 CN numbers. Added diagram of 68 pin connector.

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1 Introduction

1.1 Product Overview

The DM35520 is a software configurable high-speed, 12-bit data acquisition module in a PCIe/104 format. It provides 8 differential or 16 single-ended analog input channels, with programmable gain and input ranges. It also provides two individually controlled analog outputs, multiple board synchronization with the SyncBus and multi-channel buffered Serial Port, McBSP.

The SDM35540 has all the functionality of the DM35520, but also features auto calibration with the use of an onboard DSP and an onboard temperature sensor.

1.2 Board Features

- High-Speed Analog Inputs
  - 8 Differential or 16 Single-ended channels
  - 12-bit A/D with matched internal Sample and Hold
  - 0.8µs conversion time (1.25 MHz throughput)
  - ±5, ±10, 0 to +10 V Analog Input Ranges
  - Programmable binary gains of 1, 2, 4, 8, 16 & 32
  - 1K entry Channel-Gain Scan Memory with Skip Bit
- High-Speed Data Paths
  - Multi-channel Buffered Serial Port (McBSP)
  - 1K sample buffer on A/D converter
  - 1K sample buffer on each D/A converter channel
- Versatile Triggering
  - Software, Pace Clock, Burst Clock and External Triggers
  - Pre-, Post-, and About- Trigger Modes
  - Random Scan, burst and multi-burst using channel-gain table
- Two fast analog outputs
  - 12-bit resolution
  - 7 µs full-scale settling time (±10V range)
  - ±5, +5, ±10, & +10V output ranges
  - 5mA output current
- Digital I/O
  - 3 Data-marker Input Bits
  - 1K byte digital input buffer
  - 8 bit-programmable digital I/O lines and an 8-bit programmable port
  - Advanced digital interrupts
  - -12/+24mA output drive currents
- Timer and Counters
  - Twelve 16-bit, 8 MHz timer/counters to support timing and counting functions (3 available for user applications)
- Programmable Interrupt Source
- Auto calibration (SmartCal) for A/D and D/A with onboard DSP (SDM35540 only)
- On-board Temperature sensor (SDM35540 only)
- PCI Express Bus:
  - Provides 2.5 Gbps in each direction
  - Single lane and single Virtual Channel operation
    - Compatible with multi-Virtual Channel chipsets
  - Packetized serial traffic with PCI Express Split Completion protocol
  - Data Link Layer Cyclic Redundancy Check (CRC) generator and checker
  - Automatic Retry of bad packets
  - In-band interrupts and messages
  - Message Signaled Interrupt (MSI) support

1.3 Ordering Information

The DM35520 is available with the following options:

Table 1: Ordering Options

Part Number	Description
DM35520HR	*PCIe/104 12-bit Analog I/O dataModule*
SDM35540HR	*PCIe/104 12-bit Analog I/O Smart dataModule*
IDAN-DM35520HR	PCIe/104 12-bit Analog I/O dataModule in IDAN enclosure
IDAN-SDM35540HR	PCIe/104 12-bit Analog I/O *Smart* dataModule in IDAN enclosure

Note: Throughout this document, DM35520 refers to both the DM35520 and SDM35540 unless otherwise noted

The Intelligent Data Acquisition Node (IDAN™) building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged 104™ stack. This module can also be incorporated in a custom-built RTD HiDAN™ or HiDANplus High Reliability Intelligent Data Acquisition Node. Contact RTD sales for more information on our high reliability systems.

1.4 Contact Information

1.4.1 Sales Support

For sales inquiries, you can contact RTD Embedded Technologies sales via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: sales@rtd.com

1.4.2 Technical Support

If you are having problems with you system, please try the steps in the Troubleshooting section of this manual.

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies technical support via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: techsupport@rtd.com

2 Specifications

2.1 Operating Conditions

Table 2: Operating Conditions

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{cc5}	5V Supply Voltage		4.75	5.25	V
V_{cc3}	3.3V Supply Voltage		n/a	n/a	V
V_{cc12}	12V Supply Voltage		n/a	n/a	V
V_{cc-12}	-12V Supply Voltage		n/a	n/a	V
T_a	Operating Temperature		-40	+85	C
T_s	Storage Temperature		-55	+125	C
RH	Relative Humidity	Non-Condensing	0	90%	%
MTBF	Mean Time Before Failure	Telcordia Issue 2 30°C, Ground benign, controlled		TBD	Hours

2.2 Electrical Characteristics

Table 3: Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
P	Power Consumption	V_{cc5} = 5.0V		TBD	W
I_{cc5}	5V Input Supply Current	Active		TBD	mA
		PCIe Bus			
	Differential Output Voltage		0.8	1.2	V
	DC Differential TX Impedance		95.2	116.9	Ω
	Differential Input Voltage		0.175	3.3	V
	DC Differential RX Impedance		92.7	115.8	Ω
	Electrical Idle Detect Threshold		61	173	mV
		A/D Circuitry			
	Input Impedance			>10	MΩ
	Gains		1	128	
	Gain Error			0.1%	
	Input Voltage	20V Range Mode		±10	V
		10V Range Mode		±5	V
		Unipolar Mode	0	10	V
	Over Voltage Protection			±15	V
	Common Mode			±10	V
	Channel Scanning Error (Gain=1)	10…500khz		0%	
		600kHz		0.05%	
		700kHz		0.075%	
		800kHz		0.25%	
		900kHz		0.4%	
		1000kHz		0.45%	
		1250kHz		1%	
	Resolution			12	Bits
	Linearity Error			±1	LSB
	Sampling Rate			1.25	MHz
	FIFO Size X16			1	Kb
	Channel Gain table X24			1	Kb
		Digital I/O			
	Output Current			±8	mA
	Input Termination			10	KΩ
	Output Termination			10	Ω
		D/A Circuitry			
	Resolution			12	Bits
	Relative Accuracy			±1	LSB
	Full-Scale Accuracy			±5	LSB
	Non-lineaity			±1	LSB

Table 3: Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
	Settling Time			5	µs
	Output Current			5	mA
	FIFO Size X16	Per channel		8	Kb

3 Board Connection

3.1 Board Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your board in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

3.2 Physical Characteristics

- Weight: Approximately 55 g (0.12 lbs.)
- Dimensions: 90.17 mm L x 95.89 mm W (3.550 in L x 3.775 in W)

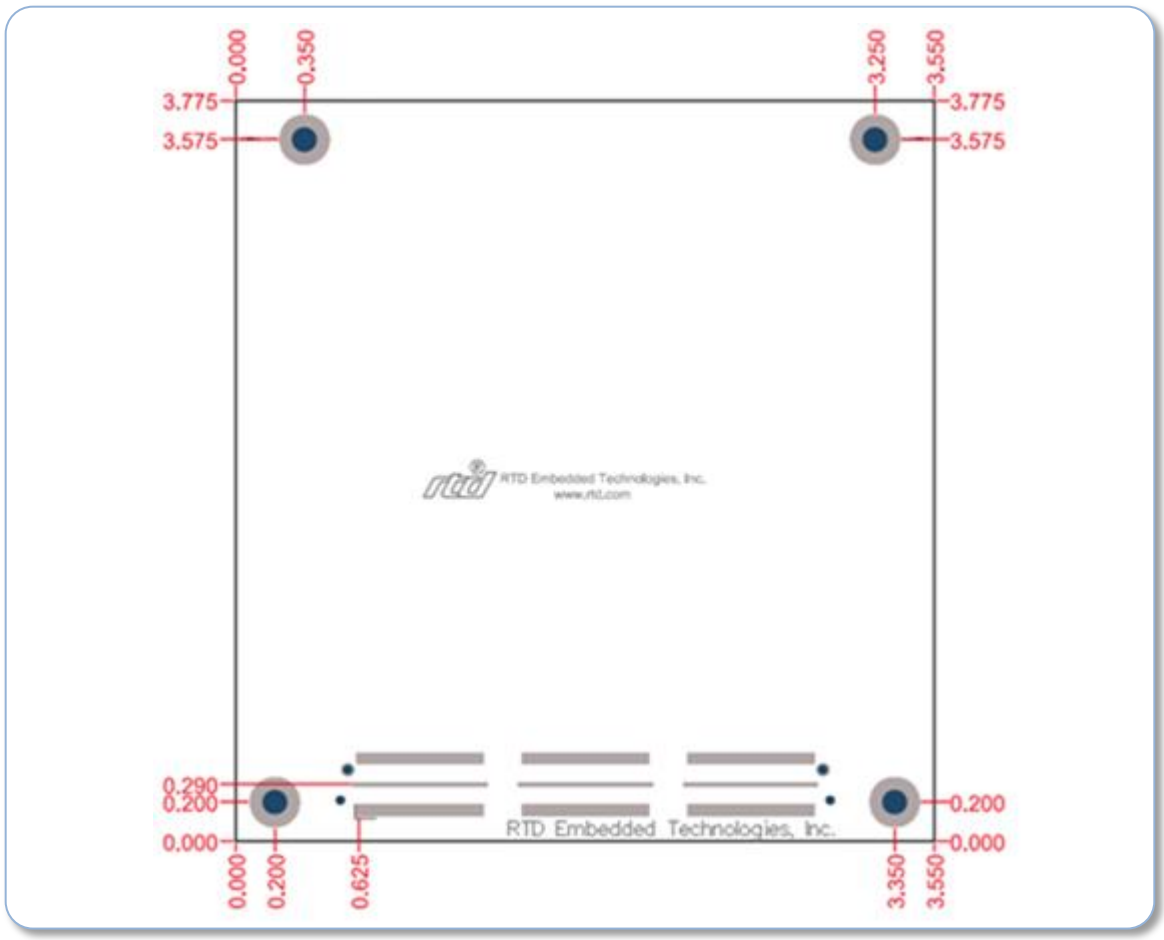


Figure 1: Board Dimensions

3.3 DM35520 Connectors and Jumpers

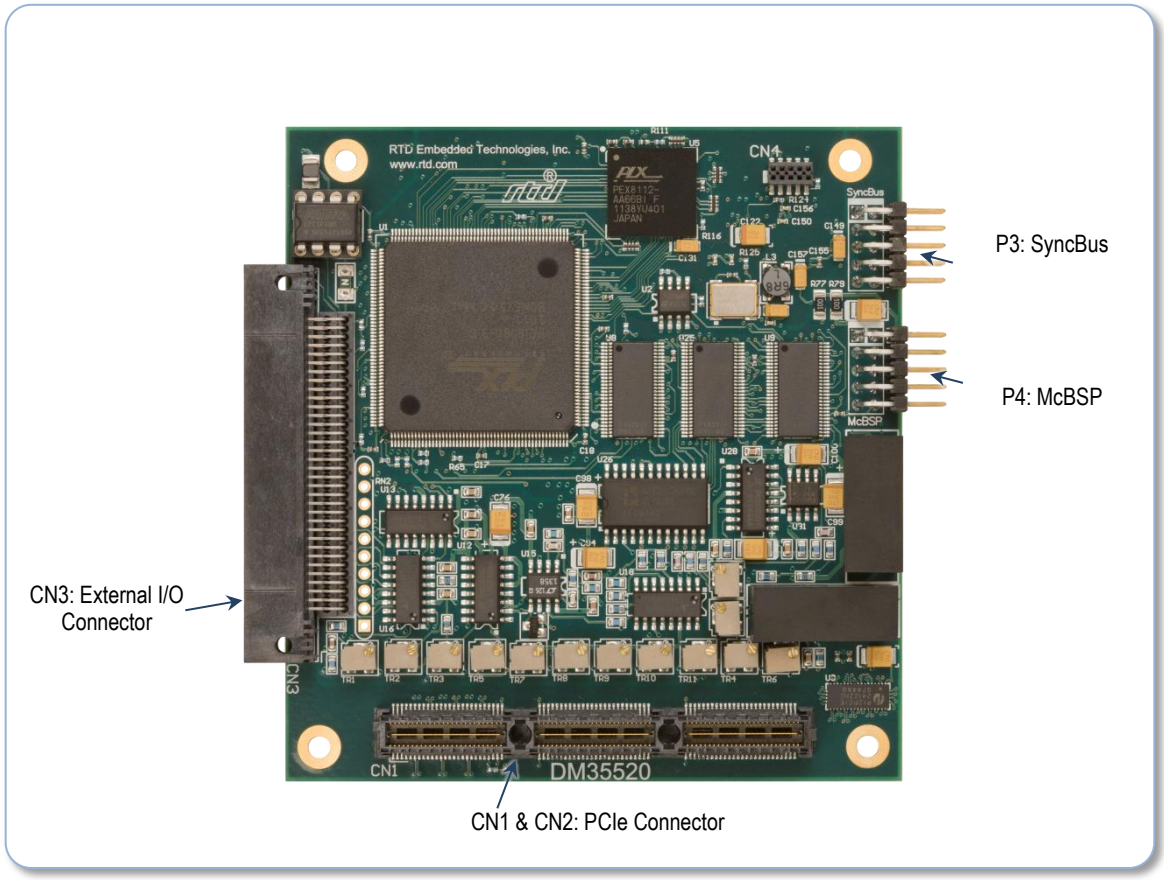


Figure 2: DM35520 Board Connections

3.3.1 External I/O Connectors

Table 4: Signal Functions

Signal	Function
AINx / AINx +/AINx -	SE Analog input high sides / DIFF analog input high sides / DIFF analog inputs low sides.
AINSENSE	Reference Signal in Non-ground referenced Single Ended (NRSE) input mode.
AOUT x	Analog outputs.
AGND	Analog Ground
D/A 1 Data Marker 0	D/A 1 0 the output data markers.
D/A 2 Data Marker 0	D/A 2 0 the output data markers.
High Speed Input x / P0.x / A/D DMx	High speed inputs to digital input FIFO / Bit programmable P0 lines from digital I/O Chip.
P1.x / DIG Table x	Port programmable lines from digital I/O Chip. Outputs from digital part of channel gain table.
Trigger Input	External trigger input to trigger A/D pacer clock. (LS TTL)
External Pace Clock Input	External pacer clock to clock A/D. (LS TTL)
Reset	Active low reset output line asserted when the host PC is in hardware reset, or the Board Clear Command is active. (LS TTL)
External Interrupt Input	Programmable rising or falling edge external Interrupt source. (LS TTL)
User Input x	User Input 0 and User Input 1 can be read by the LAS0+04h I/O read instruction. . (LS TTL)

Signal	Function
User Output x	The source of these buffered lines can be programmed. (LS TTL)
External TC Gate x	External gate signals that go to the software programmable clock source select circuit for the user timer/counters. (LS TTL)
TC Out x	Buffered outputs from the user timer/counters. (LS TTL)
External TC Clock x	External clock signals that go to the software programmable clock source select circuit for the user timer/counters. (LS TTL)
DGND	Digital Signal Ground
+5V	+5 Volts from the computer power supply to power front end boards. (Max. 2A)

CN3: External I/O Connector

CN3 is an external connector for the majority of I/O connections on the board. The connector contains signals for the analog I/O, digital I/O, data triggers, and timer/counter. The pin assignment is listed below.

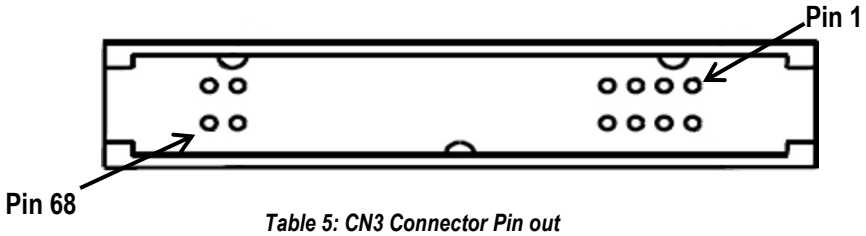


Table 5: CN3 Connector Pin out

AIN 9 / AIN1-	2	1	AIN 1 / AIN1+
AIN 10 / AIN2-	4	3	AIN 2 / AIN2+
AIN 11 / AIN3-	6	5	AIN 3 / AIN3+
AIN 12 / AIN4-	8	7	AIN 4 / AIN4+
AGND	10	9	AINSENSE
AIN 13 / AIN5-	12	11	AIN 5 / AIN5+
AIN 14 / AIN6-	14	13	AIN 6 / AIN6+
AIN 15 / AIN7-	16	15	AIN 7 / AIN7+
AIN 16 / AIN8-	18	17	AIN 8 / AIN8+
AGND	20	19	AGND
Reserved	22	21	AOUT 1
Reserved	24	23	AOUT 2
AGND	26	25	Reserved
AGND	28	27	AGND
D/A 2 DATA MARKER 0	30	29	D/A 1 DATA MARKER 0
P1.7 / DIG TABLE 7	32	31	HIGH SPEED INPUT 7 / P0.7 / A/D DM2
P1.6 / DIG TABLE 6	34	33	HIGH SPEED INPUT 6 / P0.6 / A/D DM1
P1.5 / DIG TABLE 5	36	35	HIGH SPEED INPUT 5 / P0.5 / A/D DM0
P1.4 / DIG TABLE 4	38	37	HIGH SPEED INPUT 4 / P0.4
P1.3 / DIG TABLE 3	40	39	HIGH SPEED INPUT 3 / P0.3
P1.2 / DIG TABLE 2	42	41	HIGH SPEED INPUT 2 / P0.2
P1.1 / DIG TABLE 1	44	43	HIGH SPEED INPUT 1 / P0.1
P1.0 / DIG TABLE 0	46	45	HIGH SPEED INPUT 0 / P0.0
DGND	48	47	TRIGGER INPUT
RESET	50	49	EXTERNAL PACER CLOCK INPUT
DGND	52	51	EXTERNAL INTERRUPT INPUT
USER INPUT 1	54	53	USER INPUT 0
USER OUTPUT 1	56	55	USER OUTPUT 0
DGND	58	57	TC OUT 0
EXTERNAL TC GATE 1	60	59	EXTERNAL TC CLOCK 1
TC OUT 2	62	61	TC OUT 1
EXTERNAL TC GATE 2	64	63	EXTERNAL TC CLOCK 2
DGND	66	65	+5 VOLTS
DGND	68	67	+5 VOLTS

P3: SyncBus

The SyncBus is an RTD defined digital bus for synchronous operation with other RTD's boards. The signaling level is 5V compliant TTL. There are no pull-up resistors on the bus lines. If a line is used, a master/driver for this lane needs to exist somewhere in the system.

Table 6: P3: SyncBus Pin out

SyncBus0	1	2	GND
GND	3	4	GND
SyncBus1	5	6	GND
GND	7	8	GND
SyncBus2	9	10	GND

P4: McBSP

The McBSP (Multichannel Buffered Serial) is a Texas Instruments defined serial bus for DSP and front-end communication. This port is 5V compliant.

These lines must be connected directly to the appropriate DSP Signals. This means, that the DAQ board drives the DR and FRS signals, and receives the DX, FSX, and CLKX and CLKR signals. The CLKS signal is defined only for TI connector compliance and is not physically connected on the DAQ board. This connection needs a straight 10-pin cable.

Table 7: P4: McBSP Pin out

NC	1	2	GND
CLKR	3	4	FSR
CLKX	5	6	GND
DR	7	8	FSX
DX	9	10	GND

3.3.2 Bus Connectors

CN1(Top) & CN2(Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 98)

The DM35520 is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

3.3.3 Jumpers

There are no jumpers on the DM35520

3.4 SDM35540 Connectors and Jumpers

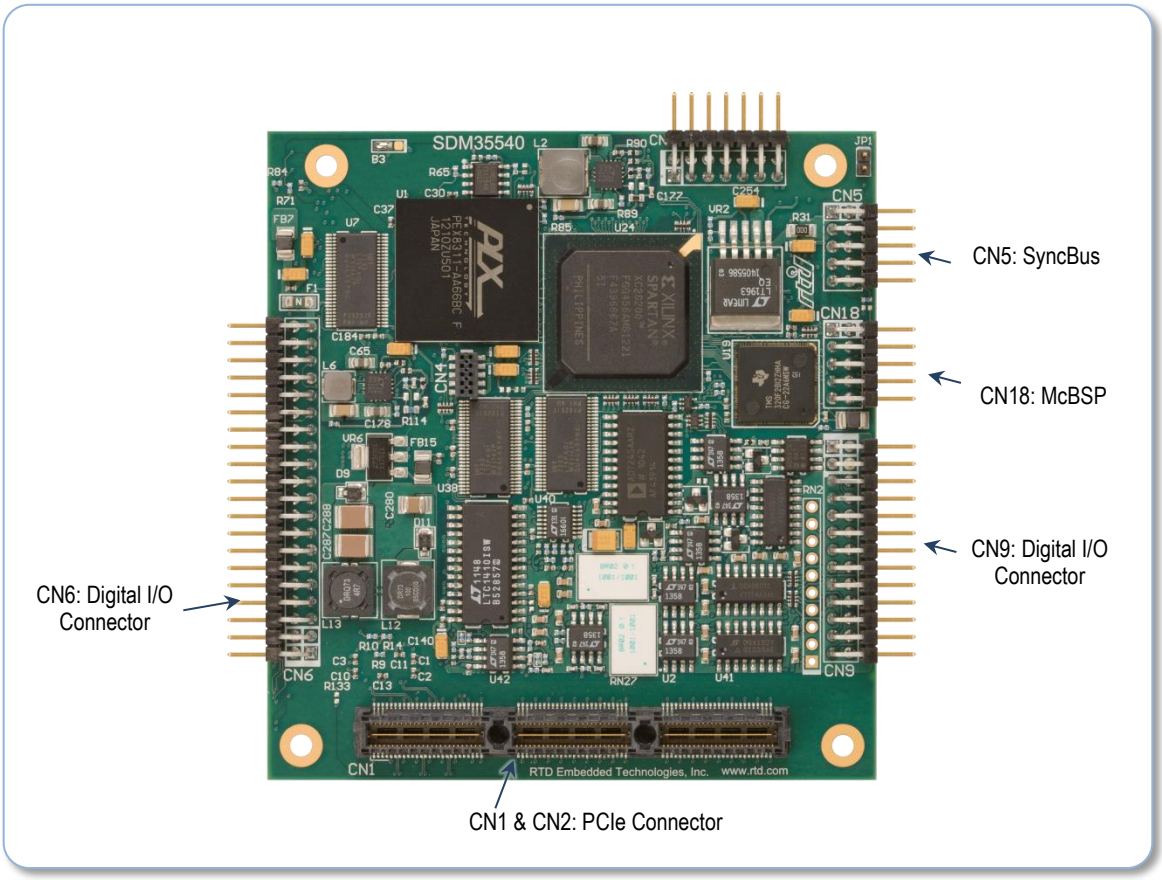


Figure 3: SDM35540 Board Connections

3.4.1 External I/O Connectors

Table 8: Signal Functions

Signal	Function
AINx / AINx +/AINx -	SE Analog input high sides / DIFF analog input high sides / DIFF analog inputs low sides.
AINSENSE	Reference Signal in Non-ground referenced Single Ended (NRSE) input mode.
AOUT x	Analog outputs.
AGND	Analog Ground
D/A 1 Data Marker 0	D/A 1 0 the output data markers.
D/A 2 Data Marker 0	D/A 2 0 the output data markers.
High Speed Input x / P0.x / A/D DMx	High speed inputs to digital input FIFO / Bit programmable P0 lines from digital I/O Chip.
P1.x / DIG Table x	Port programmable lines from digital I/O Chip. Outputs from digital part of channel gain table.
Trigger Input	External trigger input to trigger A/D pacer clock. (LS TTL)
External Pace Clock Input	External pacer clock to clock A/D. (LS TTL)
Reset	Active low reset output line asserted when the host PC is in hardware reset, or the Board Clear Command is active. (LS TTL)
External Interrupt Input	Programmable rising or falling edge external Interrupt source. (LS TTL)
User Input x	User Input 0 and User Input 1 can be read by the LAS0+04h I/O read instruction. . (LS TTL)

Signal	Function
User Output x	The source of these buffered lines can be programmed. (LS TTL)
External TC Gate x	External gate signals that go to the software programmable clock source select circuit for the user timer/counters. (LS TTL)
TC Out x	Buffered outputs from the user timer/counters. (LS TTL)
External TC Clock x	External clock signals that go to the software programmable clock source select circuit for the user timer/counters. (LS TTL)
DGND	Digital Signal Ground
+5V	+5 Volts from the computer power supply to power front end boards. (Max. 2A)

CN6: External Digital I/O Connector

CN6 is an external connector for the majority of Digital I/O connections on the board. The connector contains signals for the digital I/O, data triggers, and timer/counter. The pin assignment is listed below.

Table 9: Digital I/O Connector

P1.7 / DIG TABLE 7	2	1	HIGH SPEED INPUT 7 / P0.7 / A/D DM2
P1.6 / DIG TABLE 6	4	3	HIGH SPEED INPUT 6 / P0.6 / A/D DM1
P1.5 / DIG TABLE 5	6	5	HIGH SPEED INPUT 5 / P0.5 / A/D DM0
P1.4 / DIG TABLE 4	8	7	HIGH SPEED INPUT 4 / P0.4
P1.3 / DIG TABLE 3	10	9	HIGH SPEED INPUT 3 / P0.3
P1.2 / DIG TABLE 2	12	11	HIGH SPEED INPUT 2 / P0.2
P1.1 / DIG TABLE 1	14	13	HIGH SPEED INPUT 1 / P0.1
P1.0 / DIG TABLE 0	16	15	HIGH SPEED INPUT 0 / P0.0
Reserved	18	17	Reserved
D/A 2 DATA MARKER 0	20	19	D/A 1 DATA MARKER 0
DGND	22	21	TRIGGER INPUT
Reserved	24	23	EXTERNAL PACER CLOCK INPUT
DGND	26	25	EXTERNAL INTERRUPT INPUT
USER INPUT 1	28	27	USER INPUT 0
USER OUTPUT 1	30	29	USER OUTPUT 0
DGND	32	31	TC OUT 0
EXTERNAL TC GATE 1	34	33	EXTERNAL TC CLOCK 1
TC OUT 2	36	35	TC OUT 1
EXTERNAL TC GATE 2	38	37	EXTERNAL TC CLOCK 2
DGND	40	39	+5 VOLTS

CN9: External Analog I/O Connector

CN9 is an external connector for the analog I/O connections on the board. The pin assignment is listed below.

Table 10: Analog I/O Connector

Digital I/O 1	2	1	Digital I/O 0
AGND	4	3	+5 VOLTS
AOUT 2	6	5	AGND
AOUT 1	8	7	AGND
AIN 8 / AIN8+	10	9	AIN 16 / AIN8-
AIN 7 / AIN7+	12	11	AIN 15 / AIN7-
AIN 6 / AIN6+	14	13	AIN 14 / AIN6-
AIN 5 / AIN5+	16	15	AIN 13 / AIN5-
AINSENSE	18	17	AGND
AIN 4 / AIN4+	20	19	AIN 12 / AIN4-
AIN 3 / AIN3+	22	21	AIN 11 / AIN3-
AIN 2 / AIN2+	24	23	AIN 10 / AIN2-
AIN 1 / AIN1+	26	25	AIN 9 / AIN1-

CN5: SyncBus

The SyncBus is an RTD defined digital bus for synchronous operation with other RTD's boards. The signaling level is 5V compliant TTL. There are no pull-up resistors on the bus lines. If a line is used, a master/driver for this lane needs to exist somewhere in the system.

Table 11: SyncBus

SyncBus0	1	2	GND
GND	3	4	GND
SyncBus1	5	6	GND
GND	7	8	GND
SyncBus2	9	10	GND

CN18: McBSP

The McBSP (Multichannel Buffered Serial) is a Texas Instruments defined serial bus for DSP and front-end communication. This port is 5V compliant.

These lines must be connected directly to the appropriate DSP Signals. This means, that the DAQ board drives the DR and FRS signals, and receives the DX, FSX, and CLKX and CLKR signals. The CLKS signal is defined only for TI connector compliance and is not physically connected on the DAQ board. This connection needs a straight 10-pin cable.

Table 12: McBSP

NC	1	2	GND
CLKR	3	4	FSR
CLKX	5	6	GND
DR	7	8	FSX
DX	9	10	GND

NOTE: CN14 and CN21 are for Factory use only

3.4.1 Bus Connectors

CN1(Top) & CN2(Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 98)

The SDM35540 is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

3.4.2 Jumpers

JP1: Local Reset

Installing JP1 causes the local bus to reset. This jumper is not installed for normal operations.

3.5 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the PC/104 system or stack.
3. Select and install stand-offs to properly position the module on the stack.
4. Remove the module from its anti-static bag.
5. Check that pins of the bus connector are properly positioned.
6. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
7. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the module onto the PC/104 stack.
9. If any boards are to be stacked above this module, install them.
10. Attach any necessary cables to the PC/104 stack.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

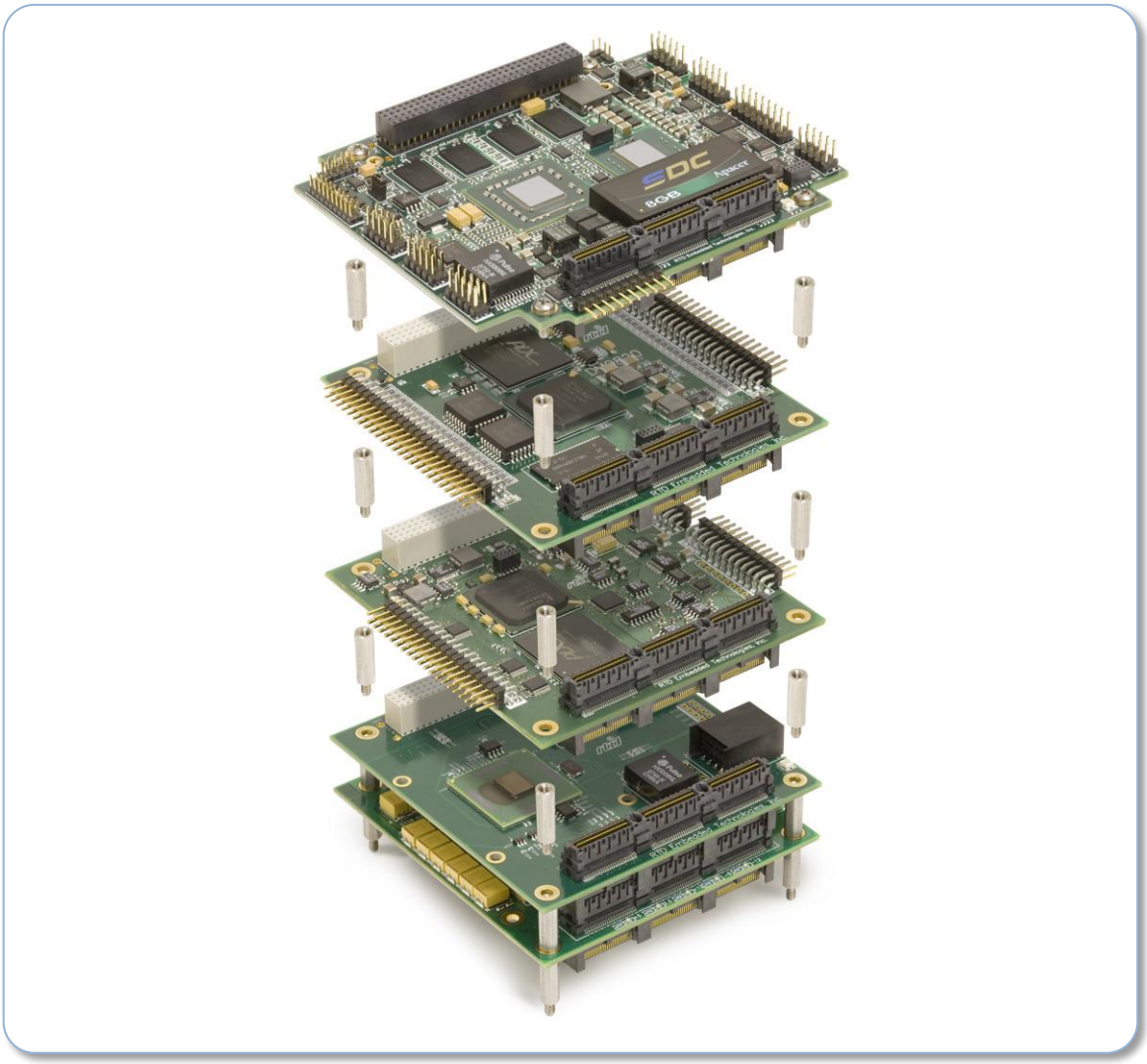


Figure 4: Example 104™ Stack

4 IDAN Connections

4.1 Module Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your module in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the module by the aluminum enclosure, and do not touch the components or connectors. Handle the module in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

4.2 Physical Characteristics

- Weight: Approximately 0.21 Kg (0.46 lbs.)
- Dimensions: 151.972 mm L x 129.978 mm W x 16.993 mm H (5.983 in L x 5.117 in W x 0.669 in H)

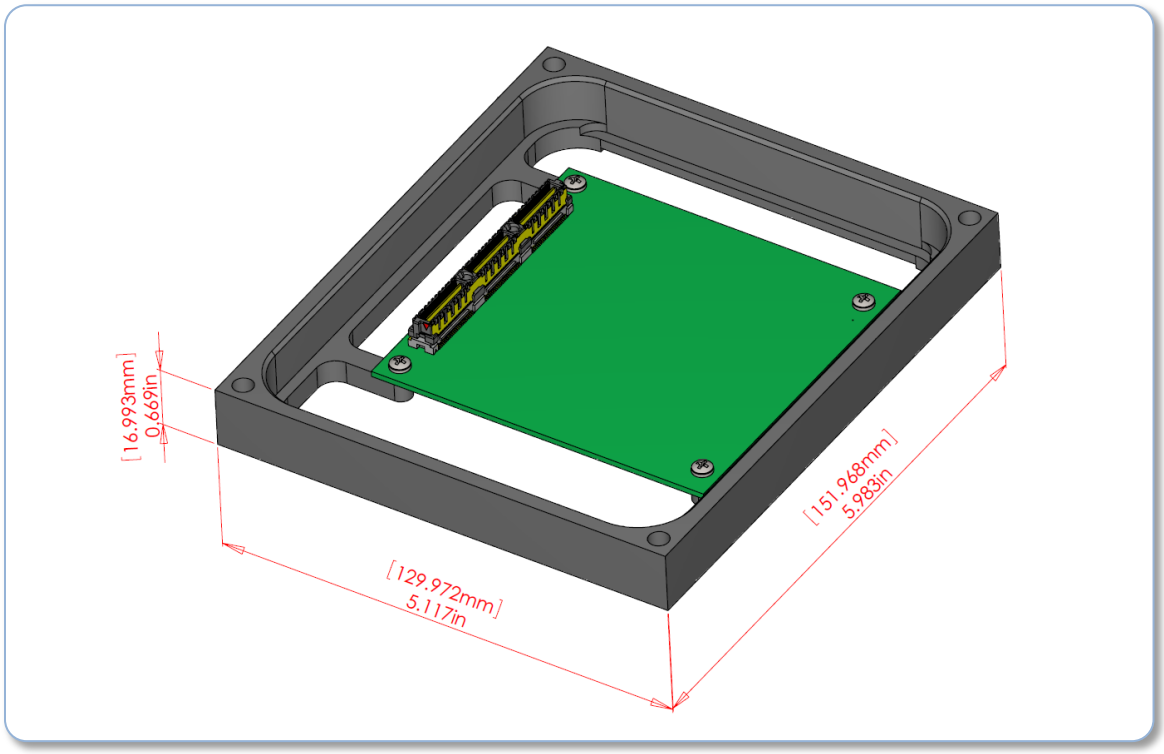
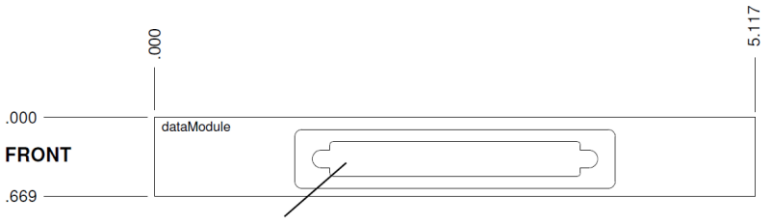


Figure 5: IDAN Dimensions

4.3 DM35520 Connectors

4.3.1 External I/O Connectors



68 pin Subminiature "D": Female
Module Part#: Amp 749070-7
Mating Part#: Amp 786090-7(IDC Crimp)

Note: Drawing is not to scale.

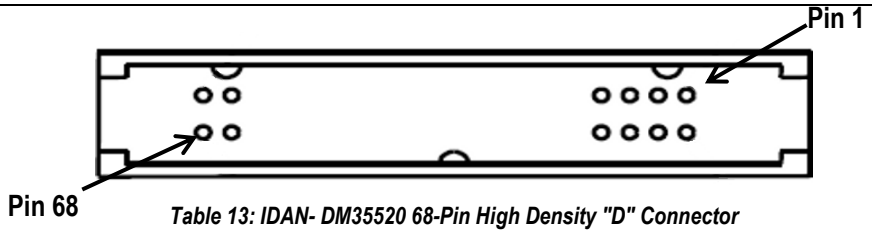


Table 13: IDAN- DM35520 68-Pin High Density "D" Connector

IDAN Pin#	Signal	DM35520 CN3 Pin #
1	AIN1+/AIN1	1
2	AIN1-/AIN9	2
3	AIN2+/AIN2	3
4	AIN2-/AIN10	4
5	AIN3+/AIN3	5
6	AIN3-/AIN11	6
7	AIN4+/AIN4	7
8	AIN4-/AIN12	8
9	Analog In sense	9
10	Analog Ground	10
11	AIN5+/AIN5	11
12	AIN5-/AIN13	12
13	AIN6+/AIN6	13
14	AIN6-/AIN114	14
15	AIN7+/AIN7	15
16	AIN7-/AIN115	16
17	AIN8+/AIN8	17
18	AIN8-/AIN16	18
19	Analog Ground	19
20	Analog Ground	20
21	AOUT 1	21
22	RESERVED	22
23	AOUT 2	23
24	RESERVED	24
25	RESERVED	25
26	Analog Ground	26
27	Analog Ground	27
28	Analog Ground	28

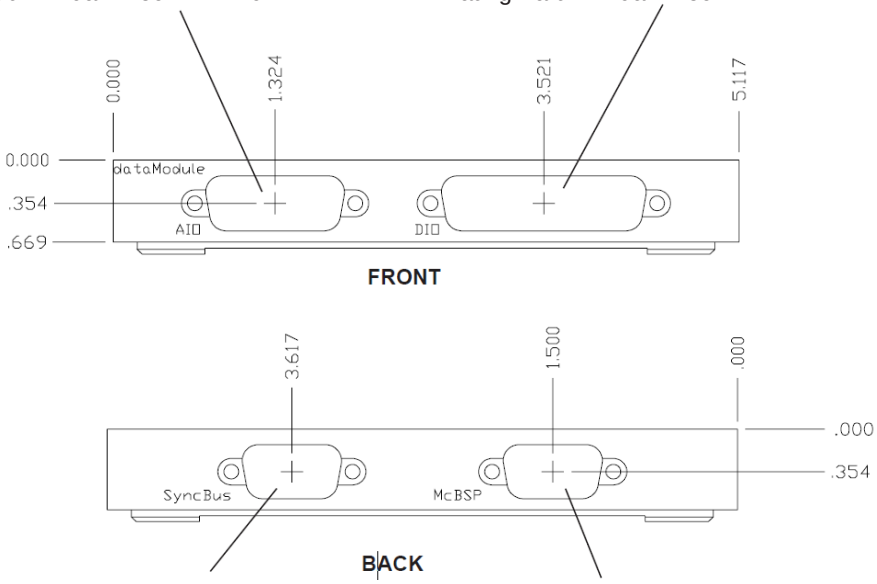
IDAN Pin#	Signal	DM35520 CN3 Pin #
29	D/A 1 Data Marker 0	29
30	D/A 2 Data Marker 0	30
31	P0.7 / High Speed Digital Input 7	31
32	P1.7 / Digital Table Output 7	32
33	P0.6 / High Speed Digital Input 6	33
34	P1.6 / Digital Table Output 6	34
35	P0.5 / High Speed Digital Input 5	35
36	P1.5 / Digital Table Output 5	36
37	P0.4 / High Speed Digital Input 4	37
38	P1.4 / Digital Table Output 4	38
39	P0.3 / High Speed Digital Input 3	39
40	P1.3 / Digital Table Output 3	40
41	P0.2 / High Speed Digital Input 2	41
42	P1.2 / Digital Table Output 2	42
43	P0.1 / High Speed Digital Input 1	43
44	P1.1 / Digital Table Output 1	44
45	P0.0 / High Speed Digital Input 0	45
46	P1.0 / Digital Table Output 0	46
47	External Trigger Input	47
48	Digital Ground	48
49	External Pacer Clock Input	49
50	Reset	50
51	External Interrupt Input	51
52	Digital Ground	52
53	User Input 0	53
54	User Input 1	54
55	User Output 0	55
56	User Output 1	56
57	Timer/Counter 0 Output	57
58	Digital Ground	58
59	Timer/Counter External Clock 1	59
60	Timer/Counter External Gate 1	60
61	Timer/Counter 1 Output	61
62	Timer/Counter 2 Output	62
63	Timer/Counter External Clock 2	63
64	Timer/Counter External Gate 2	64
65	+5 VOLTS	65
66	Digital Ground	66
67	+5 VOLTS	67
68	Digital Ground	68

4.4 SDM35540 Connectors

4.4.1 External I/O Connectors

26 pin "High Density D": female
Module Part #: Adam Tech HDT26SD
Mating Part #: Adam Tech HDT26PD

44 pin "High Density D": female
Module Part #: Adam Tech HDT44ST
Mating Part #: Adam Tech HDT44PD



9 pin "D": female
Module Part #: AMP/TYCO 1658610-4
Mating Part #: AMP/TYCO 1658608-4

9 pin "D": male
Module Part #: VALCON DF-9P
Mating Part #: VALCON DF-9S

Note: Drawing is not to scale.

Table 14: IDAN-SDM35540 Analog I/0 26-pin "D" Connector

IDAN Pin#	Signal	SDM35540 CN9 Pin #
1	Digital I/O 0	1
2	Digital I/O 1	2
3	+5 VOLTS	3
4	AGND	4
5	AGND	5
6	AOUT 2	6
7	AGND	7
8	AOUT 1	8
9	AIN 16 / AIN8-	9
10	AIN 8 / AIN8+	10
11	AIN 15 / AIN7-	11
12	AIN 7 / AIN7+	12
13	AIN 14 / AIN6-	13
14	AIN 6 / AIN6+	14
15	AIN 13 / AIN5-	15
16	AIN 5 / AIN5+	16
17	AGND	17
18	AINSENSE	18

IDAN Pin#	Signal	SDM35540 CN9 Pin #
19	AIN 12 / AIN4-	19
20	AIN 4 / AIN4+	20
21	AIN 11 / AIN3-	21
22	AIN 3 / AIN3+	22
23	AIN 10 / AIN2-	23
24	AIN 2 / AIN2+	24
25	AIN 9 / AIN1-	25
26	AIN 1 / AIN1+	26

Table 15: IDAN-SDM35540 Digital I/0 44-pin "D" Connector

IDAN Pin#	Signal	SDM35540 CN6 Pin #
1	DGND	40
2	External TC Clock 2	37
3	External TC Gate 1	34
4	TC Out 0	31
5	User Input 1	28
6	External Interrupt Input	25
7	DGND	22
8	D/A 1 Data Marker 0	19
9	P1.0/DIG Table 0	16
10	High Speed Input 1/P0.1	13
11	P1.6/ DIG Table 6	10
12	High Speed Input 4/P0.4	7
13	P1.6/ DIG Table 6	4
14	High Speed Input 7/P0.7/A/D DM2	1
15	Reserved	-
16	+5V	39
17	TC Out 2	36
18	External TC Clock 1	33
19	User Output 1	30
20	User Input 0	27
21	Reserved	24
22	External Trigger Input	21
23	Reserved	18
24	High Speed Input 0/P0.0	15
25	P1.2/DIG Table 2	12
26	High Speed Input 3/P0.3	9
27	P1.5/DIG Table 5	6
28	High Speed Input 6/P0.6/A/D DM1	3
29	Reserved	-
30	Reserved	-
31	External TC Gate 2	38
32	TC Out 1	35
33	DGND	32
34	User Output 0	29
35	DGND	26

IDAN Pin#	Signal	SDM35540 CN6 Pin #
36	External Pacer Clock Input	23
37	D/A 2 Data Maker 0	20
38	Reserved	17
39	P1.1/DIG Table 1	14
40	High Speed Input 2/P0.2	11
41	P1.4/DIG Table 4	8
42	High Speed Input 5/P0.5/A/D DM0	5
43	P1.7/DIG Table 7	2
44	Reserved	-

Table 16: IDAN-SDM35540 SyncBus 9-pin "D" Connector

IDAN Pin#	Signal	SDM35540 CN5 Pin #
1	SyncBus0	1
2	GND	3
3	SyncBus1	5
4	GND	7
5	SyncBus2	9
6	GND	2
7	GND	4
8	GND	6
9	GND	8

Table 17: IDAN-SDM35540 McBSP 9-pin "D" Connector

IDAN Pin#	Signal	SDM35540 CN18 Pin #
1	NC	1
2	CLKR	3
3	CLKX	5
4	DR	7
5	DX	9
6	GND	2
7	FSR	4
8	GND	6
9	FSX	8

4.5 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the IDAN system.
3. Remove the module from its anti-static bag.
4. Check that pins of the bus connector are properly positioned.
5. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
6. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
7. Gently and evenly press the module onto the IDAN system.
8. If any boards are to be stacked above this module, install them.
9. Finish assembling the IDAN stack by installing screws of an appropriate length.
10. Attach any necessary cables to the IDAN system.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

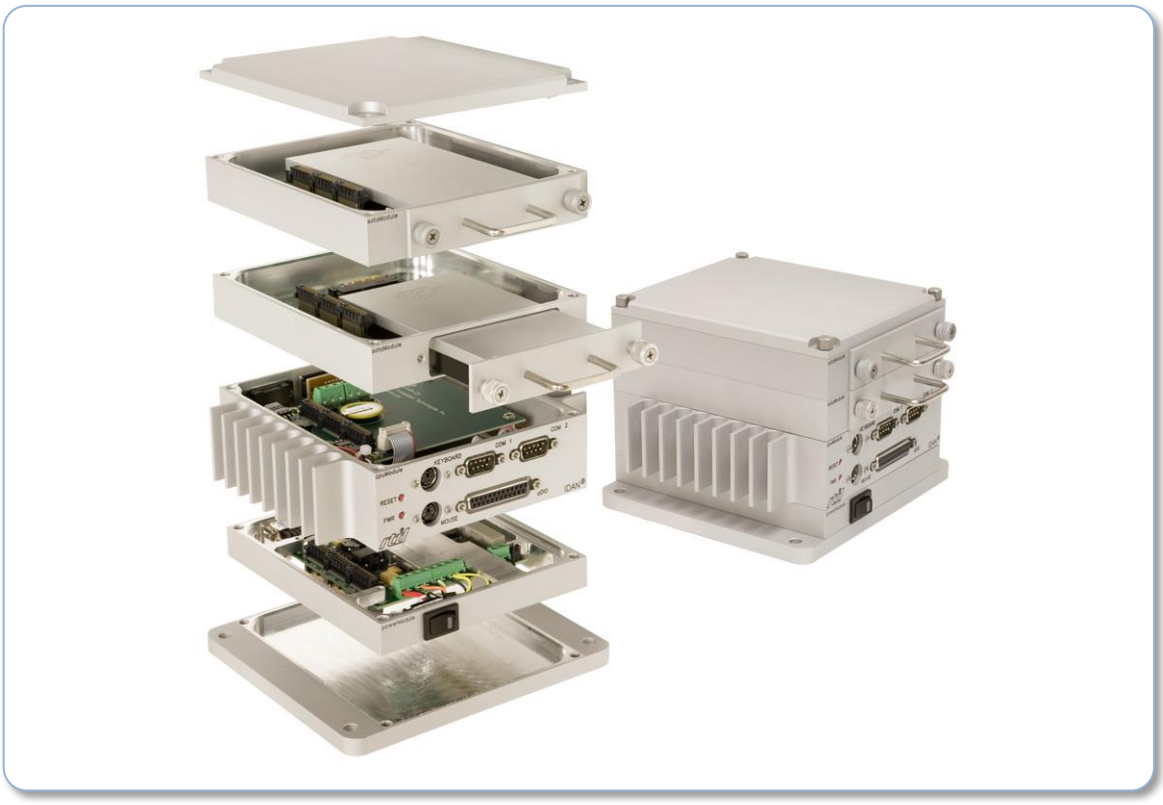


Figure 6: Example IDAN System

5 Functional Description

5.1 Block Diagram

The Figure below shows the functional block diagram of the DM35520. The various parts of the block diagram are discussed in the following sections.

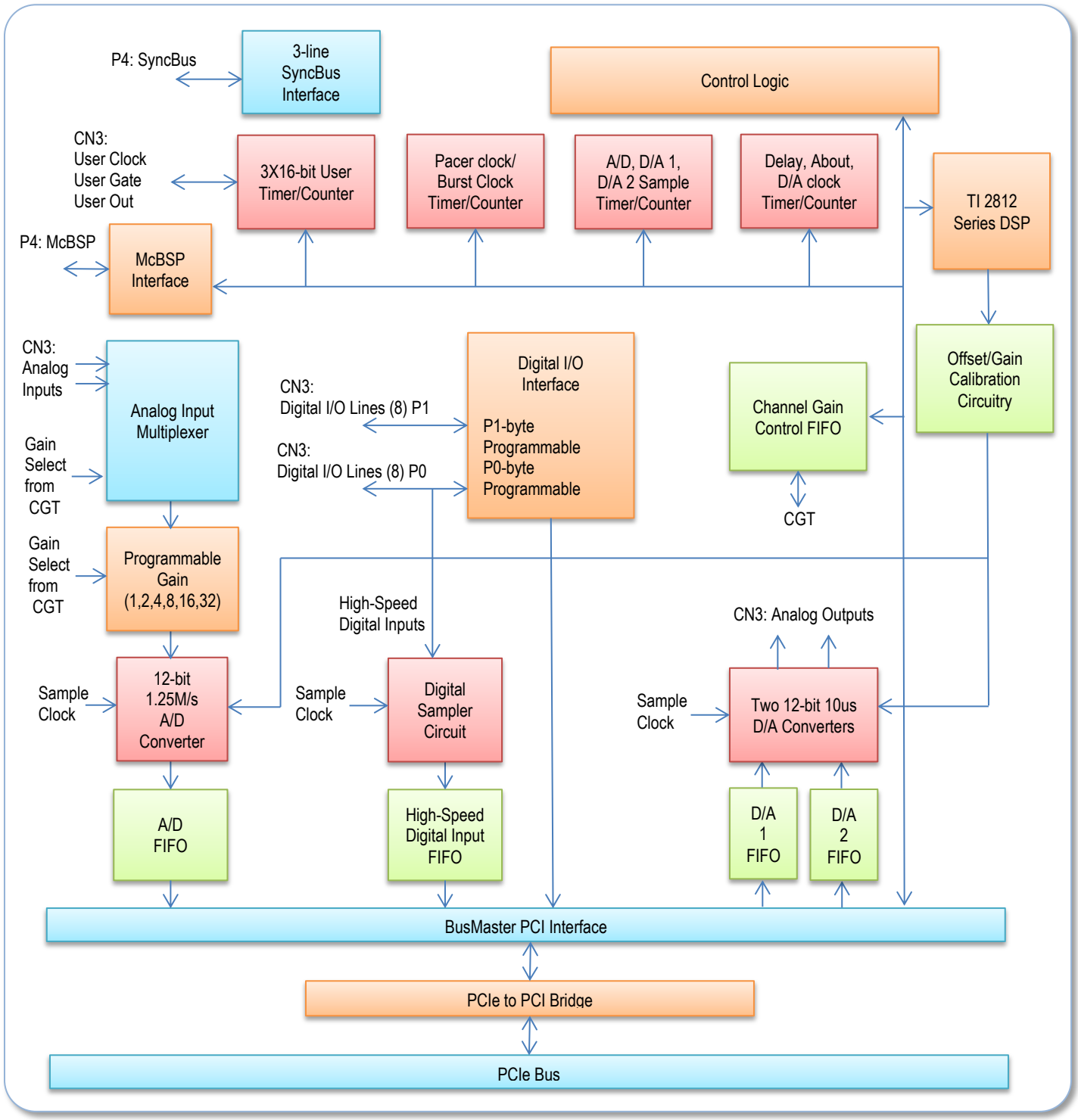


Figure 7: DM35520 Block Diagram

5.2 Hardware Description

5.2.1 Channel Gain Latch (CGL) and Channel Gain Table (CGT)

In the case of single-channel operation the Channel Gain Latch mode must be set by appropriate software instruction. Then the Channel Gain Latch must be loaded. This mode assures the highest sampling rate at the highest accuracy. This mode can be used for *analog trigger* function. You can use one of the input channels as *Analog Trigger Input.* Set the Channel input type, the number and gain according to the signal source from software. Reading the converted data from the input channel the analog trigger event can be detected. When the trigger event has been detected, the multi-channel -Channel Gain Table mode can be started.

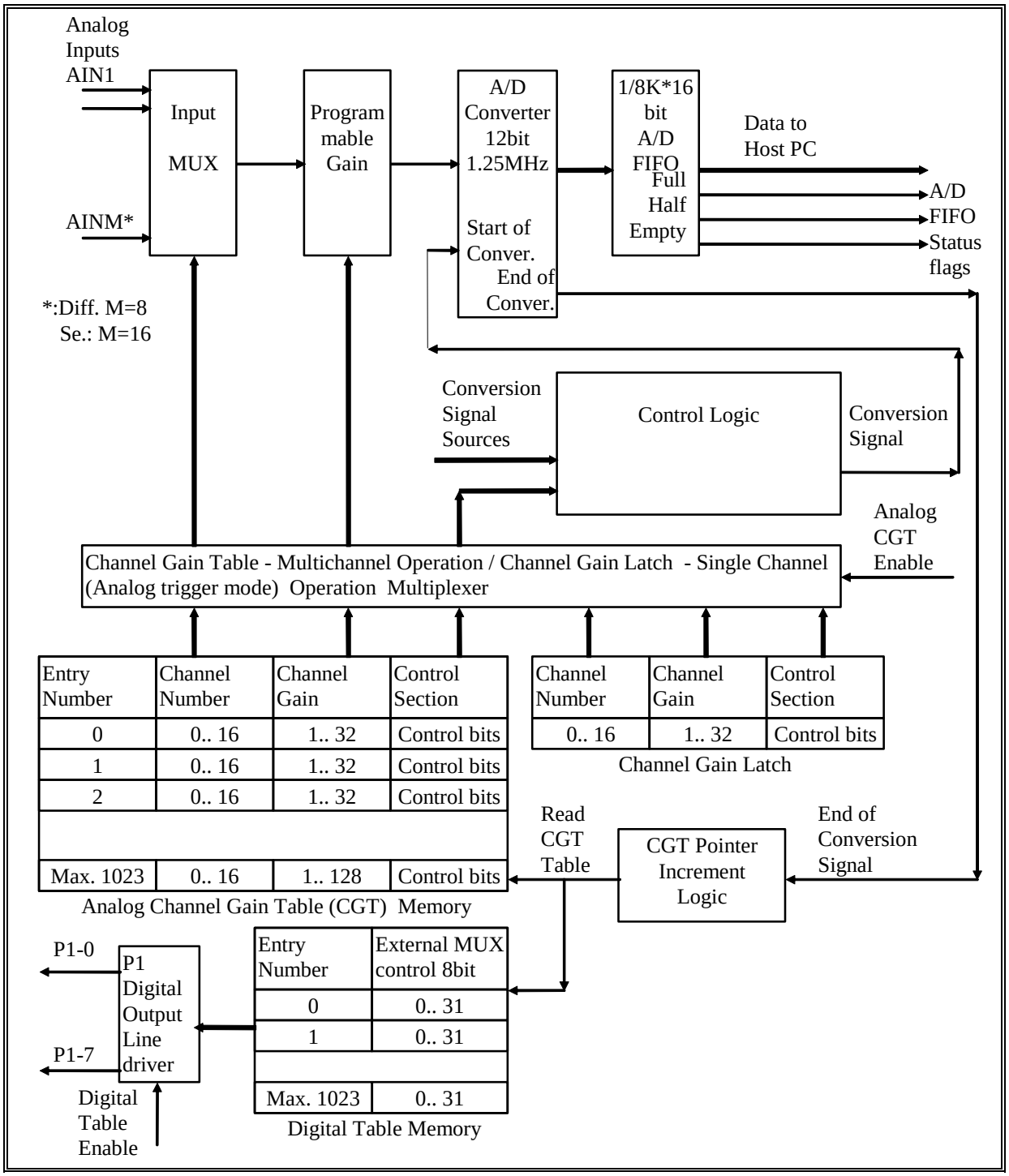
The Channel-Gain Table lets you sample channels in any order, at high speeds, with a different gain on each channel. This 1024 x 24-bit memory supports complex channel-gain scan sequences, including digital output control. Using the digital output control feature, you can control external input expansion boards such as the TMX32 to expand channel capacity to up to 512 channels. When used, these control lines are output on Port 1. When the digital lines are not used for this feature, they are available for other digital control functions.

A skip bit is provided in the channel-gain data word to support different sampling rates on different channels. When this bit is set, an A/D conversion is performed on the selected channel but not stored in the FIFO.

In the case of multi-channel operation the Channel Gain Table must be enabled by appropriate software instruction. Then the Channel Gain Table must be cleared and filled with the appropriate entries by the appropriate software instruction. After this setup the read pointer of the Channel Gain Table points to the first entry. The first A/D conversion works according to the first entry of CGT. After an active Conversion Signal the A/D Converter asserts the End of Conversion Signal. This signal increases the read pointer of the Channel Gain Table and writes the converted data to the A/D FIFO and the sampled High-Speed Digital Input lines to the FIFO if the High Speed Digital Input is in Data Marker Mode. The next conversion works according to the second entry of CGT etc. After reading the last entry, the read pointer automatically returns to the first entry of the CGT. This returning can be activated by Reset Channel Gain Table software instruction.

The Channel Gain Table assures the possibility of independent programming of the channel type (GRSE, NRSE or DIFF), the channel gain (1..32) and the input range (+/-5V, +/-10V or 0..10V). Therefore CGT assures the possibility of simultaneous update the D/A1 and D/A2 with the appropriate input channels. These functions can be reached via the bits CGT entries.

Figure 8: Channel Gain Table



5.2.2 Analog-to-Digital Conversion

The DM35520 is software configurable on a channel-by-channel basis for up to 16 single-ended or 8 differential analog inputs. Software programmable unipolar and bipolar inputs ranges and gains allow easy interfacing to a wide range of sensors.

A/D Converter

The 12-bit successive approximation A/D converter accurately digitizes dynamic input voltages in 0.8 microseconds, for a maximum throughput rate of 1.25MHz. The converter IC contains a sample-and-hold amplifier, a 12-bit A/D converter, a 2.5-volt reference, a clock, and a digital interface to provide a complete A/D conversion function on a single chip. Its low power CMOS logic combined with a high precision, low noise design give you accurate results.

Conversions are controlled by software command, by pacer clock, by using triggers to start and stop sampling, or by the sample counter to acquire a specified number of samples. An on-board or external pacer clock can be used to control the conversion rate.

A/D FIFO – Sample Buffer

A first in, first out (FIFO) 1k sample buffer helps your computer manage the high throughput rate of the A/D converter by providing an elastic storage bin for the converted data. Even if the computer does not read the data as fast as conversions are performed, conversions will continue until a FIFO full flag is sent to stop the converter.

The sample buffer does not need to be addressed when you are writing to or reading from it; internal addressing makes sure that the data is properly stored and retrieved. All data accumulated in the sample buffer is stored intact until the PC is able to complete the data transfer. Its asynchronous operation means that data can be written to or read from it at any time, at any rate. When a transfer does begin, the data first placed in the FIFO is the first data out.

Data Transfer

The converted data can be transferred to PC memory in one of three ways. Data can be transferred using the programmed I/O mode, the interrupt mode or using the on-board DMA controller. A special interrupt mode using a REP INS (Repeat Input String) instruction supports very high speed data transfers. By generating an interrupt when the FIFO's half full flag is set, a REP INS instruction can be executed, transferring data to PC memory and emptying the sample buffer at the maximum rate allowed by the data bus. The DMA mode assures the fastest burst mode bus master data transfer.

5.2.3 Digital-to-Analog Conversion

The digital-to-analog (D/A) circuitry features two independent 12-bit analog output channels with individually programmable output ranges of ±5 volts, 0 to +5 volts, ±10 volts or 0 to +10 volts. Each channel has its own 1K sample FIFO buffer for data storage before being output. Data can be continuously written to the buffer producing a non-repetitive output waveform or a set of data can be written into the buffer and continuously cycled to produce a repeating waveform. Data can be written into the output buffers by memory write instruction. Updating of the analog outputs can be done through software or by several different clocks and triggers. The outputs can be updated simultaneously or independently.

5.2.4 Timer/Counters

One 8254 programmable 16-bit, 8-MHz interval timer, and internal ten 16/24 bit timers provide a wide range of timing and counting functions.

The internal timers work as a binary count down mode.

The 8254 is the User TC. All three counters on this chip are available for user functions. Each 16-bit timer/counter has two inputs, CLK in and GATE in, and one output, timer/counter OUT. The sources of User TC clock and gate inputs can be programmed. Each TC can be programmed as binary or BCD down counters by writing the appropriate data to the command word. The command word also lets you set up the mode of operation. The six programmable modes are:

Mode 0 Event Counter (Interrupt on Terminal Count)
Mode 1 Hardware-Retriggerable One-Shot
Mode 2 Rate Generator
Mode 3 Square Wave Mode
Mode 4 Software-Triggered Strobe
Mode 5 Hardware Triggered Strobe (Retriggerable)

5.2.5 DIGITAL I/O

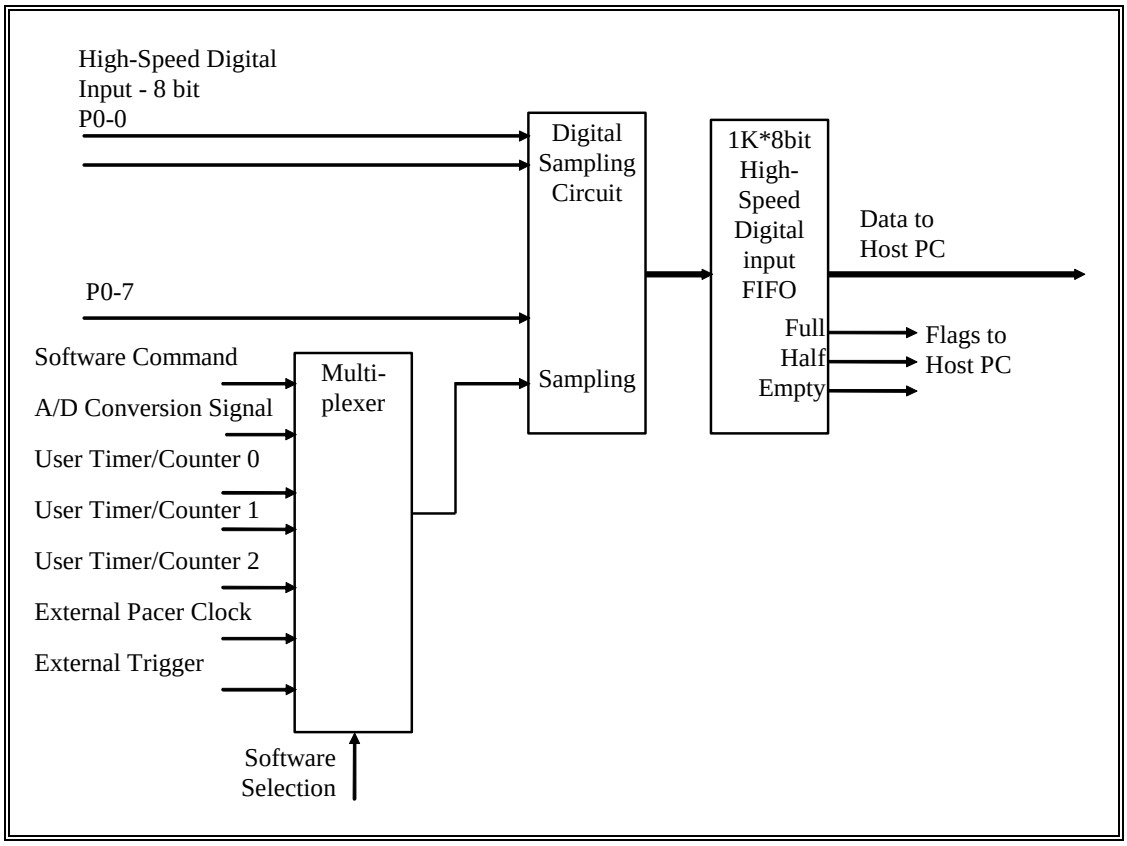
The DM35520 has 16 buffered TTL/CMOS digital I/O lines with eight independent, bit programmable lines at Port 0, and an 8-bit programmable port, Port 1. The bit programmable lines support RTD's two Advanced Digital Interrupt modes. An interrupt can be generated when any bit changes value (event interrupt), or when the lines match a programmed value (match interrupt). For either mode, masking can be used to monitor selected lines. Lines are pulled up by 10kΩ resistors. Port 0 and Port 1 are accessed through the 68 pin I/O connector.

5.2.6 HIGH-SPEED DIGITAL INPUTS

The DM35520 has 8 bit buffered TTL/CMOS High speed digital Input lines with 1K Sample FIFO buffer. These lines are shared with the Digital I/O P0 port. Lines are pulled up by 10kΩ resistors and can be accessed through the 68 pin I/O connector.

Figure 9, shows the block diagram of High-Speed Digital Input section. The sampling signal can be software selectable.

Figure 9: High-Speed Digital Inputs



The Sampled data are written automatically to the High-Speed Digital Input FIFO. Data can be transferred to PC memory in one of two ways. Data can be transferred using the programmed I/O mode, the interrupt mode or using the on-board DMA controller. The Interrupt mode assures the possibility getting Interrupt after an appropriate number of data. The number of data in High-Speed Digital Input FIFO can be counted by the User TC1. User TC1 can be an interrupt Source.

5.2.7 SYNCBUS

The three-line SyncBus assures the possibility of using multiple DM35520 in one computer synchronously

5.2.8 MCBSP MULTI-CHANNEL BUFFERED SERIAL PORT

The ten-line (including GNDs) McBSP (defined by Texas Instruments) assures the possibility of using a dspModule with DAQ boards together. This means, that the connected DSP (f. e. RTD SPM 6020/6030) has a direct connection to the analog world using the DM35520 as a front-end board.

5.3 Analog Connections

5.3.1 Connecting Analog Input Pins

The DM35520 provides flexible input connection capabilities to accommodate a wide range of sensors. You can mix several *input* modes:

- Ground Referenced Single-Ended (GRSE)
- Non Referenced Single-Ended (NRSE)
- Differential (DIFF) without ground reference, Differential with a dedicated ground, Differential with a separate ground reference through a 10 kΩ resistor.

The Differential mode with a dedicated ground is actually a single ended mode, but the channel number is only 8 channel and each channel has a dedicated ground pin and ground wire in the cable between the board and the signal conditioning card. This mode can be useful when the shielding of the signal is important.

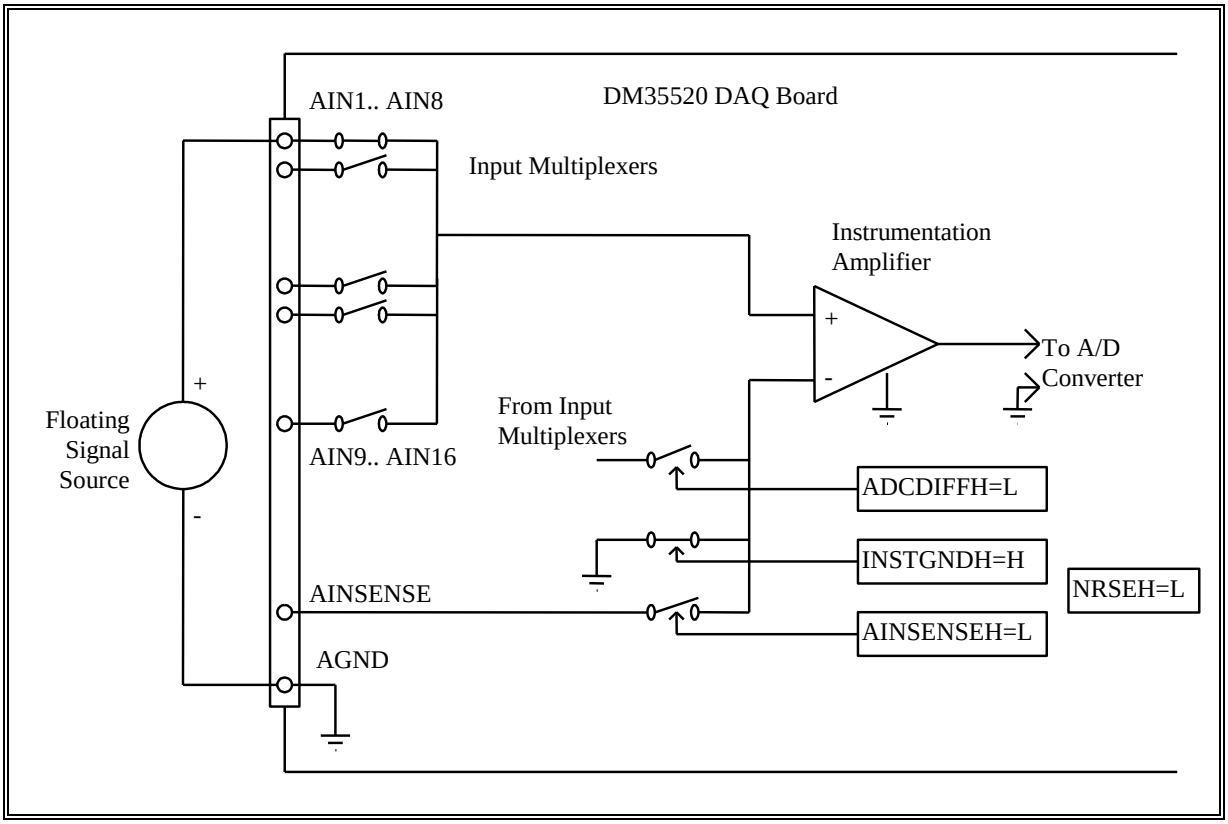
In the following the analog input modes are explained by text and Figures. In the Figures you can see the simplified block diagram of the analog input section of the Board. The NRSEH, ADCDIFFH INSTGNDH, AINSENSEH are the inside logic state variables for controlling the analog input operation. The switches are realized by analog multiplexers.

Ground Referenced Single-Ended (GRSE) Input Mode

This mode is suggested only for floating signal sources to avoid the ground loops. To configure the GRSE analog input, connect the high side of the input signal to the selected analog input channel, AIN1 through AIN16, and connect the low side to any of the ANALOG GND pins available at the connector.

In the Figure 10, you can see the switch states of this mode. The NRSEH bit is in low state which means that this is not NRSE mode. ADCDIFFH bit is in low state because this is not a differential mode. The INSTGNDH bit is in high state controlling the connection of low side of Instrumentation Amplifier to Analog Ground (AGND). The AINSENSEH bit is in low state because the reference signal of Instrumentation Amplifier is the Analog Ground.

Figure 10: Ground Referenced Single Ended input mode

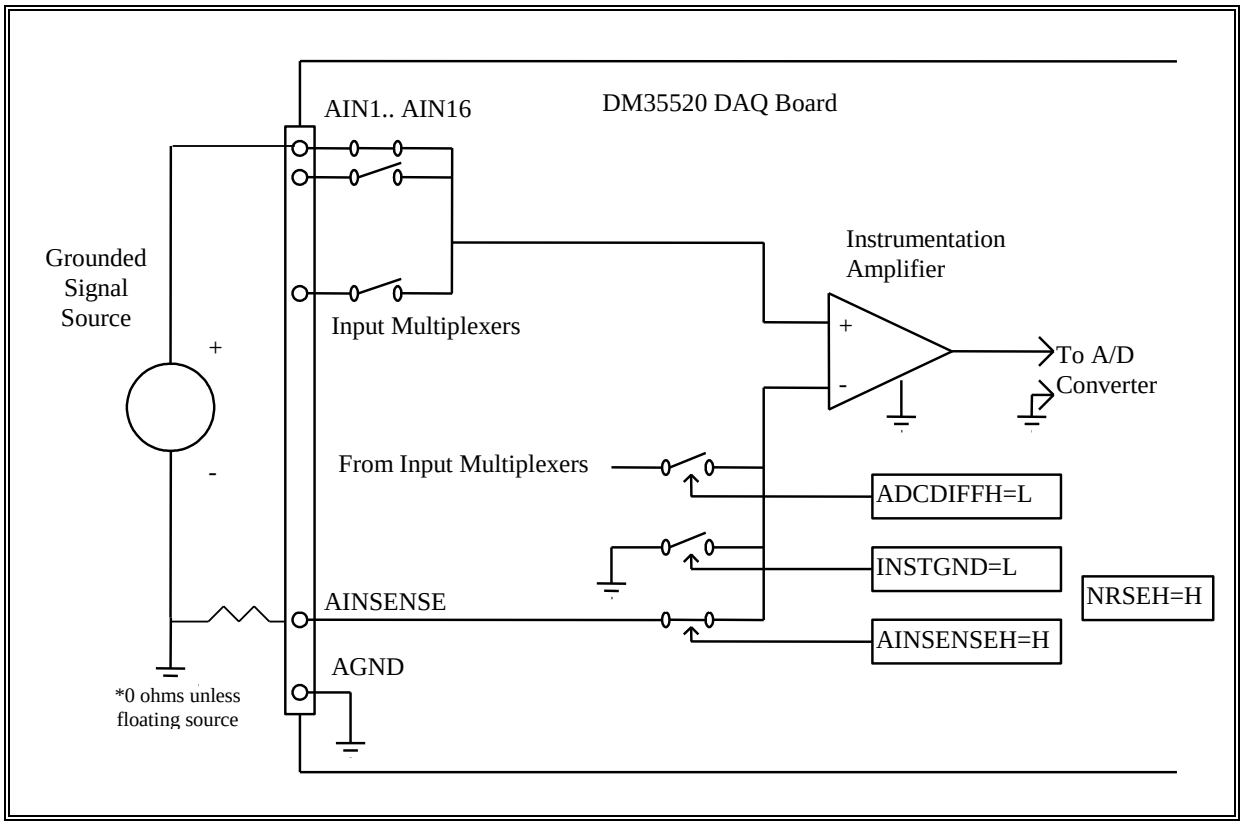


Non Referenced Single-Ended (NRSE) Input Mode

This mode can be used - first of all - for grounded signal sources (in the Figure 11) but can be used for floating sources too. In the case of floating sources an external resistor is needed to ground the AINSENSE signal. To configure the NRSE analog input, connect the high side of the input signal to the selected analog input channel, AIN1 through AIN16, and connect the low side to the AINSENSE pin available at the connector.

In the Figure 11, you can see the switch states of this mode. The NRSEH bit is in high state which means that this is the NRSE mode. ADCDIFFH bit is in low state because this is not a differential mode. The AINSENSEH bit is in high state controlling the connection of low side of Instrumentation Amplifier to AINSENSE signal. The INSTGNDH bit is in low state because the reference signal of Instrumentation Amplifier is the AINSENSE signal.

Figure 11: Non Referenced Single-Ended input mode



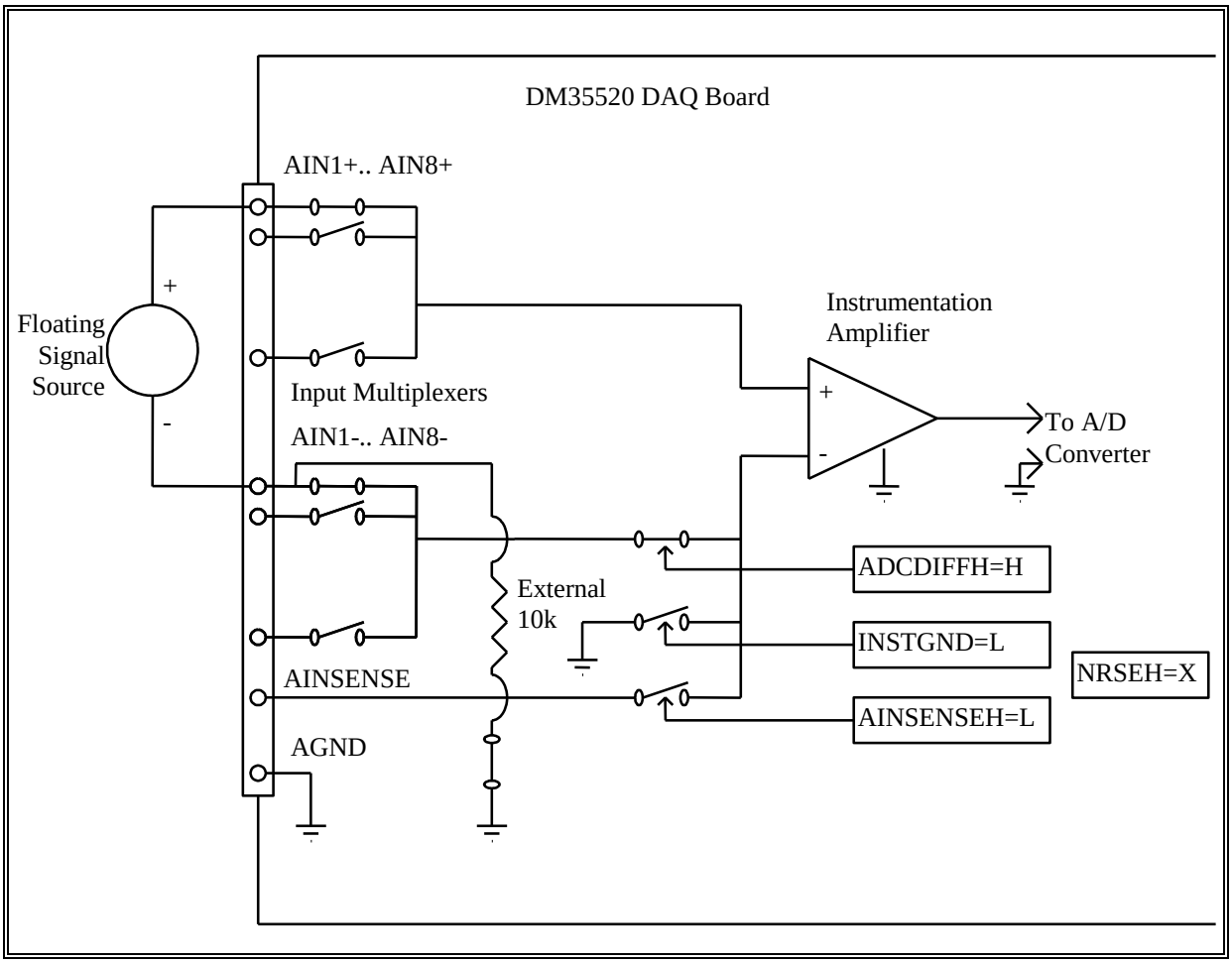
Differential (DIFF) Input Mode

For differential inputs, your signal source may or may not have a separate ground reference. When using the differential mode, you may need a reference to ground for a signal source without a separate ground reference or a direct grounding connection. (Figure 12) If either grounding scheme is need external components are needed.

Connect the high side of the analog input to the selected analog input channel, AIN1+ through AIN8+, and connect the low side to the corresponding AIN- pin.

In the Figure 12 You can see the switch states of this mode. The state of NRSEH bit is indifferent in the DIFF mode. The ADCDIFFH bit is in high state controlling the connection of low side of Instrumentation Amplifier to AIN- signal. The INSTGNDH bit is in low state because the reference signal of Instrumentation Amplifier is the AIN- signal. The AINSENSEH bit is in low state because the reference signal of Instrumentation Amplifier is the AIN- signal in DIFF mode.

Figure 12: Differential input mode



5.3.2 Connecting Analog Outputs

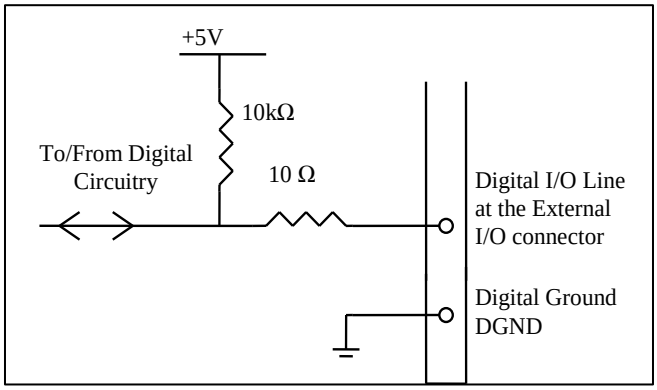
For each D/A outputs, connect the high side of the device receiving the output to the AOUT channel and connect the low side of the device to an ANALOG GND.

5.3.3 Connecting the Timer/Counters and Digital I/O

For all of these connections, the high side of an external signal source or destination device is connected to the appropriate signal pin on the I/O connector, and the low side is connected to any DIGITAL GND.

The termination circuit of digital input/output can be seen in the Figure 13. In the case of digital input lines the serial 10Ω resistor is missing, and in the case of digital output lines the 10kΩ pull-up resistor is missing.

Figure 13: Digital I/O



5.4 Address Spaces of DM35520

The DM35520 is a PCI bus board with a PCI Bus Master Interface. The board has four configuration register areas and two operation register areas. The configuration Registers are the PCI Configuration Register and the Local Configuration Register, the Runtime Registers and the DMA Registers.

The PCI Configuration Registers, Runtime Registers and the Local Configuration Registers are filled out from an EEPROM on the board after power up. The description of the registers and the content of the EEPROM can be found in the Appendix.

The most interesting areas for the user are the operation register address spaces of the board. There are two operation address spaces, the Local Address Space 0 (LAS0) and 1 (LAS1). These spaces can be accessed by memory instructions and - in the case of LAS1 - the on-board DMA controller. The base addresses of these spaces can be read from the PCI configuration area.

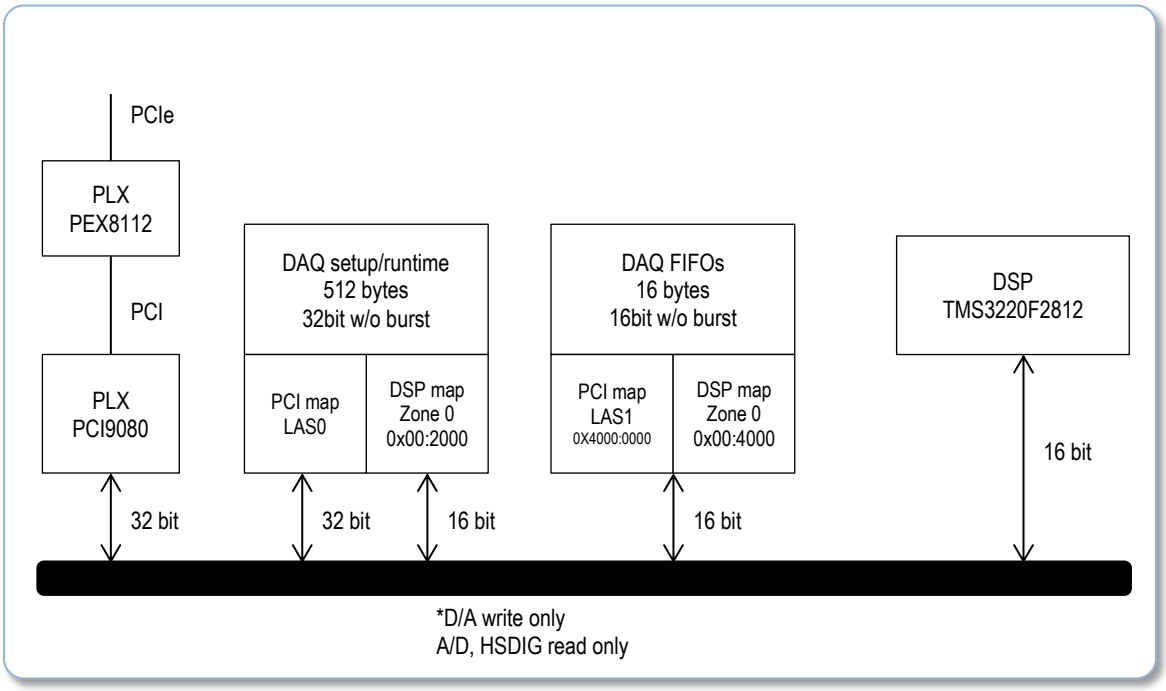
LAS0 is a 512 byte long 32 bit wide memory-mapped area. It can be used to runtime control and setup, configure of the DM35520 board.

LAS1 is a 16 byte long 16 bit wide register area for transferring data/code from/to the board.

The Runtime registers can be used to control the EEPROM access, and the Interrupt operation of the board.

The DMA registers can be used to control the two-channel on-board DMA controllers to make fast data transfer between the FIFO and the PC.

Figure 14: Address Space/ Local Bus Access



5.4.1 LOCAL ADDRESS SPACE 0 (LAS0) – RUNTIME AREA

Address LAS0 space	LAS0 Description
000 0FF	Runtime Area
100 1FF	Setup Area

Table 18: LAS0 Register Map Offsets

Read Function	Write Function	Local Address Space 0 Offset
-	-	000h
I2C Data line Read (planned feature)	I2C Data line Write (planned feature)	004h
Read User Inputs	Write User Outputs	008h
Software DAC clock Start	Software DAC clock Stop	00Ch
Read FIFO Status	Software A/D Start	010h
-	Software D/A1 Update	014h
-	Software D/A2 Update	018h
-	-	01Ch
-	-	020h
-	Software Simultaneous D/A1 and D/A2 Update	024h
Software Pacer Start	Software Pacer Stop	028h
Read Timer Counters Status	Software high-speed input Sample Command	02Ch
Read Interrupt Status	Write Interrupt Enable Mask Register	030h
Clear Interrupt set by the Clear Mask	Set Interrupt Clear Mask	034h

Read Function	Write Function	Local Address Space 0 Offset
Read Interrupt Overrun Register	Clear Interrupt Overrun Register	038h
-	I2C Data line Write enable (planned feature)	03Ch
Read Pacer Clock Counter value (24 bit)	Load count in Pacer Clock Counter (24 bit)	040h
Read Burst Clock Counter value 16bit	Load count in Burst Clock Counter 16bit	044h
Read A/D Sample counter value 16bit	Load count in A/D Sample counter 16bit	048h
Read D/A1 Update counter value 16bit	Load count in D/A1 Update counter 16bit	04Ch
Read D/A2 Update counter value 16bit	Load count in D/A2 Update counter 16bit	050h
Read Delay Counter value 16 bit	Load count in Delay Counter 16 bit	054h
Read About Counter value 16 bit	Load count in About Counter 16 bit	058h
Read DAC clock value DM35520	Load count in DAC clock DM35520	05Ch
Read 8254 User TC 0 value	Load count in 8254 User TC 0	060h
Read 8254 User TC 1 value	Load count in 8254 User TC 1	064h
Read 8254 User TC 2 value	Load count in 8254 User TC 2	068h
Reserved	Program counter mode for 8254 User TC	06Ch
Read Port 0 digital input lines	Program Port 0 digital output lines	070h
Read Port 1 digital input lines	Program Port 1 digital output lines	074h
Clear digital IRQ status flag/read Port 0 direction, mask or compare register	Clear digital chip/program Port 0 direction, mask or compare register	078h
Read Digital I/O Status word	Program Digital Control Register & Digital Interrupt enable	07Ch
Read Digital I/O Status word	Program Digital Control Register & Digital Interrupt enable	07Ch
DSP Command register to be written from the Host side and read from DSP	DSP status to written to by DSP and read form Host side	0B0h
Read analog connection DIO mask	Write analog connection DIO mask	0E0h
Read analog connection DIO data values from output pins	Write analog connection DIO data values to output pins	0E4h
Read analog connection DIO direction	Write analog connection DIO direction	0E8h
Read analog connection DIO IRQ status	-	0ECh

000h: Firmware version number (Read Only)

Read Operation (32-bit)
A read provides the FPGA version.

B31 – B8	B7 – B4	B3 – B0

B31-B8: Reserved
B7-B4: FPGA version
B3-B0: Reserved

008h: User Input read / User Output Write (Read/Write)

Read Operation (32-bit, two bits are used)
A read provides the User Input 0 and User Input 1 bits as below. These digital input lines come from the External I/O connector. The User Input bits are sampled by the read instruction.

B31 – B2	B1	B0

B31-B8: Reserved
B1: User Input 1 state
B0: User Input 0 state

Write operation (32-bit, two bits are used)
These bits go to the External I/O Connector of the board. If the source of the User Output x is set to the Software Programmable state by the 0x070E and 0x070F Functions, the state of the User Output bits can be programmed by this write operation.

B31-B2: Reserved
B1: User Output 1 state
B0: User Output 0 state

00Ch: Software DAC Clock (Read/Write)

Read Operation starts the D/A Clock
Write operation stops the D/A Clock

010h: FIFO Status Register / A/D Conversion Start (Read/Write)

Read Operation (32-bit, upper word is not used)
A read provides the status bits of the FIFO as below.

B31 – B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

B0: 0 D/A1 FIFO empty; 1 D/A1 FIFO not empty
B1: 0 D/A1 FIFO not half empty; 1 D/A1 FIFO half empty
B2: 0 D/A1 FIFO full; 1 D/A1 FIFO not full
B3: Reserved
B4: 0 D/A2 FIFO empty; 1 D/A2 FIFO not empty
B5: 0 D/A2 FIFO not half empty; 1 D/A2 FIFO half empty
B6: 0 D/A2 FIFO full; 1 D/A2 FIFO not full
B7: Reserved
B8: 0 A/D FIFO empty; 1 A/D FIFO not empty
B9: 0 A/D FIFO half full; 1 A/D FIFO not half full
B10: 0 A/D FIFO full; 1 A/D FIFO not full
B11: Reserved
B12: 0 HSDI FIFO empty; 1 HSDI FIFO not empty
B13: 0 HSDI FIFO half full; 1 HSDI FIFO not half full
B14: 0 HSDI FIFO full; 1 HSDI FIFO not full
B31-B15: Reserved

Write operation (16-bit)
Any value written to this register generates a Software A/D start command.

014h: Software update D/A 1 (Write)

Write Operation (32-bit)
Any value written to this register updates the D/A 1 if the updates source is software updates.

018h: Software update D/A 2 (Write)

Write Operation (32-bit)
Any value written to this register updates the D/A 2 if the updates source is software updates.

024h: Simultaneous Software update D/A 1 and D/A 2 (Write)

Write Operation (32-bit)
Any value written to this register simultaneously updates the D/A 1 and D/A 2 converters if the updates source is software updates.

028h: Pacer Clock Software trigger (Read/Write)

Read Operation (32-bit)
A read means a software start trigger of the Pacer Clock if the start trigger source of the pacer clock is set to a software trigger. The read value is unimportant
Write Operation (32-bit)
Any written value means a software stop trigger of the Pacer Clock if the stop trigger source pacer clock is set to a software trigger.

02Ch: Pacer/Burst Clock Timer Status Register / Software High Speed Input Sample Command (Read/Write)

Read Operation (32-bit, upper word is not used)
A read provides the status of the gate of the Timer Counter circuits.

B31 – B6	B5	B4	B3	B2	B1	B0

B0: 0 Pacer clock gated; 1 Pacer clock enabled
B1: 0 Burst clock disabled; 1 Burst clock enabled
B2: 0 Pacer clock delayed start trigger over;
1 Pacer clock delayed start trigger in progress
B3: 0: Pacer clock About trigger completed;
1: Pacer clock About trigger in progress
B4: 0 Pacer clock can **only** be start triggered by software pacer start command;
1 Pacer clock can be start triggered
B5: 0 Analog sampling is not halted
1 Analog sampling is halted by A/D FIFO full. It can be cleared by A/D FIFO clear command
B31-B6 Reserved

Write Operation (32-bit)
A write means a software Sample command for 8 bit High-Speed Digital Input lines if the sampling source is the software command. This command means a High-Speed Digital Input FIFO write procedure. The written data does not care.

030h: Interrupt Status/Mask Register (Read/Write)

The DM35520 board has a built-in Priority Interrupt Controller that assures the possibility of multiply interrupt sources can generate interrupt ordered by their priority order. The highest priority is numbered by 0. The usage of the built-in Priority Interrupt controller is very easy:

1. Set the Interrupt Mask Register (Write LAS0 + 030h) in your initialization part of the software. Enable the required interrupt sources by ones
2. The built-in Priority Interrupt Controller orders the interrupt requests and transmits them to the PC. If an interrupt occurs, you can identify the active source by reading the Interrupt Status Register (Read LAS0 + 30h) in the Interrupt Service Routine. In the Interrupt Status Register always one bit is high indicating the active interrupt source. After identifying the source the request can be serviced.
3. Clear the serviced Interrupt request by the Interrupt Clear register. First write the clear mask writing the appropriate bit pattern to the address LAS0 + 034h. Then a dummy read from LAS0 + 034h executes the clear.

If you want to check that during servicing the interrupt a new interrupt has not come yet, after clearing the interrupt request read the Interrupt Overrun Register. Zero bits mean, that all interrupt have been serviced correctly. One means that a new interrupt occurred before the previous service was finished. After reading the Interrupt Overrun Register, clear it.

Read Operation (32 bit, upper word does not used)
A read provides the status flag of the interrupt.

Lowest Priority — Highest Priority

B31 – B16

B16	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

B0:	0 Board FIFO Write inactive;	1 Board FIFO Write active
B1:	0 Reset CGT inactive;	1 Reset CGT active
B2:	Reserved	
B3:	0 Pause CGT inactive;	1 Pause CGT active
B4:	0 About Counter Out inactive;	1 About Counter Out active
B5:	0 Delay Counter Out inactive;	1 Delay Counter Out active
B6:	0 A/D Sample Counter inactive;	1 A/D Sample Counter active
B7:	0 D/A1 Update Counter inactive;	1 D/A1 Update Counter active
B8:	0 D/A2 Update Counter inactive;	1 D/A2 Update Counter active
B9:	0 User TC1 Out inactive;	1 User TC1 Out active
B10:	0 User TC1 Inverted Out inactive;	1 User TC1 Inverted Out active
B11:	0 User TC2 Out inactive;	1 User TC2 Out active
B12:	0 Digital Interrupt inactive;	1 Digital Interrupt active
B13:	0 External Interrupt inactive;	1 External Interrupt active
B14:	0 External Trigger rising edge inactive;	1 External Trigger rising edge active
B15:	0 External Trigger falling edge inactive;	1 External Trigger falling edge active
B31-B16	Reserved	

Write Operation (32 bit, upper word does not used)
The interrupt mask register:

B0:	0 Board FIFO Write disabled;	1 Board FIFO Write enabled
B1:	0 Reset CGT disabled;	1 Reset CGT enabled
B2:	Reserved	
B3:	0 Pause CGT disabled;	1 Pause CGT enabled
B4:	0 About Counter Out disabled;	1 About Counter Out enabled
B5:	0 Delay Counter Out disabled;	1 Delay Counter Out enabled
B6:	0 A/D Sample Counter disabled;	1 A/D Sample Counter enabled
B7:	0 D/A1 Update Counter disabled;	1 D/A1 Update Counter enabled
B8:	0 D/A2 Update Counter disabled;	1 D/A2 Update Counter enabled
B9:	0 User TC1 Out disabled;	1 User TC1 Out enabled
B10:	0 User TC1 Inverted Out disabled;	1 User TC1 Inverted Out enabled
B11:	0 User TC2 Out disabled;	1 User TC2 Out enabled
B12:	0 Digital Interrupt disabled;	1 Digital Interrupt enabled
B13:	0 Digital Interrupt disabled;	1 Digital Interrupt enabled
B14:	0 External Trigger rising edge disabled;	1 External Trigger rising edge enabled
B15:	0 External Trigger falling edge disabled;	1 External Trigger falling edge enabled
B31-B16	Reserved	

034h: Interrupt Clear Register (Read/Write)

Read operation (32 bit, upper word does not used)
A read clears the interrupt status flags of the selected source set by the clear mask.

B31 – B16

B16	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

B0: 0 Board FIFO Write clear no overrun; 1 Board FIFO Write clear overrun
B1: 0 Reset CGT clear no overrun; 1 Reset CGT clear overrun
B2: Reserved
B3: 0 Pause CGT clear no overrun; 1 Pause CGT clear overrun
B4: 0 About Counter Out no overrun; 1 About Counter Out overrun
B5: 0 Delay Counter Out no overrun; 1 Delay Counter Out overrun
6: 0 A/D Sample Counter clear no overrun; 1 A/D Sample Counter clear overrun
B7: 0 D/A1 Update Counter clear no overrun; 1 D/A1 Update Counter clear overrun
B8: 0 D/A2 Update Counter clear no overrun; 1 D/A2 Update Counter clear overrun
B9: 0 User TC1 Out clear no overrun; 1 User TC1 Out clear overrun
B10: 0 User TC1 Inverted Out clear no overrun; 1 User TC1 Inverted Out clear overrun
B11: 0 User TC2 Out clear no overrun; 1 User TC2 Out clear overrun
B12: 0 Digital Interrupt clear no overrun; 1 Digital Interrupt clear overrun
B13: 0 External Interrupt clear no overrun; 1 External Interrupt clear overrun
B14: 0 External Trigger rising edge clear no overrun;
1 External Trigger rising edge clear overrun
B15: 0 External Trigger falling edge clear no overrun;
1 External Trigger falling edge clear overrun
B31-B16 Reserved

Write operation (32 bit, upper word does not used)
B0: 0 Board FIFO Write clear disabled; 1 Board FIFO Write clear enabled
B1: 0 Reset CGT clear disabled; 1 Reset CGT clear enabled
B2: Reserved
B3: 0 Pause CGT clear disabled; 1 Pause CGT clear enabled
B4: 0 About Counter Out clear disabled; 1 About Counter Out clear enabled
B5: 0 Delay Counter Out clear disabled; 1 Delay Counter Out clear enabled
B6: 0 A/D Sample Counter clear disabled; 1 A/D Sample Counter clear enabled
B7: 0 D/A1 Update Counter clear disabled; 1 D/A1 Update Counter clear enabled
B8: 0 D/A2 Update Counter clear disabled; 1 D/A2 Update Counter clear enabled
B9: 0 User TC1 Out clear disabled; 1 User TC1 Out clear enabled
B10: 0 User TC1 Inverted Out clear disabled; 1 User TC1 Inverted Out clear enabled
B11: 0 User TC2 Out clear disabled; 1 User TC2 Out clear enabled
B12: 0 Digital Interrupt clear disabled; 1 Digital Interrupt clear enabled
B13: 0 External Interrupt clear disabled; 1 External Interrupt clear enabled
B14: 0 External Trigger rising edge clear disabled;
1 External Trigger rising edge clear enabled
B15: 0 External Trigger falling edge clear disabled;
1 External Trigger falling edge clear enabled
B31-B16 Reserved

038h: Interrupt Overrun Register (Read/Write)

Write operation (32 bit, upper word does not used)
A write clears all bits of the Interrupt Overrun Register.

Read operation (32 bit, upper word does not used)
A read provides the Interrupt Overrun Register. If the interrupts serviced in time all bits are zeros. If a new interrupt request comes before the pervious has been serviced and the request is cleared, the appropriate overrun bit goes into high.

040h: Pacer Clock Counter (Read/Write)

The Pacer Clock Counter is a 24 bit wide down counter synthesized in the control EPLD of the board. Its clock signal is the 20 or 8MHz clock. This primary frequency is initially 8MHz, but can be modified by writing LAS0+ 1DCh. The output signal is the Pacer Clock signal, which is in a high state during counting, and goes to the low state when the counter rolls to zero.

B31 – B24	B23 – B0

Read /Write operation (32bit, 24 bits are used)
B23-B0: 24 bit Pacer Clock counter value (counting down begins as soon as counter is loaded)
B31-B24 Reserved

044h: Burst Clock Counter (Read/Write)

The Burst Clock Counter is a 16 bit wide down counter synthesized in the control EPLD of the board. Its clock signal can be 8MHz or 20MHz clock signal (see the function at LAS0+1E0h). The output signal is the Burst Clock signal, which is in a high state during counting, and goes to the low state when the counter rolls to zero. The 16 bit wide burst clock counter assures the 122Hz minimum Burst clock frequency.

B31 – B16	B15 – B0

Read /Write operation (32bit, 16 bits are used)
B15-B0: 16 bit Burst Clock counter value
B31-B16: Reserved

048h: A/D Sample Counter (Read/Write)

The A/D Sample Counter is a 16 bit wide down counter synthesized in the control EPLD of the board. Its clock signal can be programmed by writing the LAS0 +170h address. The output signal is the A/D Sample Counter signal, which is in high state during counting, except the zero state of the counter. This signal can be an interrupt source. If the counter value is zero, the A/D Sample Counter output is in low state and the high-low transition can generate an interrupt. After loading the sample counter, an interrupt is immediately generated. This can be eliminated by disabling the interrupt during the loading process. If a number n is written into the Sample Counter, then the counter content will reach the zero value, and generates an interrupt after **n+1** event.

The 16 bit wide A/D Sample Counter assures the 65536 maximum value of counting A/D samples.

B31 – B16	B15 – B0

Read /Write operation (32bit, 16 bits are used)
B15-B0: 16 bit A/D Sample counter value
B31-B16: Reserved

04Ch: D/A 1 Update Counter (Read/Write)

The D/A1 Update Counter is a 16 bit wide down counter synthesized in the control EPLD of the board. Its clock signal is the D/A1 update signal. The output signal is the D/A1 Update Counter signal, which is in high state during counting, and goes to the low state when the counter rolls to zero. The 16 bit wide D/A1 Update Counter assures the 65536 maximum value of counting D/A1 updates.

B31 – B16	B15 – B0

Read /Write operation (32bit, 16 bits are used)
B15-B0: 16 bit D/A 1 Update counter value
B31-B16: Reserved

050h: D/A 2 Update Counter (Read/Write)

The D/A 2 Update Counter is a 16 bit wide down counter synthesized in the control EPLD of the board. Its clock signal is the D/A 2 update signal. The output signal is the D/A 2 Update Counter signal, which is in high state during counting, and goes to the low state when the counter rolls to zero. The 16 bit wide D/A 2 Update Counter assures the 65536 maximum value of counting D/A 2 updates.

B31 – B16	B15 – B0

Read /Write operation (32bit, 16 bits are used)
B15-B0: 16 bit D/A 2 Update counter value
B31-B16: Reserved

054h: Delay Counter (Read/Write)

The Delay Counter is a 16 bit wide down counter synthesized in the control EPLD of the board. Its clock signal is the same frequency clock signal as the Pacer Clock. During the down counting process the Pacer clock is shut down. The 16 bit wide Delay Counter assures the 65535 maximum value of Pacer clock period delaying the Start Pacer Clock.

B31 – B16	B15 – B0

Read /Write operation (32bit, 16 bits are used)
B15-B0: 16 bit Delay counter value
B31-B16: Reserved

058h: About Counter (Read/Write)

The About Counter is used for delayed Pacer Clock Stop function. If the sampling clock is the Pacer Clock, the number of samples to acquire after stop trigger is programmed in the About Counter. The about Counter is a 16 bit wide down counter synthesized in the control EPLD of the board. The 16 bit wide About Counter assures the 65535 maximum value of samples delaying the Stop Pacer Clock. When the about counter is loaded, it triggers the about counter interrupt. When writing code one should ignore this first expected interrupt.

B31 – B16	B15 – B0

Read /Write operation (32bit, 16 bits are used)
B15-B0: 16 bit About counter value
B31-B16: Reserved

05Ch: DAC Clock Counter (Read/Write)

The DAC Clock Counter is a 24 bit wide down counter synthesized in the control EPLD of the board. Its clock signal is the 8 / 20MHz clock. The output signal is the DAC Clock signal, which is in high state during counting, and goes to the low state when the counter rolls to zero. The DAC Clock may be the update signal of the D/A converters.

B31 – B24	B23 – B0

Read /Write operation (32bit, 16 bits are used)
B23-B0: 16 bit DAC Clock counter value (counting down begins as soon as counter is loaded)
B31-B24: Reserved

060h, 064h, 068h: User Timer/Counter 0, 1, 2 (Read/Write)

The DM35520 DAQ Board has an 8254 Timer Counter chip for the user. The clock sources and gates can be programmed.

B31 – B8	B7 – B0

Read/Write operation (32bit, 16 bits are used)
B7-B0: Two 8 bit accesses will return/write the count in TC0/1/2 respectively (LSB followed by MSB)
B31-B8: Reserved

06Ch: User Timer/Counter control word (Write Only)

Write operation (32bit, 8 bits are used)

Accesses the timer/counter's control register to directly control the three 16-bit counters, 0, 1, and 2.

B31 – B8	B7	B6	B5	B4	B3	B2	B1	B0

B0: 0 Binary; 1 BCD
B3-B1: 000 Mode 0 event count
001 Mode 1 Programmable one shot
010 Mode 2 Rate Generator
011 Mode 3 Square Wave Rate Generator
100 Mode 4 Software Triggered Strobe
101 Mode 5 Hardware Triggered Strobe
B5-B4: 00 Latching operation
01 Read/Load LSB only
01 Read/Load MSB only
11 Read/Load LSB then MSB
B7-B6: 00 Counter 0
01 Counter 1
01 Counter 2
11 Read back setting
B31-B8 Reserved

070h: Digital I/O chip Port 0, Bit Programmable Port (Read/Write)

This port transfers the 8-bit Port 0 bit programmable digital input/output data between the board and external devices. The bits are individually programmed as input or output by writing to the Direction Register at LAS0+078h. For all bits set as inputs, a read reads the input values and a write is ignored. For all bits set as outputs, a read reads the last value sent out on the line and a write writes the current loaded value out to the line.

Note that when any reset of the digital circuitry is performed (clear chip or computer reset), all digital lines are reset to inputs and their corresponding output registers are cleared.

Read /Write operation (32bit, 8 bits are used)

B31 – B8	B7	B6	B5	B4	B3	B2	B1	B0

B7-B0: P0.7- P0.0
B31-B8 Reserved

074h: Digital I/O chip Port 1, Bit Programmable Port (Read/Write)

This port transfers the 8-bit Port 1 digital input or digital output byte between the board and an external device. When Port 1 is set as inputs, a read reads the input values and a write is ignored. When Port 1 is set as outputs, a read reads the last value sent out of the port and a write writes the current loaded value out of the port.

Note that when any reset of the digital circuitry is performed (clear chip or computer reset), all digital lines are reset to inputs and their corresponding output registers are cleared.

Read /Write operation (32bit, 8 bits are used)

B31 – B8	B7	B6	B5	B4	B3	B2	B1	B0

B7-B0: P1.7- P1.0
B31-B8 Reserved

078h: Read/Program Port 0 Direction/Mask/Compare Registers (Read/Write)

A read clears the IRQ status flag or provides the contents of one of digital I/O Port 0's three control registers; and a write clears the digital chip or programs one of the three control registers, depending on the setting of bits 0 and 1 at LAS0 + 07Ch. When bits 1 and 0 at LAS0 + 07Ch are 00, the read/write operations clear the digital IRQ status flag (read) and the digital chip (write). When these bits are set to any other value, one of the three Port 0 registers is addressed.

Direction Register (LAS0 + 07Ch, bits 1 and 0 = 01):
This register programs the direction, of each bit at Port 0, when 0x7C = xxxxxx01 binary.

B31 – B8	B7	B6	B5	B4	B3	B2	B1	B0

B7-B0: 0 Input; 1 Output
B31-B8 Reserved

Mask Register (LAS0 +07Ch, bits 1 and 0 = 10):
This register programs the mask, of each bit at Port 0, when 0x7C =xxxxxx10 binary.

B31 – B8	B7	B6	B5	B4	B3	B2	B1	B0

B7-B0: 0 Bit enabled; 1 Masked
B31-B8 Reserved

In the Advanced Digital Interrupt modes, this register is used to mask out specific bits when monitoring the bit pattern present at Port 0 for interrupt generation. In normal operation where the Advanced Digital Interrupt feature is not being used, any bit which is masked by writing a 1 to that bit will not change state, regardless of the digital data written to Port 0. For example, if you set the state of bit 0 low and then mask this bit, the state will remain low, regardless of what you output at Port 0 (an output of 1 will not change the bit's state until the bit is unmasked).

Compare Register (LAS0 + 07Ch, bits 1 and 0 = 11):
This register is used for the Advanced Digital Interrupt modes. In the match mode where an interrupt is generated when the Port 0 bits match a loaded value, this register is used to load the bit pattern to be matched at Port 0. Bits can be selectively masked so that they are ignored when making a match. NOTE: Make sure that bit 3 at LAS0 + 07Ch is set to 1, selecting match mode, BEFORE writing the Compare Register value at this address. In the event mode where an interrupt is generated when any Port 0 bit changes its current state, the value which caused the interrupt is latched at this register and can be read from it. Bits can be selectively masked using the Mask Register so a change of state is ignored on these lines in the event mode.

07Ch: Read Digital IRQ Status/Program Digital Mode (Read/Write)

Digital IRQ/Strobe Status (Read 32bit, 8 bits are used):
A read shows you whether a digital interrupt has occurred (bit 6), whether a strobe has occurred (bit 7, when using the strobe input as described in Chapter 7), and lets you review the states of bits 0 through 5 in this register. If bit 6 is high, then a digital interrupt has taken place. If bit 7 is high, a strobe has been issued.

B31 – B8	B7	B6	B5	B4	B3	B2	B1	B0

B1-B0: Port 0 Control Register Select (see register 078h)
00 Clear Digital IRQ Status Flag (read); Reset Digital I/O (write)
01 P0 direction register
10 P0 mask register
11 P0 compare register
B2 0 P1 direction Input; 1 Output
B3 0 Digital IRQ Event Mode; 1 Match Mode
B4 0 Digital IRQ Disabled; 1 Enabled
B5 Digital Sample Clock Select
0 8MHz clock
1 Programmable clock
B6 0 No digital interrupt 1 Digital interrupt (READ only)
B7 0 No strobe 1 Strobe (READ only)
B31-B8 Reserved

0B0h: Command Register (Read/Write) SDM35540 ONLY

Read operation (32bit, upper word/ lower byte not used):
This register is written to by the DSP after it has run the command routine. The host is responsible for reading this register to see what error code if any has been generated.

B31-B16								
B15	B14	B13	B12	B11	B10	B9	B8	B7-B0

B31-B16: Reserved
B15-B8: 0 Command successful; 1 No Auto-Calibration in Flash
B7- B0: Reserved

Write operation (32bit, upper 3 bytes not used):
This register is written to by the host to perform a variety of board functions. A non-maskable interrupt is generated to the DSP which in turn reads the register and performs the function.

B31-B16								
B15 – B8	B7	B6	B5	B4	B3	B2	B1	B0

B31-B16: Reserved
B15-B8: Reserved
B7- B0:

0x01	Auto-Calibrate
0x02	Internal Flash Download
0x03	Reserved
0x04	Reserved
0x05	Erase Internal Flash
0x06	Reserved
0x07	Attention DSP (is DSP alive)
0x08	Load Factory Default calibration values
0x09	Reserved
0x0A	Get Auto-Calibration Code Version
0x0B	Get Boot loader Code Version

0E0h: Analog Connector DIO Mask (Read/Write) SDM35540 ONLY

Read /Write operation (32bit, 6 bits are used)
Sets the mask for interrupts on the input and digital outputs. Default is all bits masked.

B31 – B6	B5	B4	B3	B2	B1	B0

B0:	0 Data output pin 1 of CN9 is masked;	1 Data output pin 1 of CN9is unmasked
B1:	0 Data output pin 2 of CN9 is masked;	1 Data output pin 2 of CN9is unmasked
B2:	0 Positive edge interrupt pin 1 of CN9 is masked;	1 Positive edge interrupt pin 1 of CN9 is unmasked
B3:	0 Positive edge interrupt pin 2 of CN9 is masked;	1 Positive edge interrupt pin 2 of CN9 is unmasked
B4:	0 Negative edge interrupt pin 1 of CN9 is masked;	1 Negative edge interrupt pin 1 of CN9 is unmasked
B5:	0 Negative edge interrupt pin 2 of CN9 is masked;	1 Negative edge interrupt pin 2 of CN9 is unmasked
B31-B6	Reserved	

0E4h: Analog Connector DIO Data (Read/Write) SDM35540 ONLY

Read /Write operation (32bit, 2 bits are used)
The written data is the value seen before the output buffer (i.e. if user does not turn direction bit to output this written value does not necessarily reflect what you wrote when you perform a read) The read data is direct from the pin on CN9.

B31 – B2	B1	B0

B0: Data value pin 1 CN9
B1: Data value pin 2 CN9
B31-B2 Reserved

0E8h: Analog Connector DIO Direction (Read/Write) SDM35540 ONLY

Read /Write operation (32bit, 2 bits are used)
Represents the direction of the DIO pins on CN9. Default is input.

B31 – B2	B1	B0

B0: 0 Input pin 1 CN9 1 Output pin 1 CN9
B1: 0 Input pin 2 CN9 1 Output pin 2 CN9
B31-B2 Reserved

0E8h: Analog Connector DIO Interrupt Status (Read Only) SDM35540 ONLY

Read operation (32bit, 4 bits are used)
A read from this register will give the unmasked interrupt status on pins designated as inputs. The read also clears the register. A read from this register will give interrupt status (masked or unmasked) on pins designated as inputs. The interrupts listed below are combined to generate an interrupt on the local bus along with the interrupts listed in register LAS0 offset 0x30.

B31 – B6	B5	B4	B3	B2	B1-B0

B1–B0: Reserved
B2: 0 Positive edge interrupt pin 1 of CN9 inactive; 1 Positive edge interrupt pin 1 of CN9 is active
B3: 0 Positive edge interrupt pin 2 of CN9 is inactive; 1 Positive edge interrupt pin 2 of CN9 is active
B4: 0 Negative edge interrupt pin 1 of CN9 is inactive; 1 Negative edge interrupt pin 1 of CN9 is active
B5: 0 Negative edge interrupt pin 2 of CN9 is inactive; 1 Negative edge interrupt pin 2 of CN9 is active
B31-B6 Reserved

5.4.1 LOCAL ADDRESS SPACE 0 (LAS0) – RUNTIME AREA

The LAS0 Setup Area (LAS0 + 100 to 1FF) is used to program the operating modes DM35520 Board. The functionality of this area is the same as the Function Select / Argument of older PCI4400 board. The following tables show the programming possibilities of the DAQ board.

After power up the registers DM35520 is in initial state. This initial state can be reached also by Software Reset. The initial state is signed by☜.

Table 19 shows the LAS0 Setup area. Function Codes are the PCI4400 style Function Code Function select Code information.

Table 19: LAS0 Setup Area

Function Group	Function Name	LAS0 Offset Address / Function code (hex)	Function argument
Board Control	Software Rest of the Board	100h 0X000F	-
Demand Mode DMA Control	DMA0 Request source Select	104h 0x0100	0x00 = Request disable 0x01 = A/D Sample Counter 0x02 = D/A1 Sample Counter 0x03 = D/A2 Sample Counter 0x04 = User TC 1 0x08 = A/D FIFO half full 0x09 = D/A1 FIFO half Empty 0x0A = D/A2 FIFO half Empty
	DMA1 Request source Select	108h 0x0101	0x00 = Request disable 0x01 = A/D Sample Counter 0x02 = D/A1 Sample Counter

Function Group	Function Name	LAS0 Offset Address / Function code (hex)	Function argument
			0x03 = D/A2 Sample Counter 0x04 = User TC 1 0x08 = A/D FIFO half full 0x09 = D/A1 FIFO half Empty 0x0A = D/A2 FIFO half Empty
	Reset DMA0 Request Machine	1CCh 0x0710	-
	Reset DMA1 Request Machine	1D0h 0x0711	-
A/D Conversion and High Speed Digital Input Control	A/D Conversion Signal Select	10Ch 0x0200	0x0 = Software A/D Start (WR_LAS0 + 010h) 0x1 = Pacer Clock 0x2 = Burst Clock 0x3 = Digital Interrupt 0x4 = D/A 1 Data Marker 1 0x5 = D/A 2 Data Marker 11 0x6 = SyncBus 0 0x7 = SyncBus 1 0x8 = SyncBus 2
	Burst Clock start trigger select	110h 0x0201	0x0 = Software A/D Start (WR_LAS0 + 010h) 0x1 = Pacer Clock 0x2 = External Trigger 0x3 = Digital Interrupt 0x4 = SyncBus 0 0x5 = SyncBus 1 0x6 = SyncBus 2
	Pacer Clock start trigger select	114h 0x0202	0x0 = Software Pacer Start (RD_LAS0 + 028h) 0x1 = External trigger 0x2 = Digital interrupt 0x3 = User TC 2 out 0x4 = SyncBus 0 0x5 = SyncBus 1 0x6 = SyncBus 2 0x7 = Reserved 0x8 = Delayed Software Pacer Start 0x9 = Delayed external trigger 0xA = Delayed digital interrupt 0xB = Delayed User TC 2 out 0xC = Delayed SyncBus 0 0xD = Delayed SyncBus 1 0xE = Delayed SyncBus 2 0xF = External Trigger Gated controlled mode
A/D Conversion and High Speed Digital Input Control	Pacer Clock Stop Trigger select	118h 0x0203	0x0 = Software Pacer Stop (WR_LAS0 + 028h) 0x1 = External Trigger 0x2 = Digital Interrupt 0x3 = About Counter 0x4 = User TC2 out 0x5 = SyncBus 0 0x6 = SyncBus 1 0x7 = SyncBus 2 0x8 = About Software Pacer Stop 0x9 = About External Trigger 0xA = About Digital Interrupt 0xB = Reserved 0xC = About User TC2 out 0xD = About SyncBus 0 0xE = About SyncBus 1 0xF = About SyncBus 2

Function Group	Function Name	LAS0 Offset Address / Function code (hex)	Function argument
	About Counter Stop Enable	11Ch 0x0204	0 = Stop enabled 1 = Stop disabled
	Pacer Start Trigger Mode select	120h 0x0205	0x0 = Single Cycle Mode - new cycle can be possible after a Software Pacer Start command 0x1 = Trigger Repeat Mode - Pacer can be started by the selected Pacer Start Trigger
	Sampling Signal for High Speed Digital Input Select	124h 0x0206	0x0 = Software (Write LAS0 + 02Ch) 0x1 = A/D Conversion Signal 0x2 = User TC out 0x3 = User TC out 1 0x4 = User TC out 2 0x5 = External Pacer Clock 0x6 = External Trigger
	Clear High Speed Digital Input FIFO	128h 0x020E	-
	Clear A/D FIFO	12Ch 0x020F	-
Channel Gain / Digital Table Control	Write Channel Gain Table (Multi-channel mode)	130h 0x0300	see 130h: Write ADC channel gain table (Write Only)
	Write Channel Gain Latch (Single-channel mode)	134h 0x0301	see 134h: Write ADC channel gain latch (Write Only)
	Write Digital Table (To control external MUX)	138h 0x0302	see 138h: Write Digital table (Write Only)
	Enable Channel Gain Table	13Ch 0x0303	0x0 = Channel Gain Table disabled Channel Gain Latch enabled 0x1 = Channel Gain Table enabled Channel Gain Latch disabled
	Enable Digital Table	140h 0x0304	0x0 = Digital Table disabled Digital I/O P1 port enabled 0x1 = Digital Table enabled Digital I/O P1 port disabled
	Table Pause enable	144h 0x0305	0x0 = Table Pause disabled 0x1 = Table Pause enabled
	Reset Channel Gain Table	148h 0x030E	-
	Clear Channel Gain Table	14Ch 0x030F	-
D/A 1 Control	D/A1 output type / range	150h 0x0400	0x0 = unipolar 0..5V 0x1 = unipolar 0.. 10V 0x2 = bipolar ±5V 0x3 = bipolar ±10V
	D/A1 update source	154h 0x0401	0x0 = Software D/A1 Update 0x1 = CGT controlled D/A1 Update 0x2 = D/A Clock 0x3 = External pacer clock 0x4 = SyncBus 0 0x5 = SyncBus 1 0x6 = SyncBus 2
	D/A1 Cycle Mode	158h 0x0402	0x0 = not cycle 0x1 = cycle
	Reset D/A1 FIFO	15Ch 0x0406	-
	Clear D/A1 FIFO	160h 0x0407	-
D/A 2 Control	D/A2 output type / range	164h 0x0408	0x0 = unipolar 0..5V 0x1 = unipolar 0.. 10V 0x2 = bipolar ±5V 0x3 = bipolar ±10V
	D/A2 update source	168h	0x0 = Software D/A2 Update

Function Group	Function Name	LAS0 Offset Address / Function code (hex)	Function argument
		0x0409	0x1 = CGT controlled D/A2 Update 0x2 = D/A Clock 0x3 = External Pacer Clock 0x4 = SyncBus 0 0x5 = SyncBus 1 0x6 = SyncBus 2
	D/A2 Cycle Mode	16Ch 0x040A	0x0 = not cycle 0x1 = cycle
	Reset D/A2 FIFO	170h 0x040E	-
	Clear D/A2 FIFO	174h 0x040F	-
D/A Clock control	D/A clock start select	1D4h 0x0410	0x0 = Software Pacer Start (RD_LAS0 + 028h) 0x1 = External trigger 0x2 = Digital interrupt 0x3 = User TC 2 out 0x4 = SyncBus 0 0x5 = SyncBus 1 0x6 = SyncBus 2 0x7 = Software D/A clock start (RD_LAS0 + 00Ch)
	D/A clock stop select	1D8h 0x0411	0x0 = Software Pacer Stop (WR_LAS0 + 028h) 0x1 = External Trigger 0x2 = Digital Interrupt 0x3 = User TC2 out 0x4 = SyncBus 0 0x5 = SyncBus 1 0x6 = SyncBus 2 0x7 = Software D/A clock stop (WR_LAS0 + 00Ch) 0x8 = D/A1 update counter 0x9 = D/A2 update counter
	D/A clock free-run or start–stop mode select	1E8h 0x0412	0x0 = D/A clock is running free 0x1 = D/A clock started or stopped by functions 0x0410 or 0x0411
Timer/Counter Control	A/D Sample Counter Source Select	178h 0x0500	0x0 = Reset Channel Gain Table 0x1 = A/D FIFO write
	Pacer Clock Primary frequency Select	1DCh 0x0501	0x0 = 8MHz 0x1 = 20MHz
	Burst Clock Primary frequency Select	1E0h 0x0502	0x0 = 8MHz 0x1 = 20MHz
	DAC Clock Primary frequency Select	1E4h 0x0503	0x0 = 8MHz 0x1 = 20MHz
	Pacer Clock Select	180h 0x0509	0x0 = External Pacer Clock 0x1 = Internal Pacer Clock
SyncBus Setup	SyncBus 0 Source Select	184h 0x0510	0x0 = Software A/D Start (WR_LAS0 + 010h) 0x1 = Pacer Clock 0x2 = Burst Clock 0x3 = Digital Interrupt 0x4 = External Trigger 0x5 = Software Simultaneous D/A1 and D/A2 Update 0x6 = D/A Clock 0x7 = User TC2 out
	Enable SyncBus 0	188h 0x0511	0x0 = disable 0x1 = enable
	SyncBus 1 Source Select	18Ch 0x0512	0x0 = Software A/D Start (WR_LAS0+ 010h) 0x1 = Pacer Clock

Function Group	Function Name	LAS0 Offset Address / Function code (hex)	Function argument
			0x2 = Burst Clock 0x3 = Digital Interrupt 0x4 = External Trigger 0x5 = Software Simultaneous D/A1 and D/A2 Update 0x6 = D/A Clock 0x7 = User TC2 out
	Enable SyncBus 1	190h 0x0513	0x0 = disable 0x1 = enable
	SyncBus 2 Select	198h 0x0518	0x0 = Software A/D Start (WR_LAS0+ 010h) 0x1 = Software Pacer Start 0x2 = Software Pacer Stop 0x3 = Software D/A1 Update 0x4 = Software D/A2 Update 0x5 = External Pacer Clock 0x6 = External Trigger 0x7 = User TC2 out
	Enable SyncBus 2	19Ch 0x0519	0x0 = disable 0x1 = enable
External Trigger and External Interrupt Configuration	External Trigger polarity select	1A4h 0x0601	0x0 = positive edge 0x1 = negative edge
	External Interrupt polarity select	1A8h 0x0602	0x0 = positive edge 0x1 = negative edge
User Timer/Counter Control	User Timer/Counter 0 Clock Select	1ACh 0x0700	0x0 = 8MHz 0x1 = Ext. TC Clock 1 0x2 = Ext. TC Clock 2 0x3 = Ext. Pacer Clock
	User Timer/Counter 0 Gate Select	1B0h 0x0701	0x0 = Not gated 0x1 = Gated 0x2 = Ext. TC Gate 1 0x3 = Ext. TC Gate 2
	User Timer/Counter 1 Clock Select	1B4h 0x0702	0x0 = 8MHz 0x1 = Ext. TC Clock 1 0x2 = Ext. TC Clock 2 0x3 = Ext. Pacer Clock 0x4 = User Timer/Counter 0 out 0x5 = High-Speed Digital Input Sampling signal
	User Timer/Counter 1 Gate Select	1B8h 0x0703	0x0 = Not gated 0x1 = Gated 0x2 = Ext. TC Gate 1 0x3 = Ext. TC Gate 2 0x4 = User Timer/Counter 0 out
	User Timer/Counter 2 Clock Select	1BCh 0x0704	0x0 = 8MHz 0x1 = Ext. TC Clock 1 0x2 = Ext. TC Clock 2 0x3 = Ext. Pacer Clock 0x4 = User Timer/Counter 1 out
	User Timer/Counter 2 Gate Select	1C0h 0x0705	0x0 = Not gated 0x1 = Gated 0x2 = Ext. TC Gate 1 0x3 = Ext. TC Gate 2 0x4 = User Timer/Counter 1 out
User Output Signal Control	User Output Signal 0 select	1C4h 0x070E	0x0 = A/D Conversion Signal 0x1 = D/A1 Update 0x2 = D/A2 Update 0x3 = Software Programmable by WR_LAS0 + 008h
	User Output Signal 1 select	1C8h 0x070F	0x0 = A/D Conversion Signal 0x1 = D/A1 Update 0x2 = D/A2 Update

Function Group	Function Name	LAS0 Offset Address / Function code (hex)	Function argument
			0x3 = Software Programmable by WR_LAS0 + 008h
McBSP Control	A/D FIFO data to DSP enable	1ECh 0x0800	0x0 = A/D FIFO data to DSP is disabled 0x1 = A/D FIFO data to DSP is enabled
	D/A FIFO data from DSP enable	1F0h 0x0801	0x0 = D/A1 and D/A2 FIFO data from DSP is disabled 0x1 = D/A1 and D/A2 FIFO data from DSP is enabled
FIFO Addressing Mode	FIFO addressing mode	1F4h 0x0802	0x0 = FIFO addressing mode 0x1 = 4M step FIFO addressing (planned feature)

100h: Software Reset of the board (Write Only)

Writing a dummy value to this address means a Software Reset.

Software Reset of the board resets all inside logic variables of the board, equivalently with the power-up states. (☜).

104h: DMA0 Request Source Select (Write Only)

The DMA0 Request Source Signal can be selected by writing these values to LAS0+104h:

0x00 = Request disable
0x01 = A/D Sample Counter *
0x02 = D/A1 Sample Counter *
0x03 = D/A2 Sample Counter *
0x04 = User TC 1 *
0x08 = A/D FIFO half full
0x09 = D/A1 FIFO half Empty
0x0A = D/A2 FIFO half Empty

The selected source controls the DMA request signal of the PCI9080/9056 chip (DREQ0). The signals signed by * set a request flip-flop only. These setups need the Reset DMA0 Request Machine command.

The FIFO flags control the DMA request signal directly, so they do not need the Reset command.

108h: DMA1 Request Source Select (Write Only)

The DMA1 Request Source Signal can be selected by writing these values to LAS0+108h:

0x00 = Request disable
0x01 = A/D Sample Counter*
0x02 = D/A1 Sample Counter*
0x03 = D/A2 Sample Counter*
0x04 = User TC 1*
0x08 = A/D FIFO half full
0x09 = D/A1 FIFO half Empty
0x0A = D/A2 FIFO half Empty

The selected source controls the DMA request signal of the PCI9080/9056 chip (DREQ1). The signals signed by * set a request flip-flop only. These setups need the Reset DMA1 Request Machine command.

The FIFO flags control the DMA request signal directly, so they do not need the Reset command.

1CCh: Reset DMA0 Request machine (Write Only)

The *Reset DMA0 Request machine* command resets the DMA0 Request to the PCI9080/9056 PCI interface chip. This command can be activated by writing to LAS0+1CCh a dummy value. This command has effect only in Demand Mode of the PCI9080/9056. It is needed only with DMA request sources signed by * in 104h: DMA0 Request Source Select (Write Only).

10Ch: A/D Conversion Signal Select (Write Only)

The A/D conversion Signal can be selected by writing these values to LAS0+108h:

0x0 = Software A/D Start (value unimportant)
0x1 = Pacer Clock (Ext. or Int.)
0x2 = Burst Clock
0x3 = Digital Interrupt
0x4 = D/A1 Data Marker 1
0x5 = D/A2 Data Marker 1
0x6 = SyncBus0
0x7 = SyncBus1
0x8 = SyncBus2

The A/D Conversion signal select Function is used to choose the A/D Sampling signal. The Data Markers (0x4 and 0x5) are updated simultaneously with the appropriate D/A output. The conversion is started at the rising edge of the data marker. The data marker must be held in low state until you want to start a conversion. After the conversion the appropriate data marker must be cleared.

110h: A/D Burst Clock start trigger select (Write Only)

If you want to use the burst clock as conversion signal source the start trigger must be set by writing this address. The stop trigger of the burst clock is generated automatically, because the stop signal basically is the CGT reset signal that occurs at the end of the whole CGT cycle.

0x0 = Software A/D Start (value unimportant)
0x1 = Pacer Clock
0x2 = External Trigger
0x3 = Digital Interrupt
0x4 = SyncBus 0
0x5 = SyncBus 1
0x6 = SyncBus 2

114h: Pacer Clock start trigger select (Write Only)

If you want to use the Pacer Clock you must specify the start and stop conditions. The Pacer Clock Start Trigger Function selects the start signal of the Pacer Clock:

0x0 = Software Pacer Start (a dummy read from 28h)
0x1 = External trigger
0x2 = Digital interrupt
0x3 = User TC 2 out
0x4 = SyncBus 0
0x5 = SyncBus 1
0x6 = SyncBus 2
0x7 = Reserved
0x8 = Delayed Software Pacer Start (a dummy read from 28h)
0x9 = Delayed external trigger
0xA = Delayed digital interrupt
0xB = Delayed User TC 2 out
0xC = Delayed SyncBus 0
0xD = Delayed SyncBus 1
0xE = Delayed SyncBus 2
0xF = External Trigger Gated controlled

The following start trigger sources, 0x8 through 0xF provide delayed triggering. When the start trigger is issued, the A/D Delay Counter, counts down and conversions are started when the A/D Delay Counter reaches 0. The A/D Delay Counter counts at the pacer clock rate. When using the External Trigger Gated control (0xF) the pacer clock runs as long as the External Trigger Input line is held high or low, depending on the trigger polarity. This mode does not use a stop trigger.

118h: Pacer Clock stop trigger select (Write Only)

The Pacer Clock Stop Trigger Function selects the stop signal of the Pacer Clock:

0x0 = Software Pacer Stop (a dummy write to 28h)
0x1 = External Trigger
0x2 = Digital Interrupt
0x3 = About Counter
0x4 = User TC2 out
0x5 = SyncBus 0
0x6 = SyncBus 1
0x7 = SyncBus 2
0x8 = About Software Pacer Stop (a dummy write to 28h)
0x9 = About External Trigger
0xA = About Digital Interrupt
0xB = Reserved
0xC = About User TC2 out
0xD = About SyncBus 0
0xE = About SyncBus 1
0xF = About SyncBus 2

Stop trigger sources 0x8 through 0xF provide about triggering, where data is acquired from the time the start trigger is received, and continues for a specified number of samples *after* the stop trigger is received. The number of samples taken after the stop trigger is received is set by the About Counter which counts down and is clocked by the writing signal of A/D FIFO. This method assures the desired number of samples will be sampled (count reaches 0).

11Ch: About Counter Stop Enable (Write Only)

If the Pacer Clock is the source of A/D Conversion signal and the Pacer Clock Stop comes from the About Counter counting the samples in the A/D FIFO you can extend the counting capability highest number than 10 bit defined 1024 samples. Writing this address you can enable or disable the stop function:

0 = Stop enabled
1 = Stop disabled

120h: Pacer Start Trigger Mode select (Write Only)

When set to single cycle, a trigger will initiate one conversion cycle and then stop, regardless of whether the trigger line is pulsed more than once; when set to repeat, a new cycle will start each time a trigger is received, and the current cycle has been completed. Triggers received while a cycle is in progress will be ignored. Writing this address you can select single cycle or repeat mode:

0x0 = Single Cycle Mode - new cycle can be possible after a Software Pacer Start command
0x1 = Trigger Repeat Mode - Pacer can be started by the selected Pacer Start Trigger

124h: Sampling Signal for High Speed Digital Input Select (Write Only)

The sampling signal of High-Speed Digital Input can be selected by writing this address. If you select the A/D conversion signal, the 8-bit digital input lines are simultaneously sampled with the analog signals.

0x0 = Software (dummy write 2Ch)
0x1 = A/D Conversion Signal
0x2 = User TC out
0x3 = User TC out 1
0x4 = User TC out 2
0x5 = External Pacer Clock
0x6 = External Trigger

128h: Clear High Speed Digital Input FIFO (Write Only)

Writing a dummy data to this address clears the High-Speed Digital Input FIFO.

12Ch: Clear A/D FIFO (Write Only)

Writing a dummy data to this address clears the A/D FIFO.

130h: Write ADC channel gain table (Write Only)

In the case of multi-channel operation the Channel Gain Table must be used. Before writing the channel gain table entries write a dummy data to 14Ch to clear the table. The structure of the entries in the table can be seen below:

B31 – B16															
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

B3-B0: 0x0 1st analog input channel
0x1 2nd analog input channel
….
0xF 16th analog input channel
B6-B4: 0x0 Gain 1
0x1 Gain 2
0x2 Gain 4
0x3 Gain 8
0x4 Gain 16
0x5 Gain 32
0x6 Gain 64 **(SDM35540 only)**
B7: 0 AGND referenced SE input; 1 AINSENSE referenced SE input
B9-B8: 0x0 +/-5V input range
0x1 +/-10V input range
0x2 0 – 10V input range
0x3 reserved
B10: 0 Single Ended; 1 Differential
B11: 0 Pause bit disabled; 1 Enabled
B12: 0 D/A1 update disabled; 1 Enabled
B13: 0 D/A2 update disabled; 1 Enabled
B14: Skip bit disabled; 1 Enabled
B15: Reserved
B31-B16 Reserved

Using the pause bit: The pause bit of the channel-gain word is set to 1 if you want to stop at an entry in the table and wait for the next trigger to resume conversions. In burst mode, the pause bit is ignored.
Using the skip bit: The skip bit of the channel-gain word is set to 1 if you want to skip an entry in the table. This feature allows you to sample multiple channels at different rates on each channel. For example, if you want to sample channel 1 once each second and channel 4 once every 3 seconds, you can set the skip bit on channel 4. With the skip bit set on the four table entries; these entries will be ignored, and no A/D conversion will be performed. This saves memory and eliminates the need to throw away unwanted data.

134h: Write ADC channel gain latch (Write Only)

In the case of single-channel operation the Channel Gain Latch must be used. The data structure is the same as in the Channel Gain Table but there are no meaning of the skip bit, D/Ax Update and the Pause Bit. These bits must be zero.

138h: Write Digital table (Write Only)

The Digital Table is part of the Channel Gain Table, and can be used to control external devices. Using this function you can fill the 8bit wide Digital Table. Reading of the Digital Table is simultaneous with reading the Channel Gain Table.

B31 – B8	B7 – B0

Read /Write operation (32bit, 16 bits are used)
B7-B0: P1.7-P1.0 Eight bit Digital output table bits
B31-B8 Reserved

The Digital Output Table bits use the same lines as the Digital I/O Chip Port 1 I/O port. In the case of usage the P1 digital I/O lines the Digital Table bits cannot be used. The Enable Digital Table Function (0x0304) can be used to select between the Digital I/O P1 port and the Digital Output Table bits. The digital portion of the channel-gain table provides 8 bits to control devices such as external expansion boards. For example, if you have connected one of your input channels on the DM35520 to RTD's TMX32 input expansion board, you can use the bottom 5 bits in this byte to control the TMX32 board channel selection. To load digital information into this portion of the channel, use this function. This information will be output on the Port 1 lines when you run through the table. The format shown above is for controlling the TMX32's channel selection (32 single-ended or 16 differential). The first load operation will be in the first entry slot of the table (lining up with the first entry in the

A/D table), and each load thereafter fills the next position in the channel-gain table. Note that when you are using the digital table, all 8 bits are used and controlled by the table, regardless of the number of bits you may actually need for your digital control application.

13Ch: Enable Channel Gain Table (Write Only)

Writing to this address you can select the Channel Gain Latch or the Channel Gain Table controlled operation.

0x0 = CGT disabled; Channel Gain Latch enabled
0x1 = CGT enabled Channel Gain Latch disabled

140h: Enable Digital Table (Write Only)

Writing to this address you can select the P1 port of Digital I/O chip or the output of the Digital Table on the pin 32, 46 of External I/O connector.

0x0 = Digital Table disabled; Digital I/O P1 port enabled
0x1 = Digital Table enabled; Digital I/O P1 port disabled

144h: Table Pause enable (Write Only)

The pause bit of the Channel Gain Table is set to 1 if you want to stop at an entry in the table and wait for the next trigger to resume conversions. In burst mode, the pause bit is ignored. Writing this address this mode can be enabled:

0x0 = Table Pause enabled
0x1 = Table Pause disabled

148h: Reset Channel Gain Table (Write Only)

Writing a dummy data to this address sets the read pointer of the Channel Gain Table to the beginning of the Table. The write pointer of the Table does not change.

14Ch: Clear Channel Gain Table (Write Only)

Writing a dummy data to this address sets the read ***and*** the write pointer of the Channel Gain Table to the beginning of the Table. This function is used to configure the D/A output channels, DAC1 and DAC2, on the DM35520 as follows:

150h: D/A 1 output type/range (Write Only)

Writing this address sets the voltage output range and polarity for DAC1:

0x0 = 0 – 5V range
0x1 = 0 – 10V range
0x2 = ±5V range
0x3 = ±10V range

154h: D/A 1 update source (Write Only)

Writing this address selects the update source for D/A1.

0x0 = Software D/A1 Update (a dummy write to 14h)
0x1 = CGT controlled D/A1 Update
0x2 = D/A Clock (source is output of D/A clock counter)
0x3 = External pacer clock
0x4 = SyncBus 0
0x5 = SyncBus 1
0x6 = SyncBus 2

The CGT Controlled Update assures simultaneous D/A update with the A/D conversion

158h: D/A 1 Cycle Mode (Write Only)

This bit enables the cycle mode for D/A1 converter. By writing 0x01, D/A1 will continuously repeat the data that is stored in the D/A1 FIFO. This is useful for waveform generation.

0x0 = not cycle
0x1 = cycle

15Ch: Reset D/A 1 Cycle FIFO (Write Only)

Writing a dummy data to this address sets the read pointer of the D/A1 FIFO to the beginning of the FIFO. The write pointer of the FIFO does not change.

160h: Clear D/A 1 Cycle FIFO (Write Only)

Writing a dummy data to this address sets the read ***and*** the write pointer of the D/A1 FIFO to the beginning of the FIFO.

164h: D/A 2 output type/range (Write Only)

Writing this address sets the voltage output range and polarity for DAC1:

0x0 = 0 – 5V range
0x1 = 0 – 10V range
0x2 = ±5V range
0x3 = ±10V range

168h: D/A 2 update source (Write Only)

Writing this address selects the update source for D/A2.

0x0 = Software D/A1 Update (a dummy write to 18h)
0x1 = CGT controlled D/A1 Update
0x2 = D/A Clock (source is output of D/A clock counter)
0x3 = External pacer clock
0x4 = SyncBus 0
0x5 = SyncBus 1
0x6 = SyncBus 2

The CGT Controlled Update assures simultaneous D/A update with the A/D conversion.

16Ch: D/A 2 Cycle Mode (Write Only)

This bits enables the cycle mode for D/A2 converter. By writing 0x01, D/A2 will continuously repeat the data that is stored in the D/A 2 FIFO. This is useful for waveform generation.

0x0 = not cycle
0x1 = cycle

170h: Reset D/A 2 FIFO (Write Only)

Writing a dummy data to this address sets the read pointer of the D/A2 FIFO to the beginning of the FIFO. The write pointer of the FIFO does not change.

174h: Clear D/A 2 FIFO (Write Only)

Writing a dummy data to this address sets the read ***and*** the write pointer of the D/A2 FIFO to the beginning of the FIFO.

178h: A/D Sample Counter Source Select (Write Only)

Writing this address the A/D Sample Counter Clock can be selected:

0x0 = Reset Channel Gain Table
0x1 = A/D FIFO write

If you want to count all of the sampled analog data select the A/D FIFO write argument. If you want to count the CGT periods select the Reset Channel Gain Table argument.

180h: Pacer Select (Write Only)

Selects the internal Pacer Clock, which is the output of internal Pacer Clock generator or an external Pacer Clock routed onto the board through External I/O connector:

0x0 = External Pacer Clock
0x1 = Internal Pacer Clock

The maximum Pacer Clock rate supported by the board is 1.25 MHz.

184h: SyncBus 0 Source Select (Write Only)

This function selects the source of the SyncBus 0 signal:

0x0 = Software A/D Start
0x1 = Pacer Clock
0x2 = Burst Clock
0x3 = Digital Interrupt
0x4 = External Trigger
0x5 = Software Simultaneous D/A1 and D/A2 Update
0x6 = D/A Clock
0x7 = User TC2 out

The SyncBus is a 3-line synchronization purpose bus to synchronize the operation of multiple DM35520 or other RTD DAQ Boards. The source of signals can be the same and can be on the other DM35520 boards.

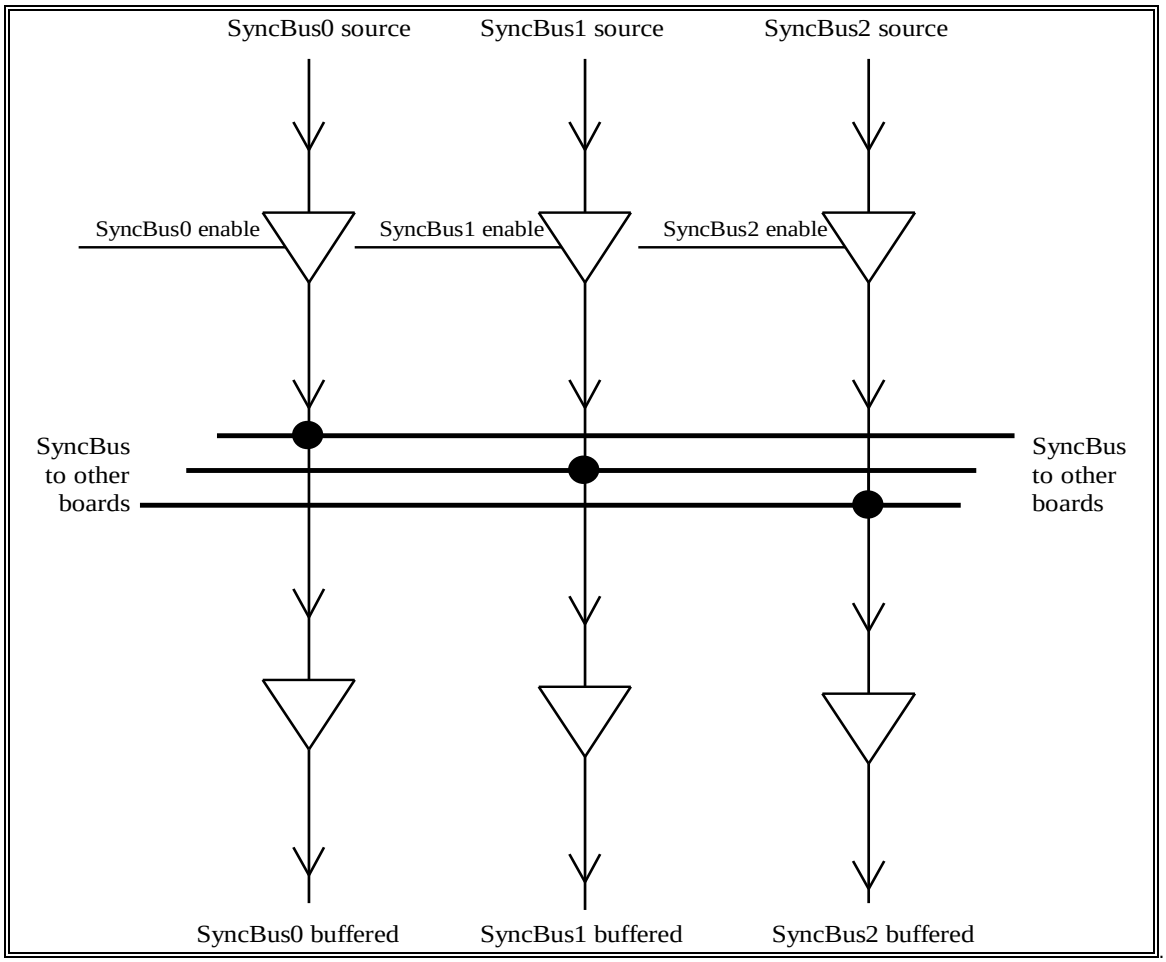
188h: Enable SyncBus 0 (Write Only)

This function enables the SyncBus 0 buffer

0x0 = disable
0x1 = enable

NOTE: When connecting SyncBus signals together ensure that each signal has only one driver.

Figure 15: SyncBus Structure



18Ch: SyncBus 1 Source Select (Write Only)

This function selects the source of the SyncBus 1 signal:

0x0 = Software A/D Start
0x1 = Pacer Clock
0x2 = Burst Clock
0x3 = Digital Interrupt
0x4 = External Trigger
0x5 = Software Simultaneous D/A1 and D/A2 Update
0x6 = D/A Clock
0x7 = User TC2 out

The SyncBus is a 3-line synchronization purpose bus to synchronize the operation of multiple DM35520 or other RTD DAQ Boards. The source of signals can be the same and can be on the other DM35520 boards.

190h: Enable SyncBus 1 (Write Only)

This function enables the SyncBus 1 buffer

0x0 = disable
0x1 = enable

NOTE: When connecting SyncBus signals together ensure that each signal has only one driver.

198h: SyncBus 2 Source Select (Write Only)

This function selects the source of the SyncBus 2 signal:

0x0 = Software A/D Start
0x1 = Pacer Clock
0x2 = Burst Clock
0x3 = Digital Interrupt
0x4 = External Trigger
0x5 = Software Simultaneous D/A1 and D/A2 Update
0x6 = D/A Clock
0x7 = User TC2 out

The SyncBus is a 3-line synchronization purpose bus to synchronize the operation of multiply DM35520 or other RTD DAQ Boards. The source of signals can be the same and can be on the other DM35520 boards.

19Ch: Enable SyncBus 2 (Write Only)

This function enables the SyncBus 1 buffer

0x0 = disable
0x1 = enable

NOTE: When connecting SyncBus signals together ensure that each signal has only one driver.

1A4h: External Trigger Polarity Select (Write Only)

This function selects the active polarity of External Trigger signal from the I/O connector

0x0 = positive edge
0x1 = negative edge

1A8h: External Interrupt Polarity Select (Write Only)

This function selects the active polarity of the External Interrupt signal:

0x0 = positive edge
0x1 = negative edge

The External Interrupt signal comes from the External I/O connector. The External Interrupt may be a source of built-in priority Interrupt Controller.

The following section shows the *User TC Configuration Function Group.* The User TC is a 8254 chip with three timer, which can be used by the user. The clock gate sources can be programmed by this Function Group.

1ACh: User Timer/Counter 0 Clock Select (Write Only)

This function selects the source of the User TC 0 clock signal:

0x0 = 8MHz
0x1 = Ext. TC Clock 1
0x2 = Ext. TC Clock 2
0x3 = Ext. Pacer Clock

1B0h: User Timer/Counter 0 Gate Select (Write Only)

This function selects the source of the User TC 0 gate signal:

0x0 = Not gated (free running)
0x1 = Gated (logic high or low)
0x2 = Ext. TC Gate 1
0x3 = Ext. TC Gate 2

1B4h: User Timer/Counter 1 Clock Select (Write Only)

This function selects the source of the User TC 1 clock signal:

0x0 = 8MHz
0x1 = Ext. TC Clock 1
0x2 = Ext. TC Clock 2
0x3 = Ext. Pacer Clock
0x4 = User Timer/Counter 0 out
0x5 = High-Speed Digital Input Sampling signal

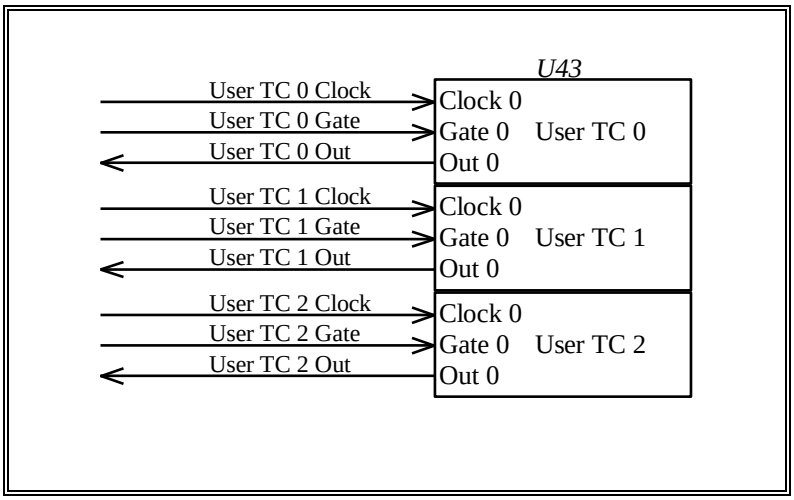
You can cascade timer TC 1 using 0x4. You can use User TC 1 as a Sample Counter for the High Speed Digital Input FIFO.

1B8h: User Timer/Counter 1 Gate Select (Write Only)

This function selects the source of the User TC 1 gate signal:

0x0 = Not gated (free running)
0x1 = Gated (logic high or low)
0x2 = Ext. TC Gate 1
0x3 = Ext. TC Gate 2
0x4 = User Timer/Counter 0 out

Figure 16: User TC Section



1BCh: User Timer/Counter 2 Clock Select (Write Only)

This function selects the source of the User TC 2 clock signal:

0x0 = 8MHz
0x1 = Ext. TC Clock 1
0x2 = Ext. TC Clock 2
0x3 = Ext. Pacer Clock
0x4 = User Timer/Counter 1 out

You can cascade timer TC 1 using 0x4.

1C0h: User Timer/Counter 2 Gate Select (Write Only)

This function selects the source of the User TC 2 gate signal:

0x0 = Not gated (free running)
0x1 = Gated (logic high or low)
0x2 = Ext. TC Gate 1
0x3 = Ext. TC Gate 2
0x4 = User Timer/Counter 1 out

1C4h: User Output 0 Signal Select (Write Only)

The selected sources are buffered and connected to the External I/O connector. The source of the *User Out 0* can be programmed using this function:

0x0 = A/D Conversion Signal
0x1 = D/A1 Update
0x2 = D/A2 Update
0x3 = Software Programmable (see register 8h)

1C8h: User Output 1 Signal Select (Write Only)

The selected sources are buffered and connected to the External I/O connector. The source of the *User Out 1* can be programmed using this function:

0x0 = A/D Conversion Signal
0x1 = D/A1 Update
0x2 = D/A2 Update
0x3 = Software Programmable (see register 8h)

1ECh: McBSP A/D FIFO Control (Write Only)

This Function enables the automatic sending of the A/D FIFO data to the connected DSP via the McBSP serial connection:

0x0 = A/D FIFO data to DSP is disabled
0x1 = A/D FIFO data to DSP is enabled

This means that this data cannot be read by the host (or other PCI master) via the PCI bus.

1F0h: McBSP D/A 1 and D/A 2 FIFO Control (Write Only)

This Function enables a connected DSP to write to the D/A1 and D/A2 FIFO via the McBSP serial connection:

0x0 = D/A1 and D/A2 FIFO data from DSP is disabled
0x1 = D/A1 and D/A2 FIFO data from DSP is enabled

5.4.2 LOCAL ADDRESS SPACE 1 (LAS1) - SETUP AREA

This is a 16bit wide memory mapped address space. Traditional boards use this space for DMA purposes. It can be accessed by word wide (16 bit) single cycle, or double word-wide (32bit) DMA controlled Burst mode read/write instructions. The range size is 16 byte.

This address space is used to transfer data from A/D input FIFO, High Speed Digital Input FIFO, and to the D/A output FIFOs.

You can use 16 bit wide (word) or 32 bit wide (Lword) direct slave read/write instructions. In the case of Lword instruction two word long burst cycle is generated by the CPU. If you use the onboard DMA controller you can use long burst cycles that assures fast data transfer between the board and the CPU.

Table 20: LAS1 Address Space

LAS1 Function		LAS1 Offset 16-bit		Local Base Address
Read Function	Write Function	Host	DSP	Host
Read A/D FIFO	-	0h		4000:0000h
Read High-Speed Digital Input FIFO	-	4h – 0x802 Function Set to 0		
-	Write D/A 1 FIFO	8h – 0x802 Function Set to 0		
-	Write D/A 2 FIFO	Ch – 0x802 Function Set to 0		

000h: Read A/D FIFO (Read Only)

A read provides the 12-bit A/D converted data as shown below. Bit 15 is the sign bit extension. This sign bit extension gives the opportunity to read the converted data as two's complement number in either unipolar or bipolar mode. The bottom three bits are the samples of the buffered version of the External I/O connector Port 0 Digital I/O port P0-5, P0-6, P0-7 lines which can be used as independent Data Markers. The sampling is simultaneous with this read instruction.

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

B0: P0-5
B1: P0-6
B2: P0-7
B3: A/D bit 1
B4: A/D bit 2
B5: A/D bit 3
B6: A/D bit 4
B7: A/D bit 5
B8: A/D bit 6
B9: A/D bit 7
B10: A/D bit 8
B11: A/D bit 9
B12: A/D bit 10
B13: A/D bit 11
B14: A/D bit 12
B15: Sign bit

004h: Read High Speed Digital Input FIFO (Read Only)

A read provides the 8-bit High Speed Digital Input Data bits which are programmable source sampled. The High Speed Digital Input lines are commonly used with the Digital I/O, bit programmable P0 port and can be used as independent Data Markers. The upper byte is undefined.

B15-B8	B7	B6	B5	B4	B3	B2	B1	B0

B0: P0-0
B1: P0-1
B2: P0-2
B3: P0-3
B4: P0-4
B5: P0-5
B6: P0-6
B7: P0-7
B15-B8: Undefined

008h: Write D/A1 FIFO (Read Only)

A write programs the D/A1 FIFO in the format shown below, as two's complement data. A write also sets the D/A1 data markers. The buffered version of D/A1 data marker 0 is connected to the I/O connector. It can be used as a source for the A/D Sample signal. This register can also be written to via the McBSP connection. In this mode the D/A selection bit (bit 2) controls the data direction to the D/A1 or D/A2 FIFO.

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

B0: D/A1 digital Output Data Marker 0
B1: D/A1 digital Output Data Marker 1
B2: 0 D/A1 receives McBSP Data; 1 D/A2 receives McBSP Data (McBSP mode only)
B3: D/A1 bit 1 (unless using McBSP, then see bit 2)
B4: D/A1 bit 2 (unless using McBSP, then see bit 2)
B5: D/A1 bit 3 (unless using McBSP, then see bit 2)
B6: D/A1 bit 4 (unless using McBSP, then see bit 2)
B7: D/A1 bit 5 (unless using McBSP, then see bit 2)
B8: D/A1 bit 6 (unless using McBSP, then see bit 2)
B9: D/A1 bit 7 (unless using McBSP, then see bit 2)
B10: D/A1 bit 8 (unless using McBSP, then see bit 2)
B11: D/A1 bit 9 (unless using McBSP, then see bit 2)
B12: D/A1 bit 10 (unless using McBSP, then see bit 2)
B13: D/A1 bit 11 (unless using McBSP, then see bit 2)
B14: D/A1 bit 12 (unless using McBSP, then see bit 2)
B15: D/A1 sign bit

00Ch: Write D/A21 FIFO (Read Only)

A write programs the D/A2 FIFO in the format shown below, as two's complement data. A write also sets the D/A2 data markers. The buffered version of D/A2 data marker 0 is connected to the I/O connector. It can be used as a source for the A/D Sample signal. This register can also be written to via the McBSP connection. In this mode the D/A selection bit (bit 2) controls the data direction to the D/A1 or D/A2 FIFO.

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

B0: D/A2 digital Output Data Marker 0
B1: D/A2 digital Output Data Marker 1
B2: 0 D/A1 receives McBSP Data; 1 D/A2 receives McBSP Data (McBSP mode only)
B3: D/A2 bit 1 (unless using McBSP, then see bit 2)
B4: D/A2 bit 2 (unless using McBSP, then see bit 2)
B5: D/A2 bit 3 (unless using McBSP, then see bit 2)
B6: D/A2 bit 4 (unless using McBSP, then see bit 2)
B7: D/A2 bit 5 (unless using McBSP, then see bit 2)
B8: D/A2 bit 6 (unless using McBSP, then see bit 2)
B9: D/A2 bit 7 (unless using McBSP, then see bit 2)
B10: D/A2 bit 8 (unless using McBSP, then see bit 2)
B11: D/A2 bit 9 (unless using McBSP, then see bit 2)
B12: D/A2 bit 10 (unless using McBSP, then see bit 2)
B13: D/A2 bit 11 (unless using McBSP, then see bit 2)
B14: D/A2 bit 12 (unless using McBSP, then see bit 2)
B15: D/A2 sign bit

5.5 A/D Conversion

This chapter shows you how to program your DM35520 to perform A/D conversions and read the results. Included in this discussion are instructions on setting up the Channel Gain Table (CGT), the on-board clocks and sample counter, and various conversions and triggering modes. The following paragraphs walk you through the programming steps for performing A/D conversions. Detailed information about the conversion modes and triggering is presented in this section. You can follow these steps in the example programs included with the board.

5.5.1 Before Starting Conversions: Initializing the Board

Regardless of the conversion mode you wish to set up, you should always start your program with a board initialization sequence. This sequence should include:

- Clear Board Command
- Clear IRQ command
- Clear Channel Gain Table command
- Clear A/D FIFO command
- Clear D/A FIFOs commands
- Clear Digital I/O chip

This initialization procedure clears all board registers, empties the Channel Gain Table, resets the digital I/O chip and empties the A/D and D/A FIFOs.

Before Starting Conversions (single-channel mode): Programming Channel Gain Latch (CGL)

Setting up these things can be done using the Channel Gain Latch (single-channel mode) or using the Channel Gain Table (multi-channel mode) The CGL can be filled up by Function 0x301. The Channel Gain Latch has very similar structure to the Channel Gain Table, so all operations are explained in the next sections of CGT.

Before Starting Conversions (multi-channel mode): Programming the Channel-Gain Table (CGT)

The Channel Gain Table can be programmed with 1024 24-bit entries in tabular format. Sixteen bits contain the A/D channel-gain data (A/D Table), and 8 bits contain digital control data (Digital Table) to support complex channel-gain sequences. To load a new Channel Gain Table, first: clear the Channel Gain Table by Function 0x030F. To add entries to an existing table, simply write to the A/D Table (and Digital Table if used) as described in the following paragraphs. Note that writing beyond the end of the table is ignored.

16-Bit A/D Table

The A/D portion of the Channel Gain Table with the channel, gain, input range, input type, pause and skip bit information is programmed into the channel-gain scan memory using the Function 0x300. If you have cleared the existing table, the first word written will be placed in the first entry of the table, the second word will be placed in the second entry, and so on. If you are adding to an existing table, the new data written will be added at the end.

Channel Select, Gain Select, Input Range and Input Type

The channel number, gain value, input range and input type are entered in the table using bits 0 through 10. Each of these parameters can be set independently for every entry in the table. This allows you to set up a complex array of sampling sequences mixing channels, gains, input ranges and input types. Care must be taken in selecting the proper input type. The board is capable of 16 single-ended inputs or 8 differential inputs. You can select combinations of single-ended and differential but each differential channel actually uses 2 single-ended channels. If you select channel 1 to be a differential channel, you must connect your signal to AIN1+ and AIN1-. Channel 8 now is not available as a single-ended channel. In the case of single ended mode you can choose the Ground Referenced Single Ended (GRSE mode) or the Non Referenced Single Ended Mode (NRSE).

Pause bit

Bit 11 is used as a pause bit. If this bit is set to a "1" and the Pause function is enabled by Function 0x0305, the A/D conversions will stop at this entry in the table and resume on the next Start Trigger. This is useful if you have 2 different sequences loaded in the table. You can enable and disable this bit's function by Function 0x305. In the case of single channel mode, when the CGL is used this function is meaningless. NOTE: This bit is ignored in the Burst sampling modes.

D/Ax update bits

Bit 12, 13 is used for simultaneous update of the D/Ax converter with the sampling of the appropriate analog input channel. When these bits are in high state a D/A update signal is generated at the sampling time of the analog input.

Skip bit

If bit 14 of the data loaded is set to 1, then the skip bit is enabled and this entry in the channel-gain table will be skipped, meaning an A/D conversion will be performed but the data is not written into the A/D FIFO. This feature provides an easy way to sample multiple channels at different rates without saving unwanted data. A simple example illustrates this bit's function.

In this example, we want to sample channel 1 once each second and channel 4 once every three seconds. First, we must program 6 entries into the channel-gain table. The channel 4 entries with the skip bit set will be skipped when A/D conversions are performed. The table will continue to cycle until a stop trigger is received.

Next, we will set the pacer clock to run at 2 Hz (0.5 seconds). This allows us to sample each channel once per second, the maximum sampling rate required by one of the channels (pacer clock rate = number of different channels sampled x fastest sample rate). The first clock pulse starts an A/D conversion according to the parameters set in the first entry of the channel-gain table, and each successive clock pulse incrementally steps through the table entries. The first clock pulse starts a sample on channel 1. The next pulse looks at the second entry in the channel-gain table and sees that the skip bit is set to 1. No A/D data is stored. The third pulse starts a sample on channel 1 again, the fourth pulse skips the next entry, and the fifth pulse takes our third reading on channel 1. On the sixth pulse, the skip bit is disabled and channel 4 is sampled. Then the sequence starts over again. Samples are not stored when they are not wanted; saving memory and eliminating the need to throw away unwanted data.

8-Bit Digital Table

The digital portion of the channel-gain table can be programmed with digital control information using the Write Digital Table Function 0x0302. If you have cleared the existing table by the CGT clear Function 0x030F, the first byte written will be placed in the first entry of the table, the second byte will be placed in the second entry, and so on. If you are adding to an existing table, the new data written will be added at the end. The first entry made into the Digital Table lines up with the first entry made into the A/D Table, the second entry made into the Digital Table lines up with the second entry made into the A/D Table, and so on. Make sure that, if you add to an existing table and did not program the Digital Table portion when you made your A/D Table entries previously, you fill those entries with digital data first before entering the desired added data. Since the first digital entry you make always lines up with the first A/D entry made, failure to do this will cause the A/D and digital control data to be misaligned in the table. You cannot turn the digital control lines off for part of a conversion sequence and then turn them on for the remainder of the sequence. Note that the digital data programmed here is sent out on the Port 1 digital I/O lines whenever this portion of the table is enabled by the Function 0x0304.

These lines can be used to control input expansion boards such as the TMX32 analog input expansion board at the same speed as the A/D conversions are performed with no software overhead.

NOTE: If you only need to use the A/D part of the table, you do not have to program the Digital Table. However if you only want to use the Digital part of the table you must program the A/D part of the table.

Setting Up A/D part and Digital part of Channel Gain Table

Let's look at how the Channel Gain Table is set up for a simple example using both the A/D and Digital Tables. In this example, we have a TMX32 expansion board connected to channel 1 on the DM35520. Load the channel-gain sequence into the A/D Table (Function 0x0300):

```
Entry 1       0000 0000 0000 0000 gain = 1, channel number = 1
Entry 2       0000 0000 0010 0000 gain = 4, channel number = 1
Entry 3       0100 0000 0000 0000 skip sample
Entry 4       0000 0000 0010 0000 gain = 4, channel number = 1
Entry 5       0000 0000 0000 0000 gain = 1, channel number = 1
Entry 6       0000 0000 0010 0000 gain = 4, channel number = 1
```

Load the digital data into the Digital Table by Function 0x0302. The first digital word loaded lines up with the first A/D Table entry, and so on:

```
Entry 1 0000 0000 0000 0000 gain=1 DM35520 channel=1 0000 0000 TMX32 channel=1
Entry 2 0000 0000 0010 0000 gain=4 DM35520 channel=1 0000 0011 TMX32 channel=4
Entry 3 0000 1000 0000 0000 skip sample              0000 0000 TMX32 channel=1 (skip)
Entry 4 0000 0000 0010 0000 gain=4 DM35520 channel=1 0000 0011 TMX32 channel=4
Entry 5 0000 0000 0000 0000 gain=1 DM35520 channel=1 0000 0000 TMX32 channel=1
Entry 6 0000 0000 0010 0000 gain=4 DM35520 channel=1 0000 0011 TMX32 channel=4
```

Using the Channel Gain Table for A/D Conversions

After the Channel Gain Table is programmed, it must be enabled in order to be used for A/D conversions by Function 0x0303. The Digital Table can be enabled by Function 0x0304 when the digital control data is stored. You cannot use the Digital Table without enabling the Channel Gain Table. When the Digital Table is enabled, the 8-bit data is sent out on the Port 1 digital I/O lines.

When you are using the channel-gain table to take samples, it is strongly recommended that you do not enable, disable, and then re-enable the table while performing a sequence of conversions. This causes skipping of an entry in the table. In this case you should issue a reset table command by Function 0x030E.

Channel-gain Table and Throughput Rates

When using the Channel Gain Table, you should group your entries to maximize the throughput of your module. Low-level input signals and varying gains are likely to drop the throughput rate because low level inputs must drive out high level input residual signals. To maximize throughput:

- Keep channels configured for a certain range grouped together, even if they are out of sequence.
- Use external signal conditioning if you are performing high speed scanning of low level signals. This increases throughput and reduces noise.
- If you have room in the channel-gain table, you can make an entry twice to make sure that sufficient settling time has been allowed and an accurate reading has been taken. Set the skip bit for the first entry so that it is ignored.
- For best results, do not use the channel-gain table when measuring steady-state signals. Use the single convert mode to step through the channels.

5.5.2 A/D Conversion Modes

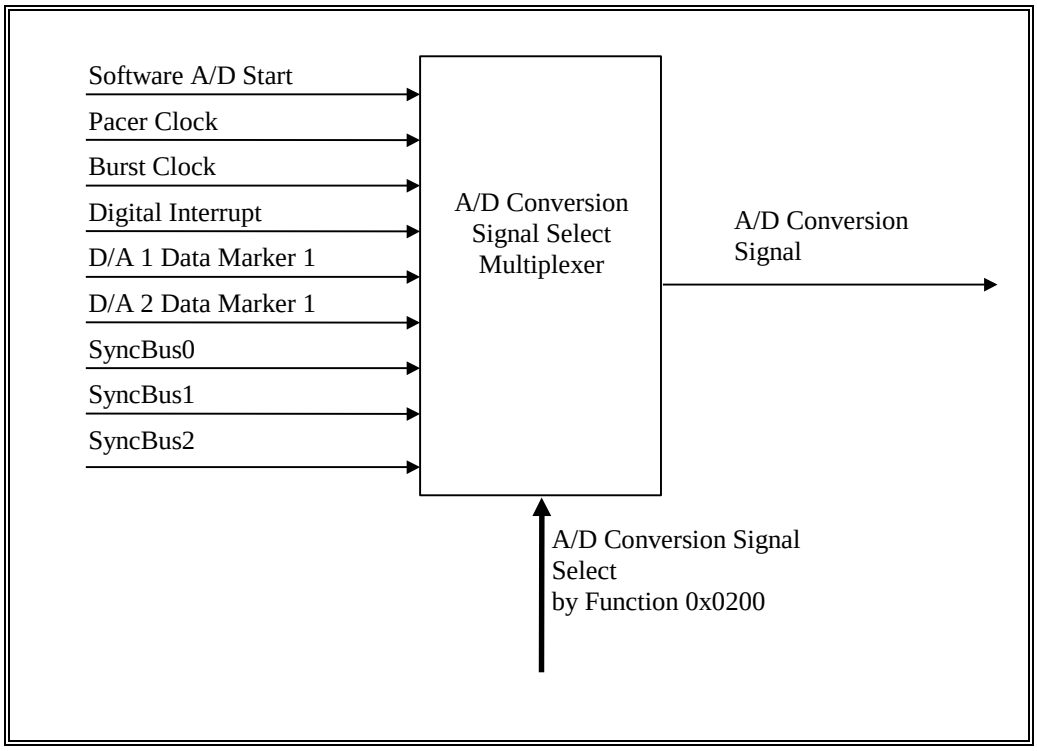
To support a wide range of sampling requirements, the DM35520 provides several conversion modes with a selection of trigger sources to start and stop a sequence of conversions. Understanding how these modes and sources can be configured to work together is the key to understanding the A/D conversion capabilities of your module.

The following paragraphs describe the conversion and trigger modes.

Start A/D Conversion signal

Using the Function 0x0200 one of nine modes can be selected as A/D conversion signal as can be seen on Figure 17 below.

Figure 17: A/D Conversion Signal



- *Software A/D Start* (by writing LAS0+8h to initiate a Start Convert)
- *Pacer Clock* (internal TC)
- *Burst Clock* (internal TC)
- *Digital Interrupt* generated by the Advanced Digital Interrupt circuit
- *D/A 1 Data Marker 1** for simultaneous A/D conversion with D/A update
- *D/A 2 Data Marker 1** for simultaneous A/D conversion with D/A update
- *SyncBus* signals (three lines)

Pacer Clock Start/Stop Trigger Select

The Pacer Clock start trigger can be set by the Function 0x0202. The Pacer Clock stop trigger can be set by the Function 0x0203. This function can be used to turn the pacer clock (internal or external) on and off. Through these different combinations of start and stop triggers, the DM35520 supports pre-trigger, post-trigger, and about-trigger modes with various trigger sources.

The Pacer Clock start trigger sources are:

- *Software Pacer Start* When selected, a read at LAS0+14h will start the Pacer Clock.
- *External trigger* When selected, a positive- or negative-going edge (depending on the setting of the trigger polarity, Function 0x0601) on the external TRIGGER INPUT line, will start the pacer clock. The pulse duration should be at least 100 nanoseconds.
- *Digital interrupt* When selected, a digital interrupt -generated by Advanced Digital I/O chip - will start the Pacer Clock.
- *User TC 2 out* When selected, a pulse on the User Timer/Counter 2 output line (Counter 2's count reaches 0) will start the pacer clock.
- *SyncBus 0..2* When selected a positive edge on the SyncBus 0 line will start the pacer clock.

The following start trigger sources provide delayed triggering. When the trigger is issued, the A/D delay counter, counts down and conversions are started when the A/D delay counter reaches 0. The A/D delay counter counts at the pacer clock rate.

- *Delayed Software Pacer Start*. When selected, a read at LAS0+14h will start the delay counter.
- *Delayed external trigger.* When selected, a positive- or negative-going edge (depending on the setting of the trigger polarity, bit 11 in the Control Register) on the external TRIGGER INPUT line, will start the delay counter. The pulse duration should be at least 100 nanoseconds.
- *Delayed digital interrupt*. When selected, a digital interrupt will start the delay counter.
- *Delayed User TC Counter 2 output*. When selected, a pulse on the Counter 2 output line (Counter 2's count reaches 0) will start the delay counter.
- *Delayed SyncBus 0..2* When selected, a pulse on the SyncBus0 will start the delay counter.

- *External Trigger Gated mode.* When selected, the pacer clock runs when the external TRIGGER INPUT line is held high. When this line goes low, conversions stop. This trigger mode does not use a stop trigger. If the trigger polarity bit is set for negative, the pacer clock runs when this line is low and stops when it is taken high.

The Pacer Clock stop trigger sources are:

- *Software Pacer Stop trigger.* When selected, a write at LAS0+14h will stop the Pacer Clock.
- *External trigger.* When selected, a positive- or negative-going edge (depending on the setting of the trigger polarity, setting up by Function 0x602) on the external TRIGGER INPUT line, will stop the Pacer Clock. The pulse duration should be at least 100 nanoseconds.
- *Digital interrupt.* When selected, a digital interrupt will stop the pacer clock.
- *About Counter.* When selected, the Pacer Clock stops when the About Counter's count reaches 0. About Counter counts samples which are written into the A/D FIFO
- *User TC2 out* When selected, the Pacer Clock stops when the User TC 2 counter's count reaches 0.
- *SyncBus0.. 2 signals* when selected, the Pacer Clock stops when there is a rising edge on the SyncBus line.

The following stop trigger sources provide ABOUT triggering, where data is acquired from the time the start trigger is received, and continues for a specified number of samples after the stop trigger. The number of samples to acquire after the stop trigger is programmed in the About Counter. About Counter counts samples which are written into the A/D FIFO

- *About Software Pacer Stop trigger*. When selected, a Software Pacer Stop trigger starts the About counter, and sampling continues until the About Counter's count reaches 0.
- *About external trigger.* When selected, an external trigger starts the About counter, and sampling continues until the sample counter's count reaches 0.
- *About digital interrupt.* When selected, a digital interrupt starts the About Counter, and sampling continues until the About Counter's count reaches 0.
- *About User TC Counter 2 output.* When selected, a pulse on the User Timer Counter 2 output line (Counter 2's count reaches 0) starts the About Counter, and sampling continues until the About Counter's count reaches 0.
- *About SyncBus0.. 2.* When selected, a rising edge on SyncBus0..2 starts the About Counter, and sampling continues until the About Counter's count reaches 0.

Note that the external trigger (TRIGGER INPUT) can be set to occur on a positive-going edge or a negative-going edge, depending on the setting up the Function 0x0602.

Burst Clock Start Trigger to trigger burst sample

The following paragraph describes the operation when the A/D conversion start signal is selected as Burst Clock. Burst clock is an output of Timer Counter. The clock signal of the Burst Clock Timer Counter is 8MHz or 20MHz. The gate signal of this TC is used to start and stop the Burst Clock. The start signal can be select from the following list, and the stop is derived from the empty signal of Channel Gain Table. The Burst Clock operation belongs to the Multichannel - Channel Gain Table operation.

The start triggers can be set by Function 0x0201:

- *Software A/D start* (by writing LAS0+8h)
- *Pacer Clock* (internal or external)
- *external TRIGGER INPUT*
- *Digital Interrupt*
- *SyncBus0.. 2*

Single Cycle Mode, Trigger Repeat mode

Using the Pacer Start Mode select Function 0x0205 the Single Cycle mode or the Trigger Repeat Mode can be selected. This function controls the conversion sequence when using a trigger to start the Pacer Clock. When the Function argument is low, the first pulse on the selected Pacer Clock Start Trigger source will start the pacer clock. After the stop trigger has ended the conversion cycle, the triggering circuit is disarmed and must be rearmed before another start trigger can be recognized. To rearm this trigger circuit, you must issue a Software A/D Start command (Write LAS0+8h).

When Function argument is high, the conversion sequence is repeated each time a selected Pacer Clock Start Trigger is received.

Pacer Clock Source

The Pacer Clock can be generated from an internal source or an external source using the Function 0x0509.

Types of Conversions

Single Conversion
In this mode, a single specified channel is sampled whenever the Software A/D Start Command is occurred. The active channel is the one specified in the Channel Gain Latch. This is the easiest of all conversions. It can be used in a wide variety of applications, such as sample every time a key is pressed on the keyboard, sample with each iteration of a loop, or watch the system clock and sample every five seconds.

Multiple Conversions
In this mode, conversions are continuously performed at the Pacer Clock rate, or other selected A/D Conversion Signal rate. The pacer clock can be internal or external. The maximum rate supported by the board is 1.25MHz. The Pacer Clock can be turned on and off using any of the start and stop triggering modes using the Function 0x202, and 0x203. If you use the internal pacer clock, you must program it to run at the desired rate.

This mode is ideal for filling arrays, acquiring data for a specified period of time, and taking a specified number of samples.

Random Channel Scan
In this mode, the Channel Gain Table is incrementally scanned through, with each selected A/D Conversion Signal pulse starting a conversion at the channel and gain specified in the current table entry. Before starting a conversion sequence Channel Gain Table, you need to load the table with the desired data. Then make sure that the Channel Gain Table is enabled by the Function 0x0303. This enables the A/D portion of the Channel Gain Table. If you are using the Digital Table as well, you must also enable this using the Function 0x0304. Each rising edge of selected A/D Conversion Signal starts a conversion using the current Channel Gain data and then increments to the next position in the table. When the last entry is reached, the next pulse starts the table over again.

Programmable Burst
In this mode, a single trigger initiates a scan of the entire Channel-gain table. Before starting a burst of the channel-gain table, you need to load the table with the desired data. Then make sure that the channel-gain table is enabled. If you are using the Digital Table as well, you must also enable it.

Burst is used when you want one sample from a specified number of channels for each trigger. The burst trigger, which is a trigger or pacer clock, triggers the burst and the burst clock initiates each conversion. At high speeds, the burst mode emulates simultaneous sampling of multiple input channels. For time critical simultaneous sampling applications, a simultaneous sample-and-hold board can be used (SS8 eight-channel boards are available from RTD).

Programmable Multiscan
This mode - when the A/D Conversion Start Signal is the Burst Clock - lets you scan the Channel Gain Table after a Burst Clock Start Signal. When the Channel Gain Table is empty the Burst Clock is stopped, and waiting for a new Start Signal.

As you can see, DM35520 is designed to support a wide range of conversion requirements. You can set the clocks, triggers, and channel and gain to a number of configurations to perform simple or very complex acquisition schemes where multiple bursts are taken at timed intervals. Remember that the key to configuring the board for your application is to understand what signals can actually control conversions and what signals serve as triggers. The discussions presented in this section and the example programs on the disk should help you to understand how to configure the board.

Starting an A/D Conversion
Depending on your conversion and trigger settings, the Software A/D Start command (Write LAS0 + 010h) has different functions. In any mode that uses the Software A/D Start command, this command will do the appropriate action. In any mode that does not use the Software A/D Start command as the trigger; you will still need to do a write the LAS0 + 010h to arm (enable) the triggering circuitry. An example of this would be, if you set the Pacer Clock Start Trigger as external trigger, write the LAS0 + 010h is required to arm the external trigger circuitry. After you have set all the trigger and conversion registers to the proper values, the last command will need to be Software A/D Start. Any external triggers received before this command will be ignored. It is also a good practice to clear the A/D FIFO just prior to triggering the measurement or arming the trigger. Study the example programs to see this sequence.

Conversion Status Monitoring
The A/D conversion status can be monitored through the A/D FIFO empty flag in the FIFO status word read at LAS0+8h. Typically, you will want to monitor the Empty flag (active low) for a transition from low to high. This tells you that a conversion is complete and data has been placed in the sample buffer.

Halting Conversions
In single convert modes, a single conversion is performed and the module waits for another Software A/D Start command. In multi-convert modes, conversions are halted by one of two methods: when a stop trigger has been issued to stop the pacer clock, or when the FIFO is full. The Pacer Clock Shut Down Flag, bit 4 of the status word (LAS0 + 02Ch), is set when the sample buffer is full, disabling the A/D converter. Even if you've removed data from the sample buffer since the buffer filled up and the FIFO full flag is no longer set, the Pacer Clock Shut Down

Flag will confirm that at some point in your conversion sequence, the sample buffer filled and conversions were halted. At this point a clear A/D FIFO command must be issued and a Software A/D Start convert (write at LAS0 + 010h) to rearm the trigger circuitry.

5.5.3 Reading the Converted Data

Each 12-bit conversion is stored in a 16-bit word in the sample buffer, in the A/D FIFO. The buffer can store 1024 samples. This section explains how to read the data stored in the sample buffer.

The sample buffer - A/D FIFO contains the converted data and 3-bit data marker (if used) in a 16-bit word.

The 12-bit A/D data + sign bit are left justified in a 16-bit word, with the least significant three bits reserved for the data marker. Because of this, the A/D data read must be scaled to obtain a valid A/D reading. The data marker portion should be masked out of the final A/D result. Shifting the word three bits to the right will eliminate the data marker from the data word. If you are using the data marker, then you should preserve these bits someplace in your program.

The output code format is always two's complement. This is true for both bipolar and unipolar signals since the sign bit is added above the 12-bit conversion data. For bipolar conversions, the sign bit will follow the MSB of the 12-bit data. If this bit is a "0", the reading is a positive value. If this bit is a "1", the reading is a negative value. When the input is a unipolar range, the coding is the same except that the sign bit is always a "0" indicating a positive value. The data should always be read from the A/D FIFO as a signed integer.

Voltage values for each bit will vary depending on input range and gain. For example, if the input is set for ±5 volts and the gain = 1, the formula for calculating voltage is as follows:

Voltage = ((input range / Gain) / 4096) x Conversion Data
Voltage = ((10 / 1) / 4096) x Conversion Data
Voltage = 2.44 mV x Conversion Data

Remember that when you change the gain, you are increasing the resolution of the bit value but you are decreasing the input range. In the above example if we change the gain to 4, each bit will now be equal to 610 μV but our input range is decreased from 10 volts to 2.5 volts. The formula would look like this:

Voltage = ((input range / Gain) / 4096) x Conversion Data
Voltage = ((10 / 4) / 4096) x Conversion Data
Voltage = 610 uV x Conversion Data

If we now change the input range to ±10 volts and the gain = 1, the formula would be:

Voltage = ((input range / Gain) / 4096) x Conversion Data
Voltage = ((20 / 1) / 4096) x Conversion Data
Voltage = 4.88 mV x Conversion Data

5.5.4 Using the A/D Data Markers

For certain applications where you may want to store digital information with the analog data at the same rate the analog data is being acquired, the bottom three bits of the converted data are available for this feature. For example, you may want to tag the acquired data with a marker so that you know when the data was sampled. Three lines are available at I/O connector to send the data marker settings to the sample buffer along with the 12-bit A/D converted data. These lines are P0.5, P0.6 and P0.7.

5.5.5 Programming the Pacer Clock

The DM35520 has a 24 bit count down on-board pacer clock with 8MHz/20MHz clock signal. When you want to use the pacer clock for continuous A/D conversions, you must select the Pacer Clock as A/D Conversion Signal and program the clock rate.

The pacer clock is accessed for programming at LAS0 + 040 address. To find the value you must load into the clock to produce the desired rate, you first have to calculate the value of Divider for the 24-bit clock. The formulas for making this calculation are as follows:

Pacer Clock frequency = 8 (20) MHz/(Divider+1)
Divider = (8 (20) MHz / Pacer Clock Frequency) - 1

The Pacer Clock frequency range is 1.14 MHz.. 0.47Hz defined by the 8MHz clock frequency, the 24bit wide counter and the 1.25MHz maximum Sampling frequency.

Table 21: Pacer Clock Frequency

Pacer Clock	Sampling Cycle Time	Pacer Clock	Sampling Cycle Time	Divider (decimal)
Primary Clock – 8 MHz See Function 0X0501 (1DCh)		Primary Clock – 20 MHz See Function 0X0501 (1DCh)		
1.14MHz	877ns	-	-	6
1MHz	1µs	-	-	7
888.89kHz	1.125µs	-	-	8
800kHz	1.25µs	-	-	9
500kHz	2µs	1.25MHz	800ns	15
470.588kHz	2.15µs	1.176MHz	850ns	16
..	..	..	..	..
100kHz	10µs	250kHz	4µs	79
..	..	..	..	..
50kHz	20µs	125kHz	8µs	159
10kHz	100µs	25kHz	40µs	799
1kHz	1ms	2.5kHz	0.4ms	7999
100Hz	10ms	250Hz	4ms	79999
10Hz	100ms	25Hz	40ms	799999
1Hz	1s	2.5Hz	0.4s	7999999
477mHz	2.09s	1.19Hz	0.84s	16777216

Writing the Divide r into the LAS0 + 040h the Pacer Clock works immediately according to this value. Writing process clears the Counter - generates a Pacer Clock pulse, and loads the Divider value to the Counter.

5.5.6 Programming the Burst Clock

The DM35520 has a 16-bit count down on-board Burst Clock timer with 8 / 20MHz clock signal. When you want to use the Burst Clock for performing A/D conversions in the burst mode, you must program the clock rate by writing the LAS0 + 044h. To find the Divider value you must load into the Burst Clock Counter to produce the desired rate, make the following calculation:

The Burst Clock Frequency Range is 1.14MHz.. 122Hz – 8MHz primary clock, and 1.25MHz.. 305Hz – 20MHz primary clock

Burst Clock Frequency = 8 / 20 MHz / (Divider+1)
Divider = (8 / 20 MHz / Pacer Clock Frequency) – 1

Table 22: Burst Clock Frequency

Burst Clock	Sampling Cycle Time	Burst Clock	Sampling Cycle Time	Divider (decimal)
Primary Clock – 8 MHz See Function 0X0502 (1E0h)		Primary Clock – 20 MHz See Function 0X0502 (1E0h)		
1.14MHz	877ns	-	-	6
1MHz	1µs	-	-	7
888.89kHz	1.125µs	-	-	8
800kHz	1.25µs	-	-	9
500kHz	2µs	1.25MHz	800ns	15
100kHz	10µs	250kHz	4µs	79
50kHz	20µs	125kHz	8µs	159
10kHz	100µs	25kHz	40µs	799
122Hz	8.1ms	305.17Hz	3.2ms	65535

For example to set the burst clock frequency at 100 kHz, this equation becomes:

Divider = (8 MHz / Pacer Clock Frequency) - 1 = 8MHz/100kHz - 1 = 79

After you determine the divider value that will result in the desired clock frequency, write it into the LAS0 + 044h. Writing the Divider into the LAS0 + 044h the Burst Clock works immediately according to this value. Writing process clears the Counter - generates a Burst Clock pulse, and loads the Divider value to the Counter.

5.5.7 Programming the About Counter

The About Counter lets you program the DM35520 to take a certain number of samples and then halt conversions. (Select A/D Conversion Signal to Pacer Clock, selects the Pacer Clock Stop Trigger to About Counter) The number of samples minus one to be taken is loaded into the 16-bit About Counter at LAS0 + 058h.

Note that once the counter is properly loaded and starts, any subsequent countdowns of this count will be accurate.

After you determine the desired number of samples, load the number minus 1 to the About Counter register.

Note: Make sure all registers are set and board and FIFO's are cleared before enabling interrupts.

Using the About Counter to Create Large Data Arrays

The 16-bit About Counter allows you to take up to 65,535 samples before the count reaches 0 and sampling is halted. Suppose, however, you want to take 100,000 samples and stop. The DM35520 provides a Function, About Counter Stop Enable 0x0204 which allows you to use the About counter to take more than 65,535 samples in a conversion sequence.

The About Counter stop enable bit can be set to 1 to allow the sample counter to continuously cycle through the loaded count until the stop enable bit is set to 0, which then causes the sample counter to stop at the end of the current cycle. Let's look back at our example where we want to take 100,000 readings. First, we must divide 100,000 by a whole number that gives a result of less than 65,535. In our example, we can divide as follows:

Sample Counter Count = 100,000 / 2 = 50,000

To use the sample counter to take 100,000 samples, we will load a value of 50,000 into the counter and cycle the counter two times. After the value is loaded, make sure that the Stop Bit is set to 1 so that the sample counter will cycle. Then, set up the sample counter so that it generates an interrupt when the count reaches 0. Initialize the sample counter as described in the preceding section and start the conversion sequence. When the sample counter interrupt occurs telling you that the count has reached 0 and the cycle is starting again, set the Stop Bit to 0 to stop the sample counter after the second cycle is completed. The result: the sample counter runs through the count two times and 100,000 samples are taken.

5.6 D/A Conversion

This chapter explains how to perform D/A conversions on DM35520.

Two independent 12-bit analog output channels are included on the DM35520. The analog outputs are generated by two 12-bit D/A converters with independent software programmable output ranges. Each D/A channel have 1KSample D/A FIFO. The analog output signals are accompanied by two digital data markers, DM0, and DM1. The DM0 bits are buffered and wired to the External I/O Connector. The DM1 bits may be the Start Conversion Signal of A/D converter. The digital data markers are updated simultaneously with the analog output signal.

D/A1 data is written to LAS1 + 8h and D/A2 data is written to LAS1 + Ch. The data are written into the D/A FIFOs, and the Update signals read the FIFOs, and update the D/A converters.

The configuration of D/A channels can be done by D/A1 and D/A2 Function groups (0x400... 0x040F).

The Function 0x0400 (0x0407 for D/A2) sets the voltage output range and polarity for D/A1. The output ranges are ±5, ±10, 0 to +5, or 0 to +10 volts.

The Function 0x0401 selects the update source for D/A1:

- *Software D/A1 Update.* Write a dummy data to LAS0+14h. (LAS0+18h for D/A2)
- *CGT Controlled D/A1 Update* If the D12 (D13 for D/A2) bit of CGT is 1 the D/A1 is updated simultaneously with the A/D sampled analog input
- *DAC Clock* The 24bit D/A clock inside the control logic.

The DM35520 has a 16-bit count down on-board DAC Clock timer with 8 / 20MHz clock signal. When you want to use the DAC Clock for performing D/A conversions in the burst mode, you must program the clock rate by writing the LAS0 + 05Ch. To find the Divider value you must load into the DAC Clock Counter to produce the desired rate, make the following calculation:

The DAC Clock Frequency Range is 200 kHz... 0.47Hz – 8MHz primary clock, and 200 kHz... 1.19Hz – 20MHz primary clock.

Burst Clock Frequency = 8 / 20 MHz / (Divider+1)

Divider = (8 / 20 MHz / Pacer Clock Frequency) – 1

Table 23: DAC Clock Frequency

DAC Clock	Sampling Cycle Time	DAC Clock	Sampling Cycle Time	Divider (decimal)
Primary Clock – 8 MHz See Function 0X0503 (1E4h)		Primary Clock – 20 MHz See Function 0X0503 (1E4h)		
200kHz	5µs	-	-	39
195.1kHz	5.125µs	-	-	40
80kHz	12.5µs	200kHz	5µs	99
79.208kHz	12.625µs	198.02kHz	5.05µs	100
10kHz	100µs	25kHz	40µs	79
8kHz	125µs	20kHz	50µs	999
0.47Hz	2.127s	1.19Hz	0.838s	15916777215

For example to set the DAC clock frequency at 100 kHz, this equation becomes:

Divider = (8 MHz / DAC Clock Frequency) - 1 = 8MHz/100kHz - 1 = 79

After you determine the divider value that will result in the desired clock frequency, write it into the LAS0 + 05Ch. Writing the Divider into the LAS0 + 05Ch the DAC Clock works immediately according to this value. Writing process clears the Counter - generates a DAC Clock pulse, and loads the Divider value to the Counter. Note, that the DAC clock needs a start command.

- *External Pacer Clock* The rising edge of External Pacer Clock at the external I/O Connector updates the D/A1. The minimum pulse with is 100ns.
- *SyncBus0... 2* The rising edge of SyncBus signals updates the D/A1. The source of SyncBus signals may be on the same board or on another DM35520 board.

The Function 0x0402 (0x040A for D/A2) selects the cycled or not cycled mode for D/A1. In the case of cycled mode, emptying the D/A1 FIFO the Update pointer of the FIFO is set to the beginning of the data array in the FIFO. This mode can be used for generating periodic signals without any processor intervention. This means that setting this bit to a 1; the D/A1 will continuously repeat the data that is stored in the D/A1 FIFO. This is useful for waveform generation. The not cycled mode is the normal operation mode.

The Function 0x0406 (0x040E for D/A2) resets the D/A1 FIFO. This Function sets the update pointer of the D/A1 FIFO to the beginning of the data array in the FIFO.

The Function 0x0407 (0x040 for D/A2) clears the D/A1 FIFO. This Function sets the update and write pointer of the D/A1 FIFO to the beginning of. This means that the FIFO is ready to fill with new data.

The following tables list the key digital codes and corresponding output voltages for the D/A converters.

Table 24: DAC Bipolar Binary Value vs. Output Voltage

Bipolar D/A Bit Weight	Ideal Output Voltage(mV)	
	-5 to +5 Volts	-10 to +10 Volts
2047	+4997.56	+9995.12
1024	+2500.00	+5000.00
512	+1250.00	+2500.00
256	+625.00	+1250.00
128	+312.50	+625.00
64	+156.25	+312.50
32	+78.13	+156.25
16	+39.06	+78.13
8	+19.53	+39.06
4	+9.77	+19.53
2	+4.88	+9.77
1	+2.44	+4.88
0	0	0.00
-1	-2.44	-4.88
-2	-4.88	-9.77
-4	-9.77	-19.53
-8	-19.53	-39.06
-16	-39.06	-78.13
-32	-78.13	-156.25
-64	-156.25	-312.50
-128	-312.50	-625.00
-256	-625.00	-1250.00
-512	-1250.00	-2500.00
-1024	-2500.00	-5000.00
-2048	-5000.00	-10000.00

Table 25: DAC Unipolar Binary Value vs. Output Voltage

Unipolar D/A Bit Weight	Ideal Output Voltage(mV)	
	-5 to +5 Volts	-10 to +10 Volts
4095	+4997.56	+9995.12
2047	+2500.00	+5000.00
1024	+1250.00	+2500.00
512	+625.00	+1250.00
256	+312.50	+625.00
128	+156.25	+312.50
64	+78.13	+156.25
32	+39.06	+78.13
16	+19.53	+39.06
8	+9.77	+19.53
4	+4.88	+9.77
2	+2.44	+4.88
1	+1.22	+2.44
0	0	0.00

5.6.1 1K Sample Buffer

Each D/A channel have a 1k sample buffers for storing data to be sent to the D/A converter (D/A FIFO). This means that you can fill the buffer with data and set up the D/A to output this data automatically. This is very useful for outputting high speed data or generating waveforms with precise timing requirements. By setting the cycled mode, you can fill the buffer with one cycle of a wave, start the D/A update clock and the buffer will continue to repeat until the clock is stopped. Combining this feature with the variety of update sources, you can build a flexible waveform generator.

If you are trying to generate a non-repetitive waveform, you can combine the sample buffer capability with the D/A Update Counter. To utilize this feature of the DM35520 properly, you should load the buffer with data, program the D/A Update Counter for half the buffer size (512 samples), and use the Update Counter to generate an interrupt. When an interrupt is received, you should reload the buffer with 512 new samples. By continuing this cycle, you can generate a non-repetitive waveform at high speeds.

Status of the FIFO buffers can be monitored at LAS0 + 010h. Any samples that are written to the FIFO after it is full will be ignored. You can write up to 1024 samples to the buffer before it is full. Each update pulse (either software or from one of the clocks) will remove a sample from the buffer and send it out the D/A. Each update - read after the FIFO buffer is empty will be ignored, and the output of the D/A remains in the last updated state.

At power-up or reset, the D/A outputs are set to 0 volts. Before loading data into the sample buffer it is best to clear the buffer by Function 0x0407 or 0x040F. When you issue the "Clear D/A FIFO" command, all data in the buffer is erased. If you issue the "Reset DAC FIFO" command, the data in the buffer is not erased, however the address pointer is set back to the beginning of the buffer: This is useful when you are generating waveforms and stop the updating in the middle of a cycle.

5.6.2 D/A Cycled or Not Cycled Mode

The cycle bit is used to make the buffer data repeat. Under normal operation, without the cycled mode set, data is written into the buffer and the update clock reads data out of the buffer. When the buffer is empty, the output of the D/A remains unchanged. If you set the cycle bit high, the data in the buffer will repeat. If you load a data set into the buffer, when the update clock reaches the end of the data it will automatically wrap around to the beginning and start over. This is useful for generating waveforms.

5.6.3 D/A Update Counters

The D/A1 and D/A2 16 bit wide Update Counters, are useful when using clocks to output data to the D/As. The counters can be accessed at LAS0 + 04Ch, ill LAS0 + 050h addresses. These counters will count update pulses sent to the D/A's and can be polled to read the current count or can be used to generate interrupts when the count reaches 0. These counters can be loaded to any starting value and count down. When the count reaches 0 it will automatically be reloaded with the original starting value.

5.6.4 D/A DATA MARKERS

The D/A Data Markers are used to send out digital pulses synchronized to the D/A analog output. Since each D/A FIFO buffer is 16 bits wide and the D/A only uses 12 bits, there are bits left for Data Markers. Two of these bit locations can be filled with data and this data is sent out on the appropriate pins synchronized to the D/A analog output. This is useful for sending out a trigger pulse each time a waveform crosses zero or to send out pulses to trigger A/D conversions at the proper time in the D/A waveform. Each D/A channel have 2 Data Marker bits. The DM0 outputs can be accessed at the external I/O connector.

5.7 Data transfer using DMA

There are three DMA modes. Those modes are single, block, and demand. Single mode transfers 1 data value per DMA request. Block mode transfers the amount of data values contained in the transfer count register at the initiation of one DMA request. Demand mode continually transfers data values until DMA request is de-asserted.

The PCI9080/9056, the PCI controller chip of DM35520 supports two independent DMA channels capable of transferring data from the Local Bus to the PCI Bus or from the PCI Bus to the Local Bus. Each channel consists of a DMA controller and a programmable FIFO. Both channels support Chaining and Non-chaining transfers, Demand mode DMA (can also work in non-demand mode), and End of Transfer (EOT) pins. Master mode must be enabled in the PCI Command register. We use the Demand mode DMA and do not use the EOT pins on the DM35520 Board.

The DMA transfer on the DM35520 can be used for reading or writing the LAS1 address area which contains the input and output FIFOs. Using the onboard DMA controllers we can transfer our data in burst mode, without CPU intervention. The Data transfer may be single cycle - Non-Chaining Mode or multiply cycle - Chaining mode.

The DM35520 uses the demand mode DMA. This means that the DMA transfer is started by a programmable hardware event. (See Demand Mode DMA)

5.7.1 NON-CHAINING MODE DMA

The host processor sets the Local Address (LAS1 FIFO address), PCI Address, transfer count and transfer direction. The host processor then sets a control bit to initiate the transfer or in Demand Mode a DMA request event can initiate the transfer. The PCI9080/9056 arbitrates the PCI and Local Buses and transfer data. Once the transfer is complete, the PCI9080/9056 sets the Channel Done bit to a value of 1 and generates an interrupt to the PCI Host (programmable). DMA Done bit in the internal DMA register can be pooled to indicate the status of DMA transfer. DMA registers are accessible from the PCI Bus and Local Bus.

The Local processor or PCI requires DMA. The PCI9080/9056 is Master on both the PCI and Local Buses. Direct Slave or Direct Master pre-empts DMA. The PCI9080/9056 releases the PCI Bus if one of the following occurs:

- FIFO (of PCI9080/9056) is full
- Terminal count is reached
- PCI Latency Timer (PCILTR[7:0]) expires—normally programmed by the Host PCI BIOS—and PCI GNT# de-asserts
- PCI Host asserts STOP
- Direct Master request pending

The PCI9080/9056 releases the Local Bus if one of the following occurs

- FIFO (of PCI9080/9056) is empty
- Terminal count is reached
- Local Bus Latency Timer (MARBR[7:0]) expires
- BREQ# input is asserted
- Direct Slave request is pending

5.7.2 NON-CHAINING MODE DMA

In Chaining mode DMA, the Host Processor sets up descriptor blocks in local or host memory that are composed of a PCI Address, Local Address, transfer count, transfer direction, and address of the next descriptor block. Host then sets up the address of the initial descriptor block in the Descriptor Pointer register of the PCI9080/9056 and initiates the transfer by setting a control bit. The PCI9080/9056 loads the first descriptor block and initiates the Data transfer. The PCI9080/9056 continues to load descriptor blocks and transfer data until it detects the End of Chain bit is set in the Next Descriptor Pointer register. The PCI9080/9056 can be programmed to interrupt the Local processor by setting the Interrupt after Terminal Count bit or PCI Host upon completion of each block transfer and after all block transfers are complete (done). If chaining descriptors are located in Local memory, the DMA controller can be programmed to clear the transfer size at the completion of each DMA (DMAMODE0[16] and DMAMODE1[16]).

Notes: In Chaining mode DMA, the descriptor includes PCI Address, Local Address, Transfer Size and the Next Descriptor Pointer (DMAPADR0-DMADPR0). The Descriptor Pointer register contains the End of Chain bit, Direction of Transfer, Next Descriptor Address, and Next Descriptor Location. The DMA descriptor can be on Local or PCI memory, or both (first descriptor on Local memory, and second descriptor on PCI memory).

5.7.3 DMA DATA TRANSFERS

The PCI9080/9056 DMA controller can be programmed to transfer data from the Local Bus side to the PCI Bus side or from the PCI Bus side to the Local Bus side.

Demand Mode DMA

The Demand Mode DMA is used on the DM35520 board. This means that a programmable hardware event generate DREQ0 or DREQ1 signal for the DMA controller to start the DMA transfer. Before this process the DMA registers must be initialized by software.

You can select from the following DMA request sources by writing the LAS0+101h and LAS0+102h the addresses:

```
0x0 = A/D Sample Counter ☜
0x1 = D/A1 Sample Counter
0x2 = D/A2 Sample Counter
0x3 = User TC 1
```

The Counter values must be integer*2 because the Demand mode DMA transfers long words.

DMA Priority

DMA Channel 0 priority, DMA Channel 1 priority, or rotating priority can be specified in the DMA Arbitration register.

5.7.4 DMA REGISTERS

The DMA operation is controlled via the DMA registers:

Table 26: DMA Registers

PCI (Offset from PCIBAR0 Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI9080/9056 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0			PCI/Local Writable	Serial EEPROM Writable
80h	100h	DMA Ch 0 Mode			Y	N
84h	104h	DMA Ch 0 PCI Address			Y	N
88h	108h	DMA Ch 0 Local Address			Y	N
8Ch	10Ch	DMA Ch 0 Transfer Byte Count			Y	N
90h	110h	DMA Ch 0 Descriptor Pointer			Y	N
94h	114h	DMA Ch 1 Mode			Y	N
98h	118h	DMA Ch 1 PCI Address			Y	N
9Ch	11Ch	DMA Ch 1 Local Address			Y	N
A0h	120h	DMA Ch 1 Transfer Byte Count			Y	N
A4H	124h	DMA Ch 1 Descriptor Pointer			Y	N
A8H	128h	Reserved	DMA Channel1 Command/ Status Register	DMA Channel0 Command/ Status Register	Y	N
ACh	12Ch	Mode/Arbitration Register			Y	N
B0h	130h	DMA Threshold Register			Y	N

(DMAMODE0; PCI: 80h) DMA Channel 0 Mode Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
1:0	Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits.	Yes	Yes	S = 01 J = 11 C = 11	**01**
5:2	Internal Wait States (data to data).	Yes	Yes	0	**000**
6	Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.	Yes	Yes	0	**1**
7	BTERM# Input Enable. Value of 1 enables BTERM# input. Value of 0 disables BTERM# input. If set to 0, the PCI9080/9056 bursts four Lword maximum at a time.	Yes	Yes	0	**0**
8	Local Burst Enable. Value of 1 enables bursting. Value of 0 disables local bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.	Yes	Yes	0	**1**
9	Chaining. Value of 1 indicates Chaining mode is enabled. For Chaining mode, DMA source address, destination address and byte count are loaded from memory in PCIaddress Spaces. Value of 0 indicates Non-chaining mode is enabled.	Yes	Yes	0	**1 or 0**
10	Done Interrupt Enable. Value of 1 enables interrupt when done. Value of 0 disables interrupt when done. If DMA Clear Count mode is enabled, interrupt does not occur until byte count is cleared.	Yes	Yes	0	**1 or 0**
11	Local Addressing Mode. Value of 1 indicates Local Address LA[31:2] to be held constant. Value of 0 indicates Local Address is incremented.	Yes	Yes		**1**
12	Demand Mode. Value of 1 causes DMA controller to operate in Demand mode. In Demand mode, DMA controller transfers data when its DREQ[1:0]# input is asserted. Asserts DACK[1:0]# to indicate current Local Bus transfer is in response to DREQ[1:0]# input. DMA controller transfers Lwords (32 bits) of data. May result in multiple transfers for 8- or 16-bit bus	Yes	Yes	0	**1**
13	Write and Invalidate Mode for DMA Transfers. When set to 1, the PCI9080/9056 performs Write and Invalidate cycles to PCI Bus. The PCI9080/9056 supports Write and Invalidate sizes of 8 or 16 Lwords. Size specified in PCI Cache Line Size Register. If size other than 8 or 16 is specified, the PCI9080/9056 performs Write transfers rather than Write and Invalidate transfers. Transfers must start and end at Cache Line boundaries.	Yes	Yes	0	**0**
14	DMA EOT (End of Transfer) Enable. Value of 1 enables EOT[1:0]# input pin. Value of 0 disables EOT[1:0]# input pin.	Yes	Yes	0	**0**
15	DMA Stop Data Transfer Mode. Value of 0 sends BLAST to terminate DMA transfer. Value of 1 indicates EOT asserted or DREQ[1:0]# de-asserted during Demand mode DMA terminates a DMA transfer.	Yes	Yes	0	**0**
16	DMA Clear Count Mode. When set to 1, if it is in Local memory, byte count in each chaining descriptor is cleared when corresponding DMA transfer completes. **Note:** If the chaining descriptor is in PCI memory, the count is not cleared. (This is the DM35520 situation)	Yes	Yes	0	**0**
17	DMA Channel 0 Interrupt Select. Value of 1 routes DMA Channel 0 interrupt to PCI interrupt. Value of 0 routes DMA Channel 0 interrupt to Local Bus interrupt.	Yes	Yes	0	**1**
31:18	Reserved.	Yes	No	0	**0.. 0**

(DMAPADR0; PCI:84h) DMA Channel 0 PCI Address Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
31:0	PCI Address Register. This register indicates from where, in PCI memory space, the DMA transfers (reads or writes) start.	Yes	Yes	0	**PCI Data Buffer Address**

(DMALADR0; PCI:88h) DMA Channel 0 Local Address Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
31:0	Local Address Register. This register indicates from where, in Local memory space, the DMA transfers (reads or writes) start.	Yes	Yes	0	**LAS1 + offset**

(DMASIZ0; PCI:8Ch) DMA Channel 0 Transfer Size (Bytes) Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
22:0	DMA Transfer Size (Bytes). Indicates number of bytes to transfer during DMA operation.	Yes	Yes	0	**Byte number**
31:23	Reserved.	Yes	No	0	**0.. 0**

(DMADPR0; PCI:90h) DMA Channel 0 Descriptor Pointer Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
0	Descriptor Location. Value of 1 indicates PCI Address space. Value of 0 indicates Local Address Space.	Yes	Yes	0	**1 (No local memory)**
1	End of Chain. Value of 1 indicates end of chain. Value of 0 indicates not end of chain descriptor. (Same as Non-chaining Mode.)	Yes	Yes	0	**0 or 1**
2	Interrupt after Terminal Count. Value of 1 causes interrupt to be generated after terminal count for this descriptor is reached. Value of 0 disables interrupts from being generated.	Yes	Yes	0	**0 or 1**
3	Direction of Transfer. Value of 1 indicates transfers from the Local Bus to PCI Bus. Value of 0 indicates transfers from the PCI Bus to Local Bus.	Yes	Yes	0	**0 or 1**
31:4	Next Descriptor Address. Quad word aligned (bits [3:0] = 0000).	Yes	Yes	0	**Address**

(DMAMODE1; PCI: 94h) DMA Channel 1 Mode Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
1:0	Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits.	Yes	Yes	S = 01 J = 11 C = 11	**01**
5:2	Internal Wait States (data to data).	Yes	Yes	0	**000**
6	Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.	Yes	Yes	0	**1**
7	BTERM# Input Enable. Value of 1 enables BTERM# input. Value of 0 disables BTERM# input. If set to 0, the PCI9080/9056 bursts four Lword maximum at a time.	Yes	Yes	0	**0**
8	Local Burst Enable. Value of 1 enables bursting. Value of 0 disables local bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.	Yes	Yes	0	**1**
9	Chaining. Value of 1 indicates Chaining mode is enabled. For Chaining mode, DMA source address, destination address and byte count are loaded from memory in PCI address Spaces. Value of 0 indicates Non-chaining mode is enabled.	Yes	Yes	0	**1 or 0**
10	Done Interrupt Enable. Value of 1 enables interrupt when done. Value of 0 disables interrupt when done. If DMA Clear Count mode is enabled, interrupt does not occur until byte count is cleared.	Yes	Yes	0	**1 or 0**
11	Local Addressing Mode. Value of 1 indicates Local Address LA[31:2] to be held constant. Value of 0 indicates Local Address is incremented.	Yes	Yes		**1**
12	Demand Mode. Value of 1 causes DMA controller to operate in Demand mode. In Demand mode, DMA controller transfers data when its DREQ[1:0]# input is asserted. Asserts DACK[1:0]# to indicate current Local Bus transfer is in response to DREQ[1:0]# input. DMA controller transfers Lwords (32 bits) of data. May result in multiple transfers for 8- or 16-bit bus	Yes	Yes	0	**1**
13	Write and Invalidate Mode for DMA Transfers. When set to 1, the PCI9080/9056 performs Write and Invalidate cycles to PCI Bus. The PCI9080/9056 supports Write and Invalidate sizes of 8 or 16 Lwords. Size specified in PCI Cache Line Size Register. If size other than 8 or 16 is specified, the PCI9080/9056 performs Write transfers rather than Write and Invalidate transfers. Transfers must start and end at Cache Line boundaries.	Yes	Yes	0	**0**
14	DMA EOT (End of Transfer) Enable. Value of 1 enables EOT[1:0]# input pin. Value of 0 disables EOT[1:0]# input pin.	Yes	Yes	0	**0**

Bit	Description	Read	Write	Value after Reset	Value in DM35520
	(EOT0# or EOT1#) Input.")				
15	DMA Stop Data Transfer Mode. Value of 0 sends BLAST to terminate DMA transfer. Value of 1 indicates EOT asserted or DREQ[1:0]# de-asserted during Demand mode DMA terminates a DMA transfer. (Refer to Section 3.7.6.1, "End of Transfer (EOT0# or EOT1#) Input.")	Yes	Yes	0	**0**
16	DMA Clear Count Mode. When set to 1, if it is in Local memory, byte count in each chaining descriptor is cleared when corresponding DMA transfer completes. **Note:** If the chaining descriptor is in PCI memory, the count is not cleared. (This is the DM35520 situation)	Yes	Yes	0	**0**
17	DMA Channel 0 Interrupt Select. Value of 1 routes DMA Channel 0 interrupt to PCI interrupt. Value of 0 routes DMA Channel 0 interrupt to Local Bus interrupt.	Yes	Yes	0	**1**
31:18	Reserved.	Yes	No	0	**0.. 0**

(DMAPADR1; PCI:98h) DMA Channel 1 PCI Address Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
31:0	PCI Address Register. This register indicates from where, in PCI memory space, the DMA transfers (reads or writes) start.	Yes	Yes	0	**PCI Data Buffer Address**

(DMALADR0; PCI:9Ch) DMA Channel 1 Local Address Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
31:0	Local Address Register. This register indicates from where, in Local memory space, the DMA transfers (reads or writes) start.	Yes	Yes	0	**40000000.. 4000000C**

(DMASIZ0; PCI:A0h) DMA Channel 1 Transfer Size (Bytes) Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
22:0	DMA Transfer Size (Bytes). Indicates number of bytes to transfer during DMA operation.	Yes	Yes	0	**Byte number**
31:23	Reserved.	Yes	No	0	**0.. 0**

(DMADPR0; PCI:A4h) DMA Channel 1 Descriptor Pointer Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
0	Descriptor Location. Value of 1 indicates PCI Address space. Value of 0 indicates Local Address Space.	Yes	Yes	0	**1 (No local memory)**
1	End of Chain. Value of 1 indicates end of chain. Value of 0 indicates not end of chain descriptor. (Same as Non-chaining Mode.)	Yes	Yes	0	**0 or 1**
2	Interrupt after Terminal Count. Value of 1 causes interrupt to be generated after terminal count for this descriptor is reached. Value of 0 disables interrupts from being generated.	Yes	Yes	0	**0 or 1**
3	Direction of Transfer. Value of 1 indicates transfers from the Local Bus to PCI Bus. Value of 0 indicates transfers from the PCI Bus to Local Bus.	Yes	Yes	0	**0 or 1**
31:4	Next Descriptor Address. Quad word aligned (bits [3:0] = 0000).	Yes	Yes	0	**Address**

(DMACSR0; PCI:A8h) DMA Channel 0 Command/Status Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520

Bit	Description	Read	Write	Value after Reset	Value in DM35520
0	Channel 0 Enable. Value of 1 enables channel to transfer data. Value of 0 disables channel from starting DMA transfer and if in process of transferring data suspend transfer (pause).	Yes	Yes	0	**0 or 1**
1	Channel 0 Start. Value of 1 causes channel to start transferring data if channel is enabled.	Yes	Yes/Set	0	**0 or 1**
2	Channel 0 Abort. Value of 1 causes channel to abort current transfer. Channel Enable bit must be cleared. Channel Complete bit is set when abort is complete.	Yes	Yes/Set	0	**0 or 1**
3	Clear Interrupt. Writing 1 to this bit clears Channel 0 interrupts.	Yes	Yes/Clr	0	**0 or 1**
4	Channel 0 Done. Value of 1 indicates channel's transfer is complete. Value of 0 indicates channel's transfer is not complete.	Yes	No	1	**-**
7:5	Reserved.	Yes	No	0	**-**

(DMACSR1; PCI:A9h) DMA Channel 1 Command/Status Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
0	Channel 0 Enable. Value of 1 enables channel to transfer data. Value of 0 disables channel from starting DMA transfer and if in process of transferring data suspend transfer (pause).	Yes	Yes	0	**0 or 1**
1	Channel 0 Start. Value of 1 causes channel to start transferring data if channel is enabled.	Yes	Yes/Set	0	**0 or 1**
2	Channel 0 Abort. Value of 1 causes channel to abort current transfer. Channel Enable bit must be cleared. Channel Complete bit is set when abort is complete.	Yes	Yes/Set	0	**0 or 1**
3	Clear Interrupt. Writing 1 to this bit clears Channel 0 interrupts.	Yes	Yes/Clr	0	**0 or 1**
4	Channel 0 Done. Value of 1 indicates channel's transfer is complete. Value of 0 indicates channel's transfer is not complete.	Yes	No	1	**-**
7:5	Reserved.	Yes	No	0	**-**

(DMAARB; PCI:ACh) DMA Arbitration Register

Same as Mode/Arbitration register (MARBR) at address PCI:08h.

(DMATHR; PCI:B0h) DMA Threshold Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
3:0	0 DMA Channel 0 PCI-to-Local Almost Full (C0PLAF). Number of full entries (divided by two, minus one) in the FIFO before requesting Local Bus for writes. (C0PLAF+1) + (C0PLAE+1) should be £ FIFO Depth of 32.	Yes	Yes	0	3:0
7:4	DMA Channel 0 Local-to-PCI Almost Empty (C0LPAE). Number of empty entries (divided by two, minus one) in the FIFO before requesting Local Bus for reads.(C0LPAF+1) + (C0LPAE+1) should be £ FIFO depth of 32.	Yes	Yes	0	7:4
11:8	DMA Channel 0 Local-to-PCI Almost Full (C0LPAF). Number of full entries (divided by two, minus one) in the FIFO before requesting PCI Bus for writes.	Yes	Yes	0	11:8
15:12	DMA Channel 0 PCI-to-Local Almost Empty (C0PLAE). Number of empty entries (divided by two, minus one) in the FIFO before requesting PCI Bus for reads.	Yes	Yes	0	15:12
19:16	DMA Channel 1 PCI-to-Local Almost Full (C1PLAF). Number of full entries(minus one) in the FIFO before requesting Local Bus for writes. (C1PLAF+1) + (C1PLAE+1) should be £ FIFO depth of 16.	Yes	Yes	0	19:16
23:20	DMA Channel 1 Local-to-PCI Almost Empty (C1LPAE). Number of empty entries (minus one) in the FIFO before requesting Local Bus for reads. (C1PLAF) + (C1PLAE) should be £ FIFO depth of 16.	Yes	Yes	0	23:20
27:24	DMA Channel 1 Local-to-PCI Almost Full (C1LPAF). Number of full entries (minus one) in the FIFO before requesting PCI Bus for writes.	Yes	Yes	0	27:24
31:28	DMA Channel 1 PCI-to-Local Almost Empty (C1PLAE). Number of empty entries (minus one) in the FIFO before requesting PCI Bus for reads.	Yes	Yes	0	31:28

Note: If the number of entries needed is x, then the value is one less than half the number of entries (DMA Channel 0 only).

5.8 Interrupts

This chapter explains the possible interrupt sources and the priority Interrupt Controller of the board.

Because of the several interrupt sources on the board a Priority Interrupt Controller was built on the board. This controller assures even usage all of the interrupt sources on the board.

5.8.1 The Overall Interrupt Structure of DM35520

The Interrupt Sources of DM35520

The DM35520 PCI interrupt can be generated one of the following:

- The On-board Priority Interrupt Controller
- DMA Ch 0/Ch 1 Done
- DMA Ch 0/Ch 1 Terminal Count reached

INTA#, or individual sources of an interrupt, can be enabled or disabled with the PCI9080/9056 Interrupt Control/Status register (INTCSR). This register also provides interrupt status for each interrupt source. The PCI9080/9056 PCI Bus interrupt is level output. Disabling an Interrupt Enable bit or clearing the cause(s) of the interrupt can clear an interrupt.

The On Board Priority Interrupt Controller
The On-board Priority Interrupt controller can assert the Local Bus input pin. Asserting Local Bus input pin LINTi# can generate a PCI Bus interrupt. PCI Host processor can read the PCI9080/9056 Interrupt Control/Status register to determine that an interrupt is pending due to the LINTi# pin being asserted. The interrupt remains asserted as long as the LINTi# pin is asserted and the Local interrupt input is enabled. Clearing the Interrupt Request Register (LAS0+034h) can be taken by the PCI Host processor to cause the Local Bus to release LINTi#.

DMA Channel 0/1 Interrupts
A DMA channel can generate a PCI interrupt when done (transfer complete) or after a transfer is complete for a descriptor in Chaining mode. A bit in the DMA mode register determines whether to generate a PCI or Local interrupt. (The Local interrupt does not make sense because there is no Local Processor) The PCI processor can then read the PCI9080/9056 Interrupt Control/Status register (INTCSR) to determine whether a DMA channel interrupt is pending. A Done Status Bit in the Control/Status register can be used to determine whether the interrupt is

- a done interrupt
- the result of a transfer for a descriptor in a chain that is not yet complete

The mode register of a channel enables a Done Interrupt. In Chaining mode, a bit in the Next Descriptor Pointer register of the channel specifies whether to generate an interrupt at the end of the transfer for the current descriptor. A DMA channel interrupt is cleared by writing a 1 to the Clear Interrupt bit in the DMA Command/Status register (DMACSR0[3] and DMACSR1[3])

The Interrupt Registers of DM35520

The DM35520 has two Interrupt register groups. The first is inside the PCI9080/9056 Interface chip the other is inside the Control Logic of the board.

The PCI9080/9056 Interrupt Control/Status Register is at the PCI:68h address: INTCSR:

Table 27: Interrupt Control/Status Register

Bit	Description	Read	Write	Value after Reset	Value in DM35520
0	Enable Local Bus LSERR#. Value of 1 enables the PCI9080/9056 to assert LSERR# interrupt output when PCI Bus Target Abort or Master Abort Status bit is set in PCI Status Configuration register.	Yes	Yes	0	0
1	Enable Local Bus LSERR# when PCI parity error occurs during a PCI9080/9056 Master Transfer or a PCI9080/9056 Slave access or an Outbound Free List FIFO Overflow Init.	Yes	Yes	0	0
2	Generate PCI Bus SERR# When this bit is set to 0, writing 1 generates PCI bus SERR #.	Yes	Yes	0	0
3	Mailbox Interrupt Enable. Value of 1 enables a Local interrupt to be generated when PCI Bus writes to Mailbox registers 0 through 3. To clear a Local interrupt, the Local Master must read the Mailbox. Used in conjunction with Local interrupt enable.	Yes	Yes	0	0
7:4	Reserved.	Yes	No	0	0

Bit	Description	Read	Write	Value after Reset	Value in DM35520
8	PCI Interrupt Enable. Value of 1 enables PCI interrupts.	Yes	Yes	1	1
9	PCI Doorbell Interrupt Enable. Value of 1 enables doorbell interrupts. Used in conjunction with PCI interrupt enable. Clearing doorbell interrupt bits that caused interrupt also clears interrupt.	Yes	Yes	0	0
10	PCI Abort Interrupt Enable. Value of 1 enables Master abort or Master detect of Target abort to generate PCI interrupt. Used in conjunction with PCI interrupt enable. Clearing abort status bits also clears PCI interrupt.	Yes	Yes	0	0
11	PCI Local Interrupt Enable. Value of 1 enables Local interrupt input to generate a PCI interrupt. Use in conjunction with PCI interrupt enable. Clearing the Local Bus cause of interrupt also clears interrupt.	Yes	Yes	0	1
12	Retry Abort Enable. Value of 1 enables the PCI9080/9056 to treat 256 Master consecutive retries to a Target as a Target Abort. Value of 0 enables the PCI9080/9056 to attempt Master Retries indefinitely. **Note:** For diagnostic purposes only.	Yes	Yes	0	0
13	Value of 1 indicates PCI doorbell interrupt is active.	Yes	Yes	0	0
14	Value of 1 indicates PCI abort interrupt is active	Yes	Yes	0	0
15	Value of 1 indicates Local interrupt is active (LINTi#).	Yes	Yes	0	0
16	Local Interrupt Output Enable. Value of 1 enables Local interrupt output.	Yes	Yes	1	0
17	Local Doorbell Interrupt Enable. Value of 1 enables doorbell interrupts. Used in conjunction with Local interrupt enable. Clearing local doorbell interrupt bits that caused interrupt also clears interrupt.	Yes	Yes	0	0
18	Local DMA Channel 0 Interrupt Enable. Value of 1 enables DMA Channel 0 interrupts. Used in conjunction with Local interrupt enable. Clearing DMA status bits also clears interrupt.	Yes	Yes	0	0 or 1
19	Local DMA Channel 1 Interrupt Enable. Value of 1 enables DMA Channel 1 interrupts. Used in conjunction with Local interrupt enable. Clearing DMA status bits also clears interrupt.	Yes	Yes	0	0
20	Value of 1 indicates local doorbell interrupt is active.	Yes	No	0	0
21	Value of 1 indicates DMA Ch 0 interrupt is active.	Yes	No	0	0
22	Value of 1 indicates DMA Ch 1 interrupt is active.	Yes	No	0	0
23	Value of 1 indicates BIST interrupt is active. Writing 1 to bit 6 of PCI Configuration BIST Register generates BIST (Built-In Self-Test) interrupt. Clearing bit 6 clears interrupt. For description of self-test, refer to PCI BISTR.	Yes	No	0	0
24	Value of 0 indicates Direct Master was Bus Master during a Master or Target abort. (Not valid until abort occurs.)	Yes	No	1	1
25	Value of 0 indicates DMA CH 0 was Bus Master during a Master or Target abort. (Not valid until abort occurs.)	Yes	No	1	1
26	Value of 0 indicates DMA CH 1 was Bus Master during a Master or Target abort. (Not valid until abort occurs.)	Yes	No	1	1
27	Value of 0 indicates Target Abort was generated by the PCI9080/9056 after 256 consecutive Master retries to Target. (Not valid until abort occurs.)	Yes	No	1	1
28	Value of 1 indicates PCI wrote data to MailBox #0. Enabled only if MBOXINTENB is enabled (bit 3 high).	Yes	No	0	N/A
29	Value of 1 indicates PCI wrote data to MailBox #1. Enabled only if MBOXINTENB is enabled (bit 3 high).	Yes	No	0	N/A
30	Value of 1 indicates PCI wrote data to MailBox #2. Enabled only if MBOXINTENB is enabled (bit 3 high).	Yes	No	0	N/A
31	Value of 1 indicates PCI wrote data to MailBox #3. Enabled only if MBOXINTENB is enabled (bit 3 high).	Yes	No	0	N/A

The other group of interrupt registers are the on-board, priority interrupt, controller registers of he board (LAS0 + 030h.. 038h).

5.8.2 The Operation of On-board Priority Interrupt Controller

After power-up all of the interrupt sources are disabled on the board. In this state place your Interrupt Service Routine which will be used in the case of an interrupt generated by the board.

The initialization process of the controller is:

- Set all bits to 1 in the Interrupt Clear Mask Register.
- Read a dummy data from Clear Interrupt set by Clear Mask address. These two steps means that all Interrupt requests are cleared
- Write Interrupt mask register. If an interrupt source must be used, that position in the register must be set to 1.

After this initialization process the Interrupt Controller receives the interrupt requests, and according to their priority order transmits them to the PC. One time one request.

In the Interrupt service routine you must identify the current interrupt source reading by (INTCSR; PCI:68h) Interrupt Control/Status Register of PCI9080/9056, and then the Interrupt Status Register of on-board Priority Interrupt Controller. The INTCSR description can be found in the Chapter 8.1.2. In the on-board priority register there is a position where the bit is high, signaling the active interrupt source from the priority interrupt sources. All of the other bits are zero. Identifying the source, it can be serviced. After servicing, the request must be cleared by accessing the Interrupt clear mask and the Clear Interrupt set by Clear Mask registers.

In the normal operation, the next interrupt request comes later than clearing of the previous. If this is override, it can be detected by the Interrupt Overrun register. If the interrupts serviced in time all bits are zeros in the overrun register. If a new interrupt request comes before the previous has been serviced and the request is cleared, the appropriate overrun bit goes into high signaling the faulty - too slow interrupt service - operation.

5.8.3 Advanced Digital Interrupts

The bit programmable digital I/O circuitry supports two Advanced Digital Interrupt modes, event mode or match mode. These modes are used to monitor digital input lines (P0..7) for state changes. The mode is selected at LAS0+7Ch, B3 and enabled at LAS0+7Ch, B4.

Event Mode

When enabled, this mode samples the Port 0 input lines at a specified clock rate (using the 8 MHz system clock or a programmable clock in User TC Counter 1), looking for a change in state in any one of the eight bits. When a change of state occurs, an interrupt is generated and the input pattern is latched into the Compare Register. You can read the contents of this register at LAS0+78h (LAS0+7C bits 1 and 0 set to 11) to see which bit caused the interrupt to occur. Bits can be masked and their state changes ignored by programming the Mask Register with the mask at LAS0+78h (LAS0+7C bits 1 and 0 set to 10).

Match Mode

When enabled, this mode samples the Port 0 input lines at a specified clock rate (using the 8 MHz system clock or a programmable clock in User TC Counter 1) and compares all input states to the value programmed in the Compare Register at LAS0+78h (LAS0+7C bits 1 and 0 set to 11). When the states of all of the lines match the value in the Compare Register, an interrupt is generated. Bits can be masked and their states ignored by programming the Mask Register with the mask at LAS0+78h (LAS0+7C bits 1 and 0 set to 10).

Sampling Digital Lines for Change of State

In the Advanced Digital Interrupt modes, the digital lines are sampled at a rate set by the 8 MHz system clock or the clock programmed in User TC Counter 1. With each clock pulse, the digital circuitry looks at the state of the next Port 0 bits. To provide noise rejection and prevent erroneous interrupt generation because of noise spikes on the digital lines, a change in the state of any bit must be seen for two edges of a clock pulse to be recognized by the circuit.

5.9 Timer/Counters

The Timer/Counter section contains internal TCs in the Control EPLD and 8254 programmable interval timers for User Timer Counter.

5.9.1 The Internal Timer Timer/Counters

The internal Timer Counters works similar to the 8254 in rate mode. The DM35520 has 8 internal timer/counter:

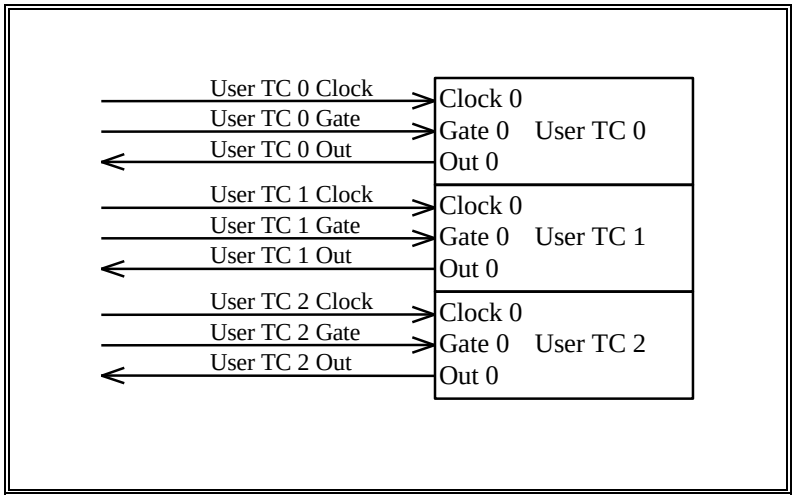
1. Pacer Clock - 24bit - Clock Signal is 8/20 MHz
2. Burst Clock - 16bit - Clock Signal is 8MHz
3. A/D Sample counter - 16 bit - Clock signal can be programmed
4. D/A1 Update counter – 16 bit - Clock signal is D/A1 update
5. D/A2 Update counter - 16 bit - Clock signal is D/A2 update
6. Delay Counter - 16 bit - Clock signal can be programmed
7. About Counter - 16 bit - Clock signal can be programmed
8. D/A Clock – 24 bit - Clock Signal is 8MHz

5.9.2 User Timer Timer/Counters

The 8254 is the User TC. All three counters on this chip are available for user functions. For details on the programming modes of the 8254, see the data sheet in Appendix.

Each timer/counter has two inputs, CLK in and GATE in, and one output, timer/counter OUT. They can be programmed as binary or BCD down counters by writing the appropriate data to the command word, as described in the I/O map discussion in 5.4. See Figure 18. The sources of the user TC clocks and gates can be programmed by User Timer address area is the LAS0+1A0... 1B4. It is important, that the registers of the Timer Counter can be accessed by byte wide instructions. The 16 bit wide word must be created from the bytes.

Figure 18: User Timer/Counter



The timers can be programmed to operate in one of six modes, depending on your application. The following paragraphs briefly describe each mode.

Mode 0, Event Counter (Interrupt on Terminal Count)
This mode is typically used for event counting. While the timer/counter counts down, the output is low, and when the count is complete, it goes high. The output stays high until a new Mode 0 control word is written to the timer/counter.

Mode 1, Hardware-Retriggerable One-Shot
The output is initially high and goes low on the clock pulse following a trigger to begin the one-shot pulse. The output remains low until the count reaches 0, and then goes high and remains high until the clock pulse after the next trigger.

Mode 2, Rate Generator
This mode functions like a divide-by-N counter and is typically used to generate a real-time clock interrupt. The output is initially high, and when the count decrement to 1, the output goes low for one clock pulse. The output then goes high again, the timer/counter reloads the initial count, and the process is repeated. This sequence continues indefinitely.

Mode 3, Square Wave Mode
Similar to Mode 2 except for the duty cycle output, this mode is typically used for baud rate generation. The output is initially high, and when the count decrement to one-half its initial count, the output goes low, for the remainder of the count. The timer/counter reloads and the output goes high again. This process repeats indefinitely.

Mode 4, Software-Triggered Strobe
The output is initially high. When the initial count expires, the output goes low for one clock pulse and then goes high again. Counting is "triggered" by writing the initial count.

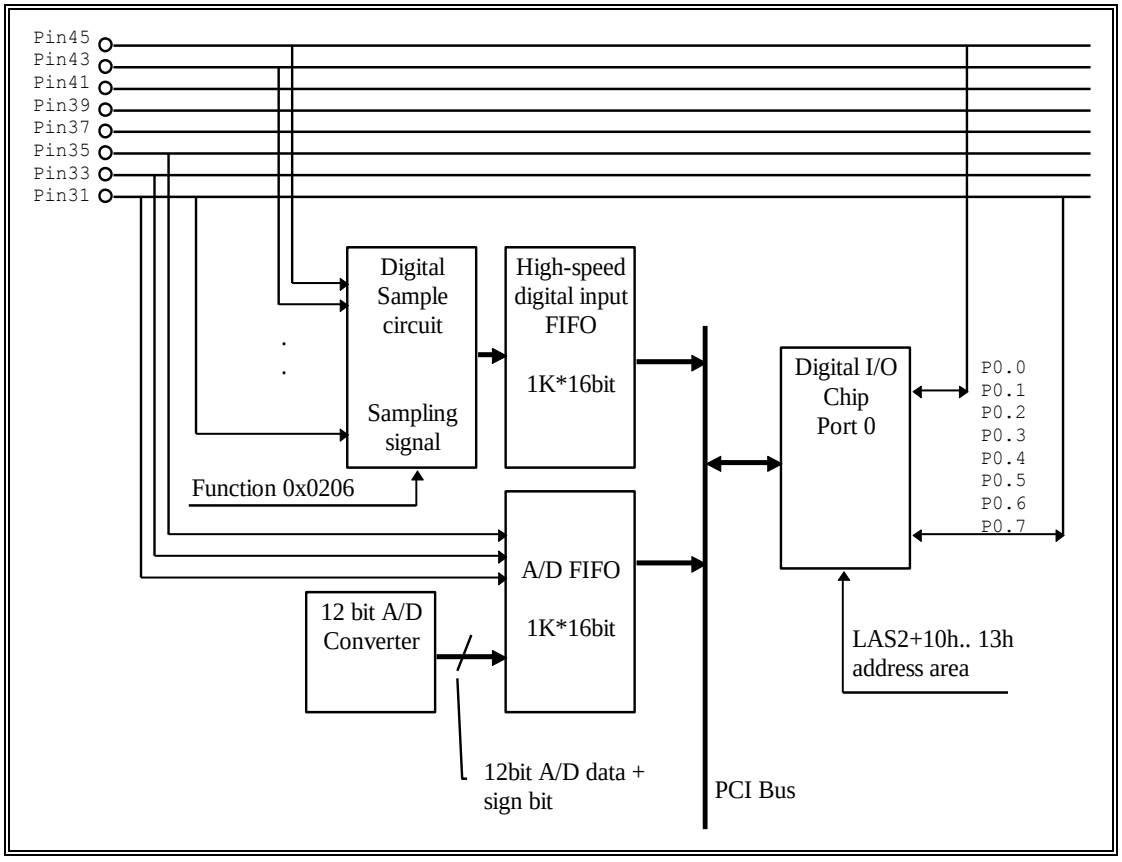
Mode 5, Hardware Triggered Strobe (Retriggerable)
The output is initially high. Counting is triggered by the rising edge of the gate input. When the initial count has expired, the output goes low for one clock pulse and then goes high again

5.10 Digital I/O

The DM35520 has several digital lines to receive and transmit digital data from, or to the external digital world. This chapter describes only the 31...46 pins of External I/O connector. These 16 Digital Input/Output lines are multifunction and assure a flexible connection with the digital world.

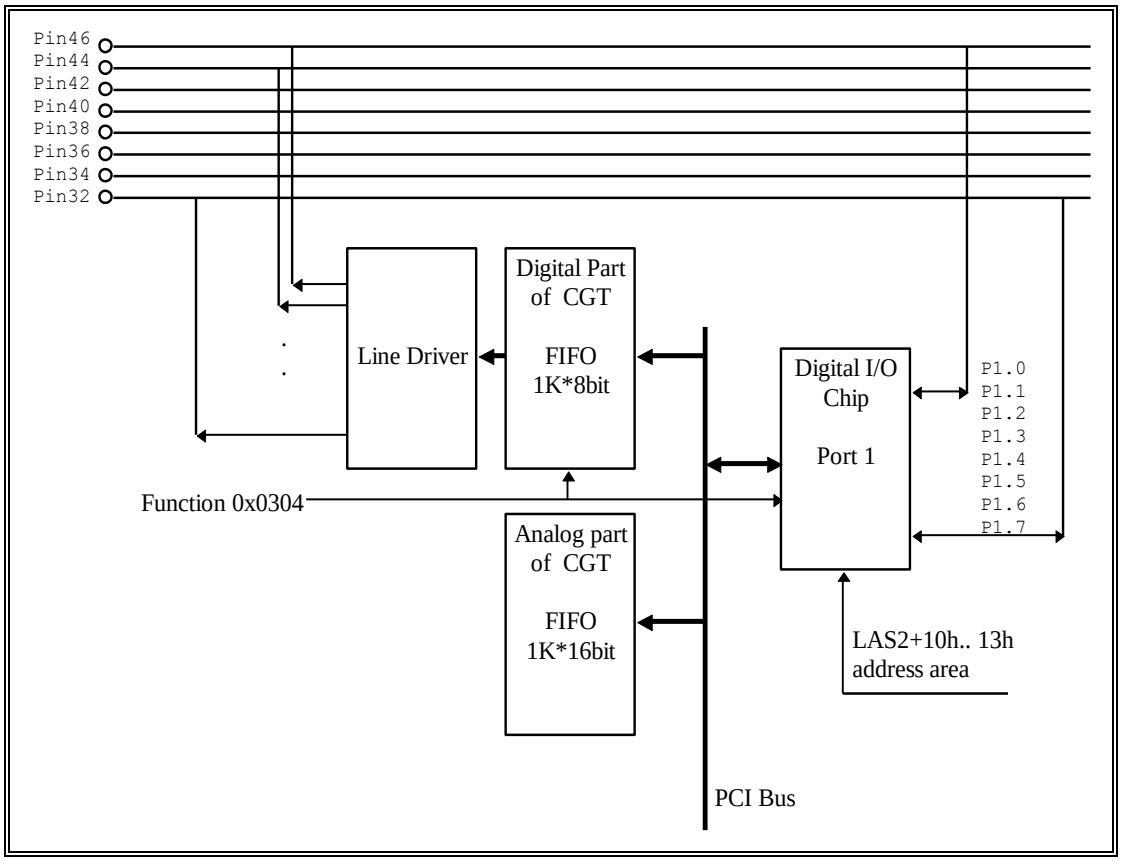
The connections of odd numbered pins are shown in the Figure 19. These lines are monitored by the high-speed digital input circuitry, and the least significant three bits of the A/D FIFO as data markers, therefore these lines can be read or driven by the Port 0 of Digital I/O Chip.

Figure 19: Digital I/O Port 0



The connections of even numbered pins are shown in the Figure 20. These lines can be driven by the digital part of the CGT; therefore these lines can be read or driven by the Port 1 of Digital I/O Chip.

Figure 20: Digital I/O Port 1



5.10.1 The Digital I/O Chip

The DM35520 has 16 buffered TTL/CMOS digital I/O lines available for digital control applications. These lines are grouped in two 8-bit ports. The sixteen bits in Port 0 can be independently programmed as input or output. Port 1 can be programmed as 8-bit input or output ports. These lines are grouped in digital I/O chip with sixteen lines. The Digital I/O chip is addressed at LAS0 + 070h... LAS0 + 07Fh.

All digital inputs are pulled up to +5V by 10kΩ resistors. All digital outputs are terminated by series 10Ω resistors.

Port 0, Bit Programmable Digital I/O

The eight Port 0 digital lines are individually set for input or output by writing to the Direction Register at LAS0 + 078h. The input lines are read and the output lines are written at LAS0 + 070h.

Advanced Digital Interrupts: Mask and Compare Registers

The Port 0 bits support two Advanced Digital Interrupt modes. An interrupt can be generated when the data read at the port matches the value loaded into the Compare Register. This is called a match interrupt. Or, an interrupt can be generated whenever any bit changes state. This is an event interrupt. For either interrupt, bits can be masked by setting the corresponding bit in the Mask Register high. In a digital interrupt mode, this masks out selected bits when monitoring the bit pattern for a match or event. In normal operation where the Advanced Digital Interrupt mode is not activated, the Mask Register can be used to preserve a bit's state, regardless of the digital data written to Port 0.

When using event interrupts, you can determine which bit caused an event interrupt to occur by reading the contents latched into the Compare Register.

Port 1, Port Programmable Digital I/O

The direction of the eight bit Port 1 digital lines is programmed at LAS0 + 07Ch, bit 2. These lines are configured as all inputs or all outputs, with their states read and written at LAS0 + 074h.

Resetting the Digital Circuitry

When a digital chip clear (LAS0 + 07Ch bits 1 and 0 = 00 followed by a write to LAS0 + 078h), Software Reset of the board (Function 0x000F), all of the digital I/O lines are set up as inputs.

Strobing Data into Port 0

When not in an Advanced Digital Interrupt mode, external data can be strobed into Port 0 by connecting a trigger pulse through the External Pacer Clock pin at the External I/O Connector. This data can be read from the Compare Register at LAS0 + 078h.

5.10.2 High-Speed Digital Input

As you can see in the Figure 19, the Pin 31...45 digital pins of external I/O connector can be sampled by high-speed digital input circuitry. The sampling signal can be selected by the Function 0x0206. Samples are written automatically into the high-speed digital input FIFO. The status bits of FIFO can be monitored at the address LAS0+8h.

If you want to get an interrupt at a required number of samples in the FIFO, use User Timer Counter 1 as high speed digital input sample counter. Select the high-speed digital input sampling signal as clock of user TC1 by the Function 0x0702.

All digital inputs are pulled up to +5V by 10kΩ resistors.

5.10.3 Digital Input Data Markers

As you can see in the Figure 19, the digital pin 31, 33, 35 can be sampled nearly simultaneously with the analog input signal by the A/D FIFO. The delay time between the analog input sampling and the digital input sampling is app. 800 ns. If you want to sample the digital lines with the analog lines really simultaneously, use the high-speed digital input with A/D Conversion Signal as sampling signal of high-speed digital input.

All digital inputs are pulled up to +5V by 10kΩ resistors.

5.11 Calibration

This chapter tells you how to calibrate the DM35520 using the trim pots on the board. These trim pots calibrate the A/D converter gain and offset, and the D/A outputs.

This chapter tells you how to calibrate the A/D converter gain and offset, and the D/A output multiplier. The offset and full-scale performance of the board's A/D and D/A converters is factory-calibrated. Any time you suspect inaccurate readings, you can check the accuracy of your conversions using the procedure below, and make adjustments as necessary.

Calibration is done with the board installed in your system. You can access the trim pots at the top edge of the board. Power up the system and let the board circuitry stabilize for 15 minutes before you start calibrating.

5.11.1 SDM35540 Calibration

The SDM35540 is an auto-calibrating board that does not require any trim pot adjustments. Upon first time boot the board loads factory default values. After invoking the calibration command (see 0xB0 register) the board recalibrates and stores these new calibration values into the EEPROM. Each time the user calibrates these old values are overwritten with the new values. The user can go back to default factory values by writing the appropriate command to the DSP Command register(see 0xB0 register). All analog paths (A/D, D/A1 and D/A2) will be calibrated. The user can perform calibration at will or based on the readings of an on-board temperature sensor. **During calibration the D/A board outputs will be grounded and disconnected from the DACs. Upon auto-calibration completion the D/A FIFOs will be cleared and the D/A outputs will be in the bipolar 5V range (+/- 5V), with the output of the DACs set to zero volts. The user does have the option to pass a value to the DAC and upon completion of calibration the DAC will be restored to that value.**

5.11.2 Required Equipment

The following equipment is required for calibration:

- Precision Voltage Source: -10 to +10 volts
- Digital Voltmeter: 5-1/2 digits
- Small Screwdriver (for trim pot adjustment)

5.11.3 DM35520 A/D Calibration

Two procedures are used to calibrate the A/D converter for all input voltage ranges. The first procedure calibrates the converter for the bipolar ranges (±5, ±10 volts), and the second procedure calibrates the unipolar range (0 to +10 volts). Table 30 shows the ideal input voltage for each bit weight for the bipolar ranges, and Table 32 shows the ideal voltage for each bit weight for the unipolar range.

Bipolar Calibration

Bipolar Range Adjustments: -5 to +5 Volts

Two adjustments are made to calibrate the A/D converter for the bipolar range of +/-5 volts. One is the offset adjustment, and the other is the full scale, or gain, adjustment. Trim pot TR4 is used to make the offset adjustment, and trim pot TR5 is used for gain adjustment. Before making these adjustments, make sure that the board is programmed for a range of ±5 volts.

Use analog input channel 1 and set it for a gain of 1 while calibrating the board. Connect your precision voltage source to channel 1. Set the voltage source to -1.22070 millivolts, start a conversion, and read the resulting data. Adjust trim pot TR4 until the reading flickers between the values listed in the table below. Next, set the voltage to -4.99878 volts, and repeat the procedure, this time adjusting TR5 until the data flickers between the values in the table.

Table 28: Bipolar Offset and Gain Adjustment

Data Values for Calibrating Bipolar 10 Volt Range (-5 to +5 volts)		
	Offset(TR4) Input Voltage = -1.22mV	Converter Gain(TR5) Input Voltage = -4.99878V
A/D Converted Data	0000 0000 0000 1111 1111 1111	0000 0000 0000 1000 0000 0001

Bipolar Range Adjustments: -10 to +10 Volts

To adjust the bipolar 20-volt range (-10 to +10 volts), program the board for ± 10 volt input range. Then, set the input voltage to +5.0000 volts and adjust TR2 until the output matches the data in the table below.

Table 29: 20V Range Adjustment

Data Values for Calibrating Bipolar 20 Volt Range (-10 to +10 volts)	
	TR2 Input Voltage = +5.0000V
A/D Converted Data	0100 0000 0000

Below is a table listing the ideal input voltage for each bit weight for the bipolar ranges.

Table 30: Bipolar ADC Bit Weight

A/D Converter Bit Weights, Bipolar			
SIGN	A/D Bit Weight	Ideal Input Voltage(millivolts)	
		±5V	±10V
1	1111 1111 1111	-2.44	-4.88
1	1000 0000 0000	-5000.00	-10000.00
0	0100 0000 0000	+2500.00	+5000.00
0	0010 0000 0000	+1250.00	+2500.00
0	0001 0000 0000	+625.00	+1250.00
0	0000 1000 0000	+312.50	+625.00
0	0000 0100 0000	+156.25	+312.50
0	0000 0010 0000	+78.13	+156.25
0	0000 0001 0000	+39.06	+78.13
0	0000 0000 1000	+19.53	+39.06
0	0000 0000 0100	+9.77	+19.53
0	0000 0000 0010	+4.88	+9.77
0	0000 0000 0001	+2.44	+4.88
0	0000 0000 0000	0.00	0.00

Common Mode Calibration

Do not attempt to adjust TR1 or TR3. If you adjust them, please send the board back for RMA so we can adjust the board back in. TR1 is the common mode gain adjustment and TR3 is the common mode offset adjustment. These settings are very sensitive and should not be adjusted by the end user.

Unipolar Calibration

One adjustment is made to calibrate the A/D converter for the unipolar range of 0 to +10 volts. Trim pot TR6 is used to make the offset adjustment. This calibration procedure is performed with the module programmed for a 0 to +10 volt input range. Before making these adjustments, make sure that the module is programmed properly and has been calibrated for the bipolar ranges.

Use analog input channel 1 and set it for a gain of 1 while calibrating the board. Connect your precision voltage source to channel 1. Set the voltage source to +1.22070 millivolts, start a conversion, and read the resulting data. Adjust trim pot TR6 until the data flickers between the values listed in the table below.

Table 31: Unipolar Offset Adjustment

Data Values for Calibrating Unipolar 10 Volt Range (0 to +10 volts)	
	TR6 Input Voltage = +1.22070mV
A/D Converted Data	0000 0000 0000 0000 0000 0001

Below is a table listing the ideal input voltage for each bit weight for the unipolar range.

Table 32: Unipolar ADC Bit Weight

A/D Converter Bit Weights, Bipolar		
SIGN	A/D Bit Weight	Ideal Input Voltage(millivolts)
		0 to +10V
0	1111 1111 1111	+9997.6
0	1000 0000 0000	+5000.00
0	0100 0000 0000	+2500.00
0	0010 0000 0000	+1250.00
0	0001 0000 0000	+625.00
0	0000 1000 0000	+312.50
0	0000 0100 0000	+156.25
0	0000 0010 0000	+78.125
0	0000 0001 0000	+39.063
0	0000 0000 1000	+19.531
0	0000 0000 0100	+9.77656
0	0000 0000 0010	+4.8828
0	0000 0000 0001	+2.4414
0	0000 0000 0000	0.00

Gain Adjustment

Should you find it necessary to check any of the programmable gain settings, the following table will show the proper trim pot to adjust. If the gain of one calibration is off, all the other gains will also be off, so make sure gain of one is properly adjusted first.

Set your mode to either unipolar or bipolar and input the highest voltage your mode requires. i.e. 10V or 20V. What this step does is accentuate any gain errors present. The following trim pots should already be very close to accurate, so make small adjustments.

Table 33: Gain Calibration

Calibrating Gains	
Gain	Trim pot
X2	TR7
X4	TR8
X8	TR9
X16	TR10
X32	TR11

DM35520 D/A Calibration

The D/A circuit require no calibration for the 0 to +5 and ±5 volts ranges. The following paragraph describes the calibration procedure for the 0 to +10 and ±10 volt ranges.

To calibrate for the 0 to +10 and ±10 volt ranges, program the DAC outputs for a 0 to +10 volt range. Now program the D/A outputs with a digital value of 2048. The ideal D/A output value for a code of 2048 is +5.000 volts. Connect a voltmeter to the D/A outputs and adjust TR14 for D/A1 and TR15 for D/A2 until 5.000 volts is read on the meter.

The following tables show the ideal output voltage per bit weight for unipolar and bipolar ranges.

D/A Bit Weight, Unipolar		
Unipolar D/A Bit Weight	Ideal Output Voltage(millivolts)	
	0 to +5 Volts	0 to +10 Volts
4095	+5000.00	+10000.00
2048	+2500.00	+5000.00
1024	+1250.00	+2500.00
512	+625.00	+1250.00
256	+312.50	+625.00
128	+156.25	+312.50
64	+78.13	+156.25
32	+39.06	+78.13
16	+19.53	+39.06
8	+9.77	+19.53
4	+4.88	+9.77
2	+2.44	+4.88
1	+1.22	+2.44
0	0.00	0.00

D/A Bit Weight, Bipolar		
Unipolar D/A Bit Weight	Ideal Output Voltage(millivolts)	
	0 to +5 Volts	0 to +10 Volts
2048	+5000.00	+10000.00
1024	+2500.00	+5000.00
512	+1250.00	+2500.00
256	+625.00	+1250.00
128	+312.50	+625.00
64	+156.25	+312.50
32	+78.13	+156.25
16	+39.06	+78.13
8	+19.53	+39.06
4	+9.77	+19.53
2	+4.88	+9.77
1	+2.44	+4.88
0	0.00	0.00
-1	-2.44	-4.88
-2	-4.88	-9.77
-4	-9.77	-19.53
-8	-19.53	-39.06
-16	-39.06	-78.13
-32	-78.13	-156.25
-64	-156.25	-312.50
-128	-312.50	-625.00
-256	-625.00	-1250.00
-512	-1250.00	-2500.00
-1024	-2500.00	-5000.00
-2048	-5000.00	-10000.00

5.12 On-board DSP (SDM35540 Only)

The SDM35540 datamModule has an on-board DSP which help the host CPU during following processes:

- Auto-calibration

The DSP is seamless, and the user doesn't need to program it to use auto-calibration.

6 Troubleshooting

If you are having problems with your system, please try the following initial steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem. Perform you troubleshooting with the least number of modules in the system possible.

- **Swap Components** – Try replacing parts in the system one at a time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087
E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

7 Additional Information

7.1 PC/104 Specifications

A copy of the latest PC/104 specifications can be found on the webpage for the PC/104 Embedded Consortium:

www.pc104.org

7.2 PCI and PCI Express Specification

A copy of the latest PCI and PCI Express specifications can be found on the webpage for the PCI Special Interest Group:

www.pcisig.com

8 The PCI Configuration Registers, Local Configuration Registers, Runtime Registers

The first part of the Appendix shows the maps of all register areas.

PCI Configuration Registers:

Configuration Address Offset	PCI Writable	Byte3	Byte2	Byte1	Byte0
00h	No	Device Identification		Vendor Identification	
04h	Yes	Status		Command	
08h	No	Class Code			Revision
0Ch	Yes (7..0)	BIST	Header Type	PCI Latency Timer	Cache Line Size
10h	Yes	PCI Base Address 0 for Memory Mapped Local Configuration Registers PCIBAR0			
14h	Yes	PCI Base Address 1 for I/O Mapped Local Configuration Registers PCIBAR1			
18h	Yes	PCI Base Address 2 for Local Address Space 0 (LAS0)			
1Ch	Yes	PCI Base Address 3 for Local Address Space 1 (LAS1)			
20h	Yes	Reserved			
24h	Yes	Reserved			
28h	No	Reserved			
2Ch	No	Subsystem ID		Subsystem Vendor ID	
30h	Yes	PCI Base Address for Local Expansion ROM			
34h	No	Reserved			
38h	No	Reserved			
3Ch	Yes(7..0)	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

Local Configuration Registers:

PCI Address Offset from Local Configuration Registers Base Address	PCI and Serial EEPROM Writable	To ensure software compatibility with other versions of the PCI9080/9056 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0
00h	Yes	LAS0RR - Range for PCI-to-Local Address Space 0
04h	Yes	LAS0BA - Local Base Address (Remap) for PCI-to-Local Address Space 0
08h	Yes	MARBR - Mode/Arbitration Register
0Ch	Yes	BIGEND - Big/Little Endian Description Register
10h	Yes	EROMRR - Range for Expansion ROM
14h	Yes	EROMBA - Local Base Address (Remap) for PCI to ROM
18h	Yes	LBRD0 - Local Address Space 0 Bus Region Description Register
1Ch	Yes	DMRR - Local Range Register for Direct Master to PCI
20h	Yes	DMLBAM - Local Base Address Register for Direct Master to PCI memory
24h	Yes	DMLBAI - Local Base Address Register for Direct Master to PCI IO/CFG
28h	Yes	DMPBAM - PCI Base Address Register for Direct Master to PCI memory
2Ch	Yes	DMCFGA - PCI Configuration Address Reg. for Direct Master to PCI IO/CFG
F0h	Yes	LAS1RR - Range for PCI-to-Local Address Space 1
F4h	Yes	LAS1BA - Local Base Address (Remap) for PCI-to-Local Address Space 0
F8h	Yes	LBRD1 - Local Address Space 1 Bus Region Description Register

Runtime Registers:

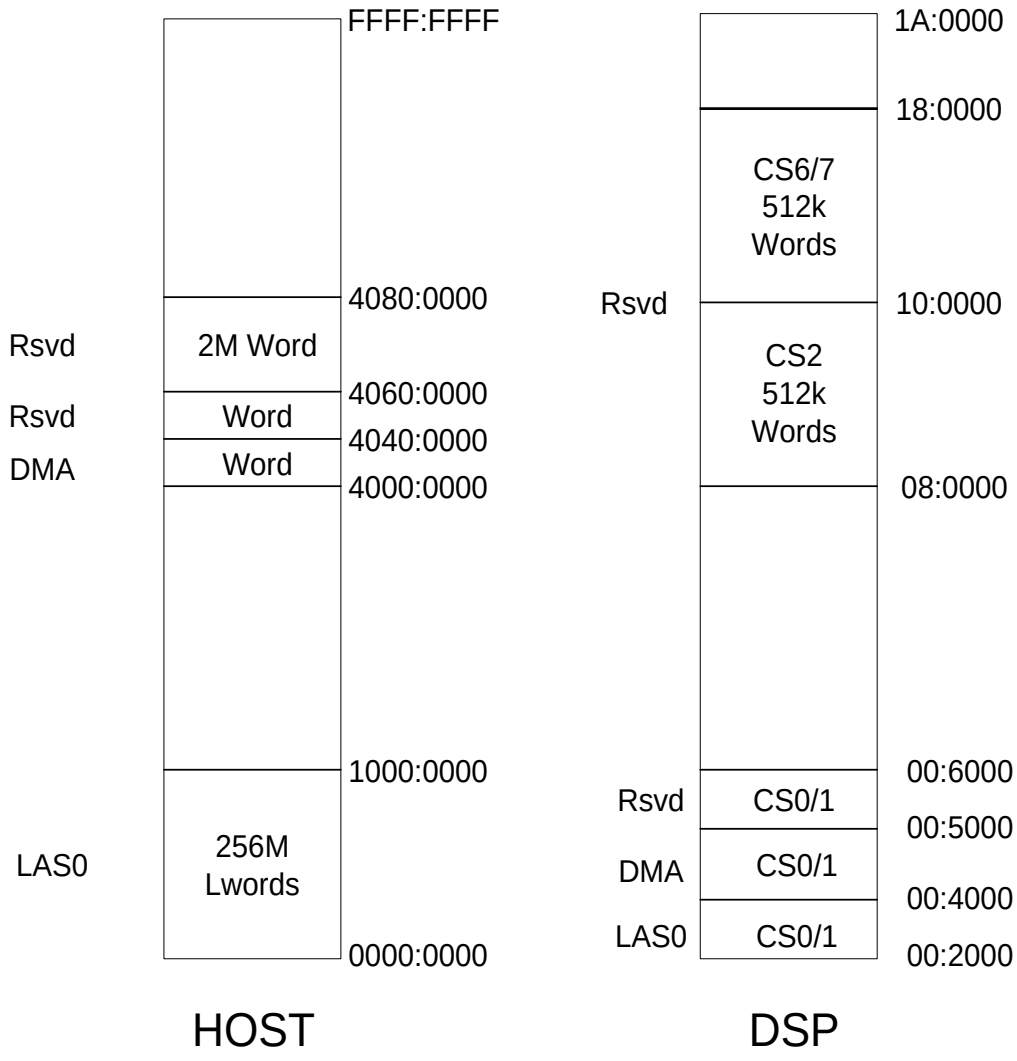
PCI (Offset from Base Address)	PCI Writable	Serial EEPROM Writable	To ensure software compatibility with other versions of the PCI9080/9056 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0
40h	Yes	Yes	Mailbox Register 0 (see Note)
44h	Yes	Yes	Mailbox Register 1 (see Note)
48h	Yes	No	Mailbox Register 2
4Ch	Yes	No	Mailbox Register 3
50h	Yes	No	Mailbox Register 4
54h	Yes	No	Mailbox Register 5
58h	Yes	No	Mailbox Register 6
5C	Yes	No	Mailbox Register 7
60h	Yes	No	PCI-to-Local Doorbell Register
64h	Yes	No	Local-to-PCI Doorbell Register
68h	Yes	No	Interrupt Control / Status
6Ch	Yes	No	Serial EEPROM Control, PCI Command Codes, User I/O Control, Init Control
70h	No	No	Device ID / Vendor ID
74h	No	No	Unused / Revision ID
78h	Yes	No	Mailbox Register 0 (see Note)
7Ch	Yes	No	Mailbox Register 1 (see Note)

Note: Mailbox registers 0 and 1 are always accessible at addresses 78h/C0h and 7Ch/C4. When the I2O feature is disabled (QSR[0]=0), Mailbox registers 0 and 1 are also accessible at PCI Addresses 40h and 44h for PCI9060 compatibility. When the I2O feature is enabled, the Inbound and Outbound Queue pointers are accessed at addresses40h and 44h, replacing the Mailbox registers in PCI Address space.

DMA Registers:

PCI (Offset from PCIBAR0 Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI9080/9056 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI/ Local Writable	Serial EEPROM Writable
80h	100h	DMA Ch 0 Mode	Y	N
84h	104h	DMA Ch 0 PCI Address	Y	N
88h	108h	DMA Ch 0 Local Address	Y	N
8Ch	10Ch	DMA Ch 0 Transfer Byte Count	Y	N
90h	110h	DMA Ch 0 Descriptor Pointer	Y	N
94h	114h	DMA Ch 1 Mode	Y	N
98h	118h	DMA Ch 1 PCI Address	Y	N
9Ch	11Ch	DMA Ch 1 Local Address	Y	N
A0h	120h	DMA Ch 1 Transfer Byte Count	Y	N
A4h	124h	DMA Ch 1 Descriptor Pointer	Y	N
A8h	128h	Reserved / DMA Channel1 Command/ Status Register / DMA Channel0 Command/ Status Register	Y	N
ACh	12Ch	Mode/Arbitration Register	Y	N
B0h	130h	DMA Threshold Register	Y	N

DMA : currently 16 Words
LAS0 : currently 512 LWords



Local Bus Memory Map

Host Side Local Bus address ranges:

Absolute Address On Local bus	Size	Description
0x0000 0000 0x0FFF FFFF	256M Lwords	LAS0
0x1000 0000 0x3FFF FFFF		reserved
0x4000 0000 0x403F FFFF	4M Word	LAS1 FIFO space

LAS0 register area:

LAS0 address offset	LAS0 Description
0x000 – 0x0FF	Runtime Area
0x100 – 0x1FF	Setup Area

Runtime Area of LAS0:

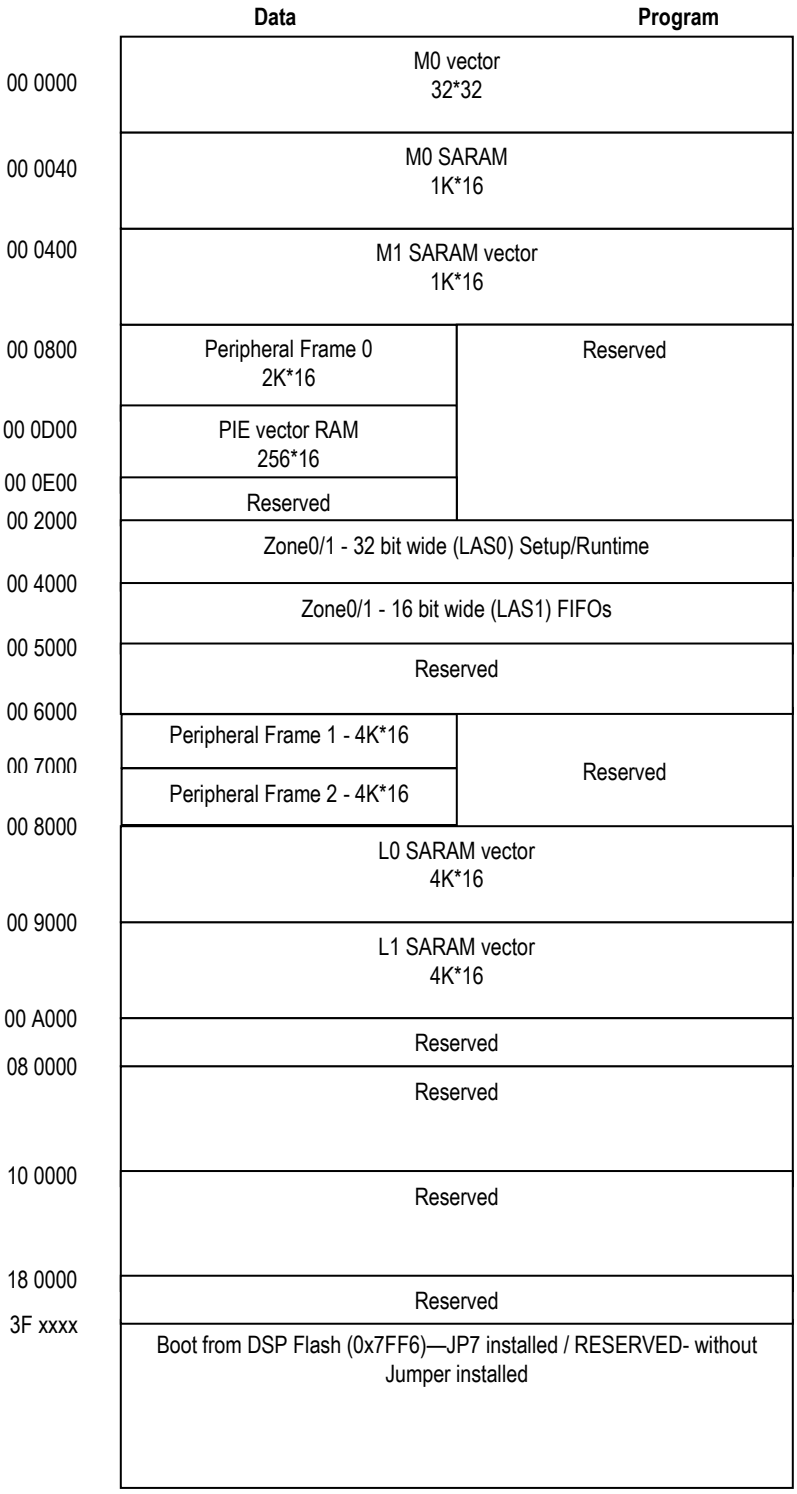
Read Function	Write Function	Local Address Space 0 Offset	Block Descriptions
	reserved	000h	D/A, A/D sampling runtime registers
Reserved	reserved	004h	
Read User Inputs	Write User Outputs	008h	
Software DAC clock start	Software DAC clock stop	00Ch	
Read FIFO Status	Software A/D Start	010h	
Reserved	Software D/A1 Update	014h	
Reserved	Software D/A2 Update	018h	
Reserved	reserved	01Ch	
Reserved	reserved	020h	
Reserved	Software Simultaneous D/A1 and D/A2 Update	024h	
Software Pacer Start	Software Pacer Stop	028h	
Read Timer Counters Status	Software high-speed input Sample	02Ch	
Read Interrupt Status	Write Interrupt Enable Mask Register	030h	
Clear Interrupt set by the Clear Mask	Set Interrupt Clear Mask	034h	
Read Interrupt Overrun Register	Clear Interrupt Overrun Register	038h	
Reserved	Reserved	03Ch	
Read *Pacer Clock* Counter value (24 bit)	Load count in *Pacer Clock* Counter (24 bit)	040h	Timer Counter Runtime registers
Read *Burst Clock* Counter value (10 bit)	Load count in *Burst Clock* Counter (10 bit)	044h	

Read Function	Write Function	Local Address Space 0 Offset	Block Descriptions
Read *A/D Sample counter* value (10 bit)	Load count in *A/D Sample counter* (10 bit)		
Read *D/A1 Update counter* value (10 bit)	Load count in *D/A1 Update* counter (10 bit)	04Ch	
Read *D/A2 Update counter* value (10 bit)	Load count in *D/A2 Update* counter (10 bit)	050h	
Read *Delay Counter* value (16 bit)	Load count in *Delay Counter* (16 bit)	054h	
Read *About Counter* value (16 bit)	Load count in *About Counter* (16 bit)	058h	
Read *DAC clock* value (16 bit)	Load count in *DAC clock* (16 bit)	05Ch	
Read 8254 *User TC 0* value	Load count in 8254 *User TC 0*	060h	
Read 8254 *User TC 1* value	Load count in 8254 *User TC 1*	064h	
Read 8254 *User TC 2* value	Load count in 8254 *User TC 2*	068h	
Reserved	Program counter mode for 8254 *User TC*	06Ch	
Read Port 0 digital input lines	Program Port 0 digital output lines	070h	Digital I/O Runtime registers
Read Port 1 digital input lines	Program Port 1 digital output lines	074h	
Clear digital IRQ status flag/read Port 0 direction, mask or compare register	Clear digital chip/program Port 0 direction, mask or compare register	078h	
Read Digital I/O Status word	Program Digital Control Register & Digital Interrupt enable	07Ch	
DSP Command register to be written from the Host side and read from DSP	DSP status to written to by DSP and read from Host side	0B0h	DSP Command

The LAS1 Register Area:

Read Function	Write Function	Local Address Space 1 Offset
Read A/D FIFO	-	0h (16-bit)
Read High Speed Digital Input FIFO	-	4h (16-bit)
-	Write D/A1 FIFO	8h (16-bit)
-	Write D/A2 FIFO	Ch (16-bit)

8.1 *DSP Memory map*



8.2 PCI Configuration Registers

The PCI configuration registers can be accessed by PCI BIOS calls. The meaning of the PCI configuration register is on the Table below. If you use the board via RTD's software driver you do not have any doing with this area.

Configuration Address Offset	PCI Writable	Byte3	Byte2	Byte1	Byte0
00h	No	Device Identification		Vendor Identification	
04h	Yes	Status		Command	
08h	No	Class Code			Revision
0Ch	Yes (7..0)	BIST	Header Type	PCI Latency Timer	Cache Line Size
10h	Yes	PCI Base Address 0 for Memory Mapped Local Configuration Registers PCIBAR0			
14h	Yes	PCI Base Address 1 for I/O Mapped Local Configuration Registers PCIBAR1			
18h	Yes	PCI Base Address 2 for Local Address Space 0 (LAS0)			
1Ch	Yes	PCI Base Address 3 for Local Address Space 1 (LAS1)			
20h	Yes	Reserved			
24h	Yes	Reserved			
28h	No	Reserved			
2Ch	No	Subsystem ID		Subsystem Vendor ID	
30h	Yes	PCI Base Address for Local Expansion ROM			
34h	No	Reserved			
38h	No	Reserved			
3Ch	Yes(7..0)	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

Field	Contents	Comment
Vendor Identification	1435h	Value Assigned to RTD Inc. by the PCI Special Interest Group
Device Identification	7520h	Type number of the Board
Class Code	1180h	Data acquisition controller
Cache Line Size	00h	
PCI Latency Timer	00h	
Header Type	00h	Single Function PCI Device
BIST	00h	The Built In Self-Test is not Supported
PCI Base Address 0 for Memory Mapped Local Configuration Registers	Assigned by the PCI BIOS	Controls the operation of local system
PCI Base Address 1 for I/O Mapped Local Configuration Registers	Assigned by the PCI BIOS	Controls the operation of local system
PCI Base Address 2 for Local Address Space 0 (LAS0)	Assigned by the PCI BIOS	LAS0 is the base address of the configuration/setup area and Timer/Counter, Digital I/O chip of DM35520
PCI Base Address 3 for Local Address Space 1 (LAS1)	Assigned by the PCI BIOS	LAS1 is the base address of the A/D, D/A, and High-Speed Digital Input data transfer area of DM35520
Subsystem ID	9080/9056h	Depends on type of PLX chip
Subsystem Vendor ID	10B5h	Vendor ID for PLX
PCI Base Address for Local Expansion ROM	00000000h	No external BIOS
Interrupt Line	0xh	Interrupt Line Assigned by the BIOS
Interrupt Pin	01h	INTA# Interrupt
Min_Gnt	00h	
Max_Lat	00h	

8.2.1 PCIIDR - DEVICE ID, VENDOR ID

(PCI CFG offset:00, EEPROM offset:00)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0100	0101	0010	0000	0001	0100	0011	0101
4	5	2	0	1	4	3	5

45201435

8.2.2 PCICCR - CLASS CODE

(PCI CFG offset:09- 0B, EEPROM offset:04)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
1111	1111	0000	0000	0000	0000	0000	0000
F	F	0	0	0	0	0	0

FF000000

8.2.3 PCICLSR, PCI LTR, PCI HTR, PCIIPR PCIILR

(PCI CFG offset:0C.. 0E, 3D, 3C, EEPROM offset:08)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0001	0000	0000
0	0	0	0	0	1	0	0

00000100

8.2.4 PCISVID - PCI SUBSYSTEM VENDOR ID

(PCI CFG offset:2C, EEPROM offset:44)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
1001	0000	1000	0000	0001	0000	1011	0101
9	0	8	0	1	0	B	5

9080/905610B5

8.2.5 PEROMBA - EXPANSION ROM PCI BASE ADDRESS REGISTER

(PCI CFG offset:30, EEPROM offset:54)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	0	0	0

00000000

8.3 Local Configuration Registers

PCI Address Offset from Local Configuration Registers Base Address	PCI and Serial EEPROM Writable	32 bit registers
00h	Yes	LAS0RR - Range for PCI-to-Local Address Space 0
04h	Yes	LAS0BA - Local Base Address (Remap) for PCI-to-Local Address Space 0
08h	Yes	MARBR - Mode/Arbitration Register
0Ch	Yes	BIGEND - Big/Little Endian Description Register
10h	Yes	EROMRR - Range for Expansion ROM
14h	Yes	EROMBA - Local Base Address (Remap) for PCI to ROM
18h	Yes	LBRD0 - Local Address Space 0 Bus Region Description Register
1Ch	Yes	DMRR - Local Range Register for Direct Master to PCI
20h	Yes	DMLBAM - Local Base Address Register for Direct Master to PCI memory
24h	Yes	DMLBAI - Local Base Address Register for Direct Master to PCI IO/CFG
28h	Yes	DMPBAM - PCI Base Address Register for Direct Master to PCI memory
2Ch	Yes	DMCFGA - PCI Configuration Address Reg. for Direct Master to PCI IO/CFG
F0h	Yes	LAS1RR - Range for PCI-to-Local Address Space 1
F4h	Yes	LAS1BA - Local Base Address (Remap) for PCI-to-Local Address Space 0
F8h	Yes	LBRD1 - Local Address Space 1 Bus Region Description Register

8.3.1 Range for PCI-to-Local Address Space 0 Register

(LAS0RR, PCI:00h, EEPROM offset: 14)

The Local Address Space 0 (LAS0) is a 32 bit wide, *512 byte long* Memory-mapped area with zero Wait states without burst access.

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
1111	1111	1111	1111	1111	1110	0000	0000
F	F	F	F	F	E	0	0

FFFFFE00

B0: 1 Memory Space Indicator
B2-1: 00 Locate anywhere in 32 bit PCI address space
B3: 0 - No prefetch
B31- 4: Specifies PCI address bits used to decode PCI access to local bus Space Each of the bits correspond to an address bit. Bit 31 corresponds to address bit 31. A value of 1 indicates the bits should be included in decode. Write a value of 0 to all others.

8.3.2 Local Base Address (Remap) for PCI-to-Local Address Space 0 Register

(LAS0BA, PCI: 04, EEPROM offset: 18)

The Local Address Space 0 (LAS0) is a 16 bit wide, *32 byte long* I/O area without Wait states, without burst access.

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0001
0	0	0	0	0	0	0	1

00000001

B0: 1 Space 0 enable. A value of 1 enables decode of PCI Address for direct slave access to local space0
B1: Unused 0
B3- 2: Not used
B31- 4: The bits in this register replace the PCI address bits used in decode as the local address bits.

8.3.3 MODE/ARBITRATION REGISTER

(MARBR, PCI: 08, EEPROM offset: 1C)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0010	0000	0000	0000	0000	0000
0	0	2	0	0	0	0	0

00200000

B7-0: Local Bus Latency Timer. Number of Local Bus Clock cycles before de-asserting HOLD and releasing the Local Bus. Also used with bit 27 to delay BREQ input to give up the Local Bus only when this timer expires.

B15-8: Local Bus Pause Timer. Number of Local Bus Clock cycles before reasserting HOLD after releasing the Local Bus.

Note: Applicable only to DMA operation.

B16: Local Bus Latency Timer Enable. Value of 1 enables latency timer.

B17: Local Bus Pause Timer Enable. Value of 1 enables pause timer.

B18: Local Bus BREQ Enable. Value of 1 enables Local Bus BREQ input. When BREQ input is active, the PCI9080/9056 de-asserts HOLD and releases Local Bus.

B20-19: DMA Channel Priority. Value of 00 indicates rotational priority scheme. Value of 01 indicates Channel 0 has priority. Value of 10 indicates Channel 1 has priority. Value of 11 is reserved.

B21: Local Bus Direct Slave Give up Bus Mode. When set to 1, the PCI9080/9056 de-asserts HOLD and releases the Local Bus when the Direct Slave Write FIFO becomes empty during a Direct Slave Write or when the Direct Slave Read FIFO becomes full during a Direct Slave Read.

B22: Direct Slave LLOCKo# Enable. Value of 1 enables PCI Direct Slave locked sequences. Value of 0 disables Direct Slave locked sequences.

B23: PCI Request Mode. Value of 1 causes the PCI9080/9056 to de-assert REQ when it asserts FRAME during a Master cycle. Value of 0 causes the PCI9080/9056 to leave REQ asserted for the entire Bus Master cycle.

B24: PCI Specification v2.1 Mode. When set to 1, the PCI9080/9056 operates in Delayed Transaction mode for Direct Slave Reads. The PCI9080/9056 issues a Retry and prefetches Read data.

B25: PCI Read No Write Mode. Value of 1 forces Retry on Writes if Read is pending. Value of 0 bit allows Writes to occur while Read is pending.

B26: PCI Read with Write Flush Mode. Value of 1 submits request to flush pending a Read cycle if a Write cycle is detected. Value of 0 submits request to not effect pending Reads when a Write cycle occurs (PCI Specification v2.1 compatible).

B27: Gate Local Bus Latency Timer with BREQ. If set to 0, the PCI9080/9056 gives up the Local Bus during Direct Slave or DMA transfer after the current cycle (if enabled and BREQ is sampled). If set to 1, the PCI9080/9056 gives up the Local Bus only if BREQ is sampled and the Local Bus Latency Timer is enabled and expired during a Direct Slave or DMA transfer.

B28: PCI Read No Flush Mode. Value of 1 submits a request to not flush the Read FIFO if a PCI Read cycle completes (Read Ahead mode). Value of 0 submits a request to flush the Read FIFO if a PCI Read cycle completes.

B29: If set to 0, reads from PCI Configuration register address 00h and returns Device ID and Vendor ID. If set to 1, reads from PCI Configuration Register address 00h and returns Subsystem ID and Subsystem Vendor ID.

B31-30: Reserved.

8.3.4 BIG/LITTLE ENDIAN DESCRIPTOR REGISTER

(BIGEND, PCI:0Ch, EEPROM offset: 20h)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	0	0	0

00000000

B0: Configuration Register Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Local accesses to the Configuration registers. Value of 0 specifies Little Endian ordering. Big Endian mode can be specified for Configuration Register accesses by asserting BIGEND# pin during Address phase of access.

B1: Direct Master Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Direct Master accesses. Value of 0 specifies Little Endian ordering. Big Endian mode can be specified for Direct Master accesses by asserting the BIGEND# input pin during Address phase of access.

B2: Direct Slave Address Space 0 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Direct Slave accesses to Local Address Space 0. Value of 0 specifies Little Endian ordering.

B3: Direct Slave Address Expansion ROM 0 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Direct Slave accesses to Expansion ROM. Value of 0 specifies Little Endian ordering.

B4: Big Endian Byte Lane Mode. Value of 1 specifies that in Big Endian mode, use byte lanes [31:16] for 16-bit Local Bus and byte lanes [31:24] for 8-bit Local Bus. Value of 0 specifies that in Big Endian mode, byte lanes [15:0] be used for 16-bit Local Bus and byte lanes [7:0] for 8-bit Local Bus.

B5: Direct Slave Address Space 1 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Direct Slave accesses to Local Address Space 1. Value of 0 specifies Little Endian ordering.

B6: DMA Channel 1 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for DMA Channel 1 accesses to the Local Address Space. Value of 0 specifies Little Endian ordering.

B7: DMA Channel 0 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for DMA Channel 0 accesses to the Local Address Space. Value of 0 specifies Little Endian ordering.

B31-8: Reserved.

8.3.5 EXPANSION ROM RANGE REGISTER

(EROMRR, PCI:10h, EEPROM offset: 24h)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	0	0	0

00000000

B10-0: Reserved.

B31-11: Specifies which PCI Address bits to use for decoding PCI-to-Local Bus Expansion ROM. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits to be included in the decode and 0 to all other bits (used in conjunction with PCI Configuration register 30h). Default is 64 KB.

Note: Range (**not** Range register) must be a power of 2. "Range register value" is the inverse of range.

8.3.6 EXPANSION ROM LOCAL BASE ADDRESS (REMAP) REGISTER AND BREQO CONTROL

(EROMBA, PCI:14h, EEPROM offset: 28h)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	0	0	0

00000000

B3-0: Direct Slave BREQo (Backoff Request Out) Delay Clocks. Number of Local Bus clocks in which Direct Slave HOLD request is pending and a Local Direct Master access is in progress and not being granted the bus (LHOLDA) before asserting BREQo. Once asserted, BREQo remains asserted until the PCI9080/9056 receives LHOLDA (LSB = 8 or 64 clocks).

B4: Local Bus BREQo Enable. Value of 1 enables the PCI9080/9056 to assert BREQo output.

B5: BREQo Timer-Resolution. Value of 1 changes LSB of the BREQo timer from 8 to 64 clocks.

B10-6: Reserved. Yes No 0

B31-11: Remap of PCI Expansion ROM Space into a Local Address Space. Remap (replace) PCI Address bits used in decode as Local Address bits.

Note: Remap Address value must be multiple of Range (**not** Range register).

8.3.7 LOCAL ADDRESS SPACE 0/EXPANSION ROM BUS REGION DESCRIPTOR REGISTER

(LBRD0; PCI:18h, EEPROM offset: 2Ch)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0100	0010	0000	0000	0000	0001	0100	0011
4	2	0	0	0	1	4	3

42000143

B1-0: Memory Space 0 Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits. S = 01, J = 11, C = 11

B5-2: Memory Space 0 Internal Wait States (data to data; 0-15 wait states).

B6: Memory Space 0 Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.

B7: Memory Space 0 BTERM# Input Enable. Value of 1 enables BTERM# input. Value of 0 disables BTERM# input. If set to 0, the PCI9080/9056 bursts four Lword maximum at a time.

B8: Memory Space 0 Prefetch Disable. If mapped into memory space, a value of 0 enables Read prefetching. Value of 1 disables prefetching. If prefetching is disabled, the PCI9080/9056 disconnects after each memory read.

B9: Expansion ROM Space Prefetch Disable. Value of 0 enables Read prefetching. Value of 1 disables prefetching. If prefetching is disabled, the PCI9080/9056 disconnects after each memory read.

B10: Read Prefetch Count Enable. When set to 1 and memory prefetching is enabled, the PCI9080/9056 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI9080/9056 ignores the count and continues prefetching until terminated by PCI Bus.

B14-11: Prefetch Counter. Number of Lwords to prefetch during Memory Read cycles (0-15). Count of zero selects prefetch of 16 Lwords.

B15: Reserved.

B17-16: Expansion ROM Space Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits. S = 01,J = 11, C = 11

B21-18: Expansion ROM Space Internal Wait States (data to data; 0-15 wait states).

B22: Expansion ROM Space Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.

B23: Expansion ROM Space Bterm Input Enable. Value of 1 enables BTERM# input. Value of 0 disables Bterm input. If set to 0, the PCI9080/9056 bursts four Lword maximum at a time.

B24: Memory Space 0 Burst Enable. Value of 1 enables bursting. Value of 0 disables bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.

B25: Extra Long Load from Serial EEPROM. Value of 1 loads Subsystem ID and Local Address Space 1 registers. Value of 0 indicates not to load them.

B26: Expansion ROM Space Burst Enable. Value of 1 enables bursting. Value of 0 disables bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.

B27: Direct Slave PCI Write Mode. Value of 0 indicates the PCI9080/9056 should disconnect when the Direct Slave Write FIFO is full. Value of 1 indicates the PCI9080/9056 should de-assert TRDY# when the Write FIFO is full.

B31-28: PCI Target Retry Delay Clocks. Contains value (multiplied by 8) of the number of PCI Bus clocks after receiving PCI -to-Local Read or Write access and not successfully completing a transfer. Only pertains to Direct Slave Writes when bit 27 is set to 1.

8.3.8 LOCAL RANGE REGISTER FOR DIRECT MASTER TO PCI

(DMRR; PCI:1Ch, EEPROM offset: 30h)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	0	0	0

00000000

B15-0: Reserved (64 KB increments).

B31-16: Specifies which Local Address bits to use for decoding Local-to-PCI Bus access. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31.Write 1 to all bits that must be included in decode and 0 to all others. Used for Direct Master Memory, I/O, or Configuration accesses.

Note: Range (**not** Range register) must be power of 2. "Range register value" is the inverse of range.

8.3.9 Local Bus Base Address Register for Direct Master to PCI Memory

(DMLBAM; PCI:20h, EEPROM offset: 34h)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	0	0	0

00000000

B15-0: Reserved. Yes No 0
B31-16: Assigns value to bits to use for decoding Local-to-PCI Memory access.
Note: Local Base Address value must be multiple of Range (**not** Range register).

8.3.10 Local Base Address Register for Direct Master to PCI IO/CFG

(DMLBAI; PCI:24h, EEPROM offset: 38h)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	0	0	0

00000000

B15-0: Reserved.
B31-16: Assigns value to bits to use for decoding Local-to-PCI I/O or Configuration access. Used for Direct Master I/O and Configuration accesses.
Notes: Local Base Address value must be multiple of Range (**not** Range register). Refer to DMPBAM[13] for I/O Remap Address option.

8.3.11 PCI Base Address (Remap) Register for Direct Master to PCI Memory

(DMPBAM; PCI:28h, EEPROM offset: 3Ch)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	0	0	0

00000000

B0: Direct Master Memory Access Enable. Value of 1 enables decode of Direct Master Memory accesses. Value of 0 disables decode of Direct Master Memory accesses.
B1: Direct Master I/O Access Enable. Value of 1 enables decode of Direct Master I/O accesses. Value of 0 disables decode of Direct Master I/O accesses.
B2: LLOCK# Input Enable. Value of 1 enables LLOCK# input, enabling PCI-locked sequences. Value of 0 disables LLOCK# input.
B12, 3: Direct Master Read Prefetch Size control. Values:
00 = The PCI9080/9056 continues to prefetch Read data from the PCI Bus until the Direct Master access is finished. May result in additional four unneeded Lwords being prefetched from the PCI Bus.
01 = Prefetch up to four Lwords from the PCI Bus
10 = Prefetch up to eight Lwords from the PCI Bus
11 = Prefetch up to 16 Lwords from the PCI Bus
If PCI memory prefetch is not wanted, performs Direct Master Single cycle. Direct Master Burst reads must not exceed programmed limit.
B4: Direct Master PCI Read Mode. Value of 0 indicates the PCI9080/9056 should release PCI Bus when the Read FIFO becomes full. Value of 1 indicates the PCI9080/9056 should keep PCI Bus and de-assert IRDY when the Read FIFO becomes full.
B10, 8-5: Programmable Almost Full Flag. When the number of entries in the 32-word Direct Master Write FIFO exceeds this value, output pin DMPAF# is asserted low.
B9: Write and Invalidate Mode. When set to 1, the PCI9080/9056 waits for 8 or 16 Lwords to be written from the Local Bus before starting PCI access. When set, all Local Direct Master to PCI Write accesses must be 8- or 16-Lword bursts. Use in conjunction with PCICR[4] and Section 3.6.1.9.2, “Direct Master Write and Invalidate”.
B11: Direct Master Prefetch Limit. If set to 1, don’t prefetch past 4 KB (4098 bytes) boundaries.
B13: I/O Remap Select. When set to 1, forces PCI Address bits [31:16] to all zeros. When set to 0, uses bits [31:16] of this register as PCI Address bits [31:16].
B15-14: Direct Master Write Delay. Used to delay PCI Bus request after Direct Master Burst Write cycle has started. Values:
00 = No delay; start cycle immediately
01 = Delay 4 PCI clocks
10 = Delay 8 PCI clocks
11 = Delay 16 PCI clocks
B31-16: Remap of Local-to-PCI Space into PCI Address Space. Remap (replace) Local Address bits used in decode as PCI Address bits. Used for Direct Master Memory and I/O accesses.

Note: Remap Address value must be multiple of Range (**not** Range register).

8.3.12 PCI CONFIGURATION ADDRESS REGISTER FOR DIRECT MASTER TO PCI IO/CFG

(DMCFGA; PCI:2Ch, EEPROM offset: 40h)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0000	0000	0000
0	0	0	0	0	0	0	0

00000000

B1-0: Configuration Type (00=Type 0, 01=Type 1). 0
B7-2: Register Number. If different register Read/Write is needed, value must be programmed and new PCI Configuration cycle must be generated.
B10-8: Function Number.
B15-11: Device Number.
B23-16: Bus Number.
B30-24: Reserved.
B31: Configuration Enable. Value of 1 allows Local-to-PCI I/O accesses to be converted to a PCI Configuration cycle. Parameters in this table are used to generate PCI configuration address.

8.3.13 PCI LOCAL ADDRESS SPACE 1 RANGE REGISTER FOR PCI-TO-LOCAL BUS

(LAS1RR; PCI:F0h, EEPROM offset: 48h)

The Local Address Space 1 (LAS1) is a 16 bit wide, *16 byte long* Memory-mapped area with zero Wait states with burst access.

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
1111	1111	1111	1111	1111	1111	1111	0000
F	F	F	F	F	F	F	0

FFFFFFF0

B0: Memory Space Indicator. Value of 0 indicates Local Address Space 1 maps into PCI memory space. Value of 1 indicates Address Space 1 maps into PCI I/O space.
B2-1: If mapped into memory space, encoding is as follows:
00 Locate anywhere in 32-bit PCI Address space
01 Locate below 1 MB in PCI Address space
10 Locate anywhere in 64-bit PCI Address space
11 Reserved
If mapped into I/O space, bit 1 must be set to 0.Bit 2 is included with bits [31:3] to indicate decoding range.
B3: If mapped into memory space, a value of 1 indicates reads are prefetchable (does not affect operation of the PCI9080/9056, but is used for system status). If mapped into I/O space, bit is included with bits [31:2] to indicate decoding range.
bit 31:4: Specifies which PCI Address bits to use for decoding PCI access to Local Bus Space 1. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others (used in conjunction with PCI Configuration Register Ch 1). Default is 1 MB.

Notes: Range (**not** Range register) must be power of 2. "Range register value" is the inverse of range. User should limit all I/O spaces to 256 bytes per PCI Specification v2.1.If QSR bit 0 is set, defines PCI Base Address 0.

8.3.14 LOCAL ADDRESS SPACE 1 LOCAL BASE ADDRESS (REMAP) REGISTER

(LAS1BA; PCI:F4h, EEPROM offset: 4Ch)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0100	0000	0000	0000	0000	0000	0000	0001
4	0	0	0	0	0	0	1

40000001

B0: Space 1 Enable. Value of 1 enables decoding of PCI Addresses for Direct Slave access to Local Space 1. Value of 0 disables decoding. If set to 0, PCI BIOS may not allocate (assign) base address for Space 1.

Note: Must be set to 1 for any Direct Slave access to Space 1.

B1: Reserved.

B3-2: If Local Space 1 is mapped into memory space, bits are not used. If mapped into I/O space, bit is included with bits [31:4] for remapping.

B31-4: Remap of PCI Address to Local Address Space 1 into a Local Address Space. Remap (replace) PCI Address bits used in decode as Local Address bits.

Note: Remap Address value must be multiple of Range (**not** Range register).

8.3.15 LOCAL ADDRESS SPACE 1 BUS REGION DESCRIPTOR REGISTER

(LBRD1; PCI:F8h, EEPROM offset: 50h)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0000	0001	1100	0001
0	0	0	0	0	1	C	1

000001C1

B1-0: Memory Space 1 Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits.
J = 11
C = 11

B5-2: Memory Space 1 Internal Wait States (data to data; 0-15 wait states).

B6: Memory Space 1 Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.

B7: Memory Space 1 BTERM# Input Enable. Value of 1 enables BTERM# input. Value of 0 disables BTERM# input. If set to 0, the PCI9080/9056 bursts four Lword maximum at a time.

B8: Memory Space 1 Burst Enable. Value of 1 enables bursting. Value of 0 disables bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.

B9: Memory Space 1 Prefetch Disable. If mapped into memory space, value of 0 enables Read prefetching. Value of 1 disables prefetching. If prefetching is disabled, the PCI9080/9056 disconnects after each memory read.

B10: Read Prefetch Count Enable. When set to 1 and memory prefetching is enabled, the PCI9080/9056 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI9080/9056 ignores the count and continues prefetching until terminated by PCI Bus.

B14-11: Prefetch Counter. Number of Lwords to prefetch during memory Read cycles(0-15).

B31-15: Reserved.

8.4 Runtime Registers

The PLX Mailbox registers and doorbell registers are not used in DM35520, there are no local processors on the board. Therefore the Mailbox Register 0 and 1 can be downloaded from serial EEPROM. The Mailbox Register 0 is used to store the Date of EEPROM content creation in Year/Month/Day format in Hex.

The Interrupt Control /Status Registers are described in the Interrupt chapter.

PCI (Offset from Base Address)	PCI Writable	Serial EEPROM Writable	To ensure software compatibility with other versions of the PCI9080/9056 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	
40h	Yes	Yes	Mailbox Register 0 (see Note)	
44h	Yes	Yes	Mailbox Register 1 (see Note)	
48h	Yes	No	Mailbox Register 2 - Not used in	
4Ch	Yes	No	Mailbox Register 3- Not used	
50h	Yes	No	Mailbox Register 4- Not used	
54h	Yes	No	Mailbox Register 5- Not used	
58h	Yes	No	Mailbox Register 6- Not used	
5C	Yes	No	Mailbox Register 7- Not used	
60h	Yes	No	PCI-to-Local Doorbell Register	
64h	Yes	No	Local-to-PCI Doorbell Register	
68h	Yes	No	Interrupt Control / Status	
6Ch	Yes	No	Serial EEPROM Control, PCI Command Codes, User I/O Control, Init Control	
70h	No	No	Device ID	Vendor ID
74h	No	No	Unused	Revision ID
78h	Yes	No	Mailbox Register 0 (see Note)	
7Ch	Yes	No	Mailbox Register 1 (see Note)	

Note: Mailbox registers 0 and 1 are always accessible at addresses 78h/C0h and 7Ch/C4. When the I2O feature is disabled (QSR[0]=0), Mailbox registers 0 and 1 are also accessible at PCI Addresses 40h and 44h for PCI 9060 compatibility. When the I2O feature is enabled, the Inbound and Outbound Queue pointers are accessed at addresses40h and 44h, replacing the Mailbox registers in PCI Address space.

For the Interrupt Control/Status register description see the Chapter of Interrupt.

The only register described here is the Serial EEPROM Control Register.

8.4.1 SERIAL EEPROM CONTROL, PCI COMMAND CODES, USER I/O CONTROL, INIT CONTROL

(CNTRL; PCI:6Ch, no EEPROM loadable)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0000	0000	0000	0000	0111	0110	0111	1110
0	0	0	0	7	6	7	E

0000767E

B3-0: PCI Read Command Code for DMA. Sent out during DMA Read cycles.
B7-4: PCI Write Command Code for DMA. Sent out during DMA Write cycles.
B11-8: PCI Memory Read Command Code for Direct Master. Sent out during Direct Master Read cycles.
B15-12: PCI Memory Write Command Code for Direct Master. Sent out during Direct Master Write cycles.
B16: General Purpose Output. Value of 1 causes USERO output to go high. Value of 0 causes USER0 output to go low. Not used on DM35520.
B17: General Purpose Input. Value of 1 indicates USERI input pin is high. Value of 0 indicates USERI pin is low. Not used.
B23-18: Reserved.
B24: Serial EEPROM Clock for Local or PCI Bus Reads or Writes to Serial EEPROM. Toggling this bit generates serial EEPROM clock. (Refer to manufacturer's data sheet for particular serial EEPROM being used.)
B25: Serial EEPROM Chip Select. For Local or PCI Bus Reads or Writes to serial EEPROM, setting this bit to 1 provides serial EEPROM chip select.
B26: Write Bit to serial EEPROM. For Writes, this output bit is input to serial EEPROM Clocked into serial EEPROM by serial EEPROM clock.
B27: Read Serial EEPROM Data. For Reads, this input bit is output of serial EEPROM. Clocked out of serial EEPROM by serial EEPROM clock.
B28: Serial EEPROM Present. Value of 1 indicates serial EEPROM is present.
B29: Reload Configuration Registers. When set to 0, writing 1 causes the PCI9080/9056 to reload Local Configuration registers from serial EEPROM.
B30: PCI Adapter Software Reset. Value of 1 holds Local Bus logic in the PCI9080/9056 reset and LRESETo# asserted. Contents of PCI Configuration registers and Shared Run Time registers are not reset. Software Reset can only be cleared from the PCI Bus. (Local Bus remains reset until this bit is cleared.)
B31: Local Init Status. Value of 1 indicates Local Init done. Responses to PCI accesses are Retries until this bit is set. While input pin NB# is asserted low, this bit is forced to 1.

9 The PLX9080/9056 EEPROM Content

The EEPROM can be programmed in an external programmer or using the Serial EEPROM Control, PCI Command Codes Register.

Serial EEPROM Offset	Value (Hex)	Description
00	7520	Device ID (depends on type of board installed)
02	1435	Vendor ID
04	1180	PCICCR; Class Code
06	0000	PCICCR; Class Code rev.
08	0000	Maximum Latency, Minimum Grant,
0A	0100	Int Pin, Int Routing
0C	1999	MSW of Mailbox 0 (EEPROM Content Creation Date)
0E	0126	LSW of Mailbox 0 (EEPROM Content Creation Date)
10	0000	MSW of Mailbox 1
12	0000	LSW of Mailbox 1
14	ffff	MSW of LAS0RR; Local Address Space 0 Range - 512 byte
16	fe00	LSW of LAS0RR; Local Address Space 0 Range - 512 byte
18	0000	MSW of LAS0BA; Local Address Space 0 Base Address (Re-Map)
1A	0001	LSW of LAS0BA; Local Address Space 0 Base Address (Re-Map)
1C	0020	MSW of MARBR; Mode, Arbitration Register
1E	0000	LSW of MARBR; Mode, Arbitration Register
20	0000	MSW of BIGEND; Big/Little Endian Descriptor Register
22	0000	LSW of BIGEND; Big/Little Endian Descriptor Register
24	0000	MSW of EROMRR; Expansion ROM Range
26	0000	LSW of EROMRR; Expansion ROM Range
28	0000	MSW of EROMBA; Expansion ROM Base Address (ReMap)
2A	0000	LSW of EROMBA; Expansion ROM Base Address (ReMap)
2C	4200	MSW of LBRD0; Local Address Space 0 Bus Region Descriptors
2E	0143	LSW of LBRD0; Local Address Space 0 Bus Region Descriptors
30	0000	MSW of DMRR; Range Register for Direct Master To PCI
32	0000	LSW of DMRR; Range Register for Direct Master To PCI
34	0000	MSW of DMLBAM; Base Address Register for Direct Master to PCI
36	0000	LSW of DMLBAM; Base Address Register for Direct Master to PCI
38	0000	MSW of DMLBAI; Base Addr. Reg. for Direct Master to PCI IO/CFG
3A	0000	LSW of DMLBAI; Base Addr. Reg. for Direct Master to PCI IO/CFG
3C	0000	MSW of DMPBAM; PCI Base Addr. R. for Dir. Master to PCI (ReMap)
3E	0000	MSW of DMPBAM; PCI Base Addr. R. for Dir. Master to PCI (ReMap)
40	0000	MSW of DMCFGA; PCI Conf. Addr. R. for Dir. Master to PCI IO/CFG
42	0000	LSW of DMCFGA; PCI Conf. Addr. R. for Dir. Master to PCI IO/CFG
44	9080/ 9056	Subsystem ID,
46	10B5	Subsystem Vendor ID
48	FFFF	MSW of LAS1RR; Local Address Space 1 Range-16 byte (FF00-16MB)
4A	FFF0	LSW of LAS1RR; Local Address Space 1 Range-16 byte (0000-16MB)
4C	4000	MSW of LAS1BA; Local Address Space 1 Base Address ReMap
4E	0001	MSW of LAS1BA; Local Address Space 1 Base Address ReMap
50	0000	MSW of LBRD1; Local Address Space 1 Bus Region Descriptors
52	01C1	LSW of LBRD1; Local Address Space 1 Bus Region Descriptors
54	0000	MSW of PEROMBA;Expansion ROM PCI Base Address Register
56	0000	LSW of PEROMBA;Expansion ROM PCI Base Address Register

10 Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization (RMA) number.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by RTD Embedded Technologies, “acts of God” or other contingencies beyond the control of RTD Embedded Technologies), or as a result of service or modification by anyone other than RTD Embedded Technologies. Except as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and RTD Embedded Technologies expressly disclaims all warranties not stated herein. All implied warranties, including implied warranties for merchantability and fitness for a particular purpose, are limited to the duration of this warranty. In the event the product is not free from defects as warranted above, the purchaser's sole remedy shall be repair or replacement as provided above. Under no circumstances will RTD Embedded Technologies be liable to the purchaser or any user for any damages, including any incidental or consequential damages, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

Some states do not allow the exclusion or limitation of incidental or consequential damages for consumer products, and some states do not allow limitations on how long an implied warranty lasts, so the above limitations or exclusions may not apply to you.

This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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