SerDes and its Role in Future Designs

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Serdes / Differential Pair

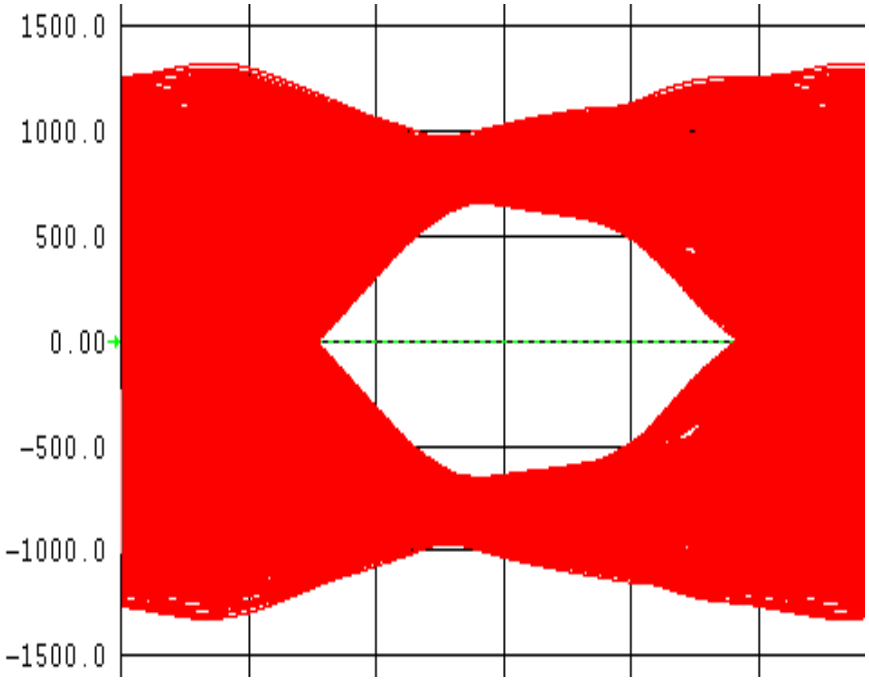
The Future of High Speed Designs

- PCB material
- Stackup
- Crosstalk
- FWE (Fiber Weave Effect)
- Stubs & backdrilling
- Surface roughness
- IL/RL/FEXT/NEXT (Insertion/Return Loss/Crosstalk)
- BOR (Break Out Region) or signal launch
- DC blocking cap planes
- Bypass/Decoupling mounting inductance

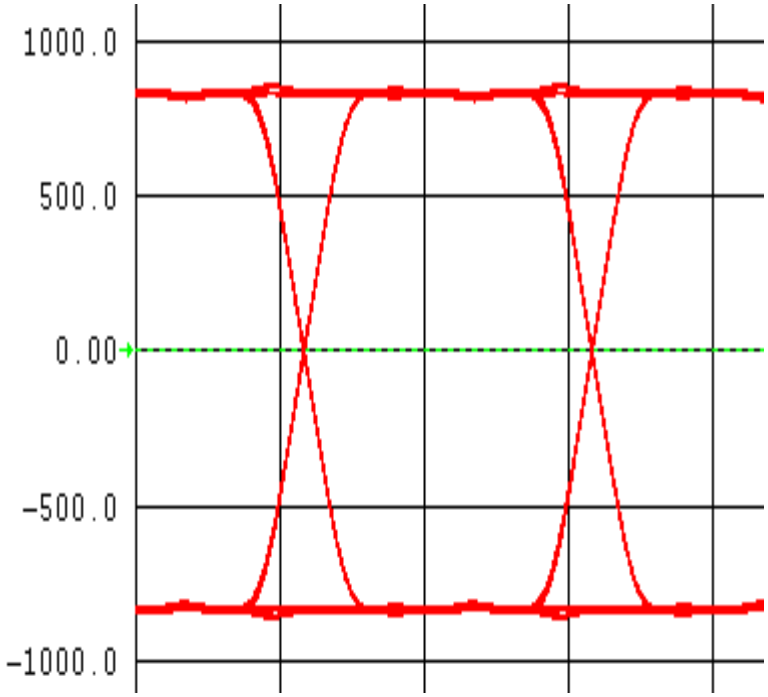
Differential Pair Skew

Equal Skew – Slower Frequency & t_{rise}

200 mil / 5 mm - Skew at driver



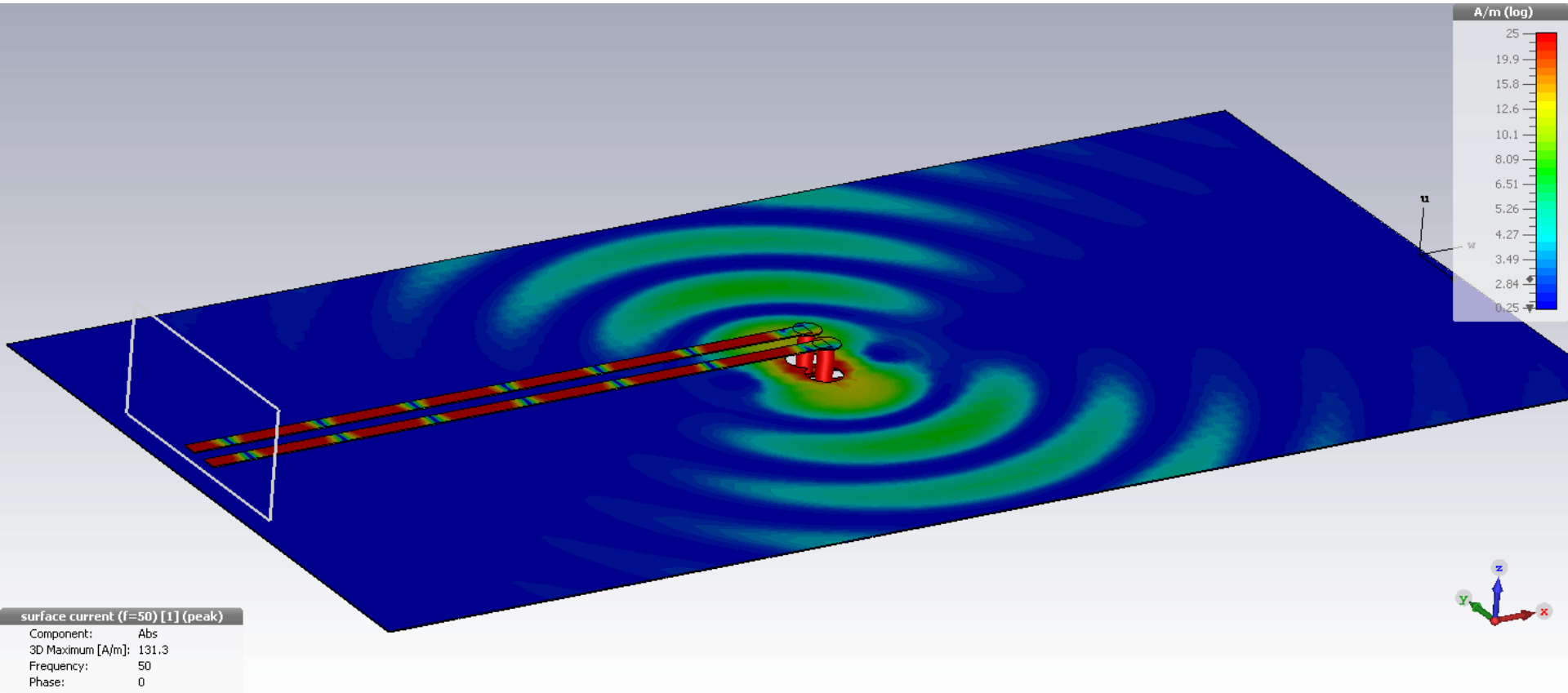
10 Gb/s



1 Gb/s

Reference Connectivity

No Return Currents Path

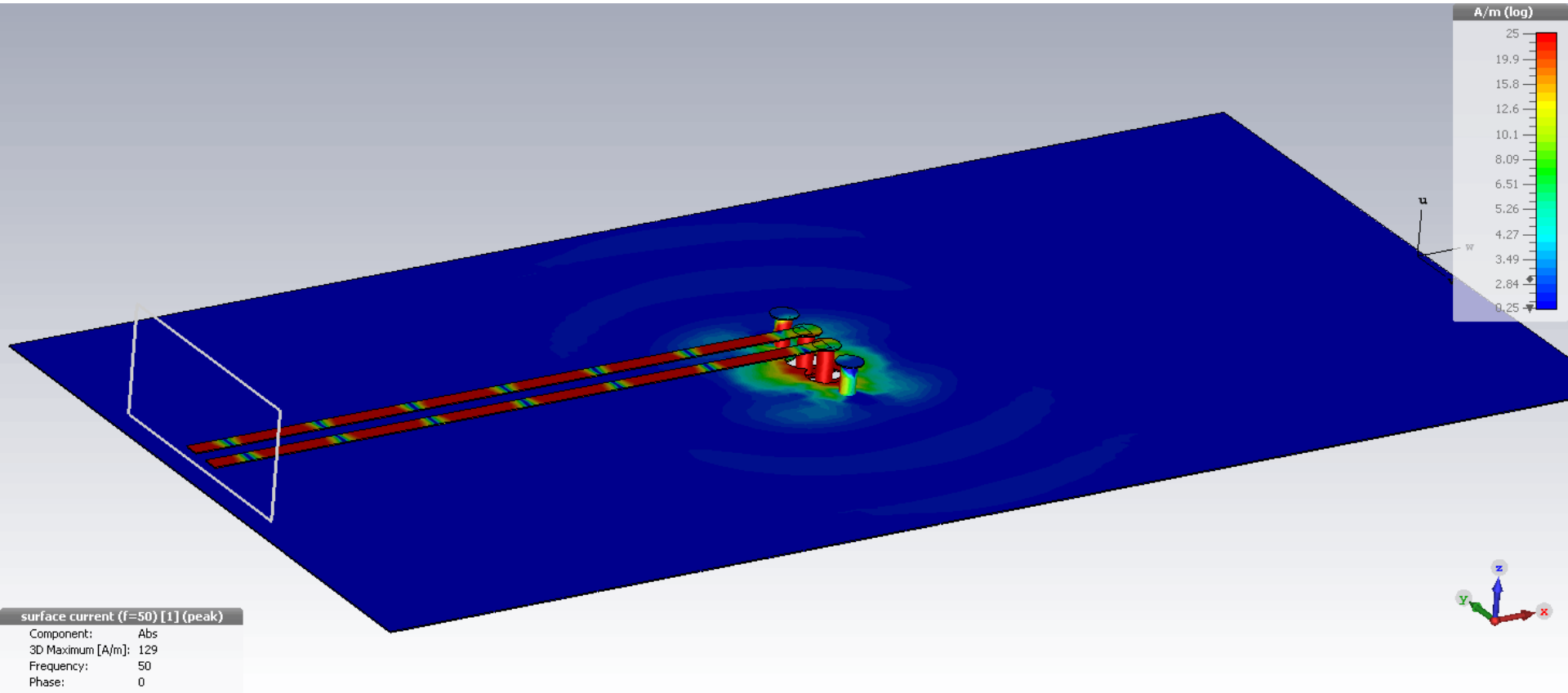


Differential pair with no via stitching

No return current path close

Reference Connectivity

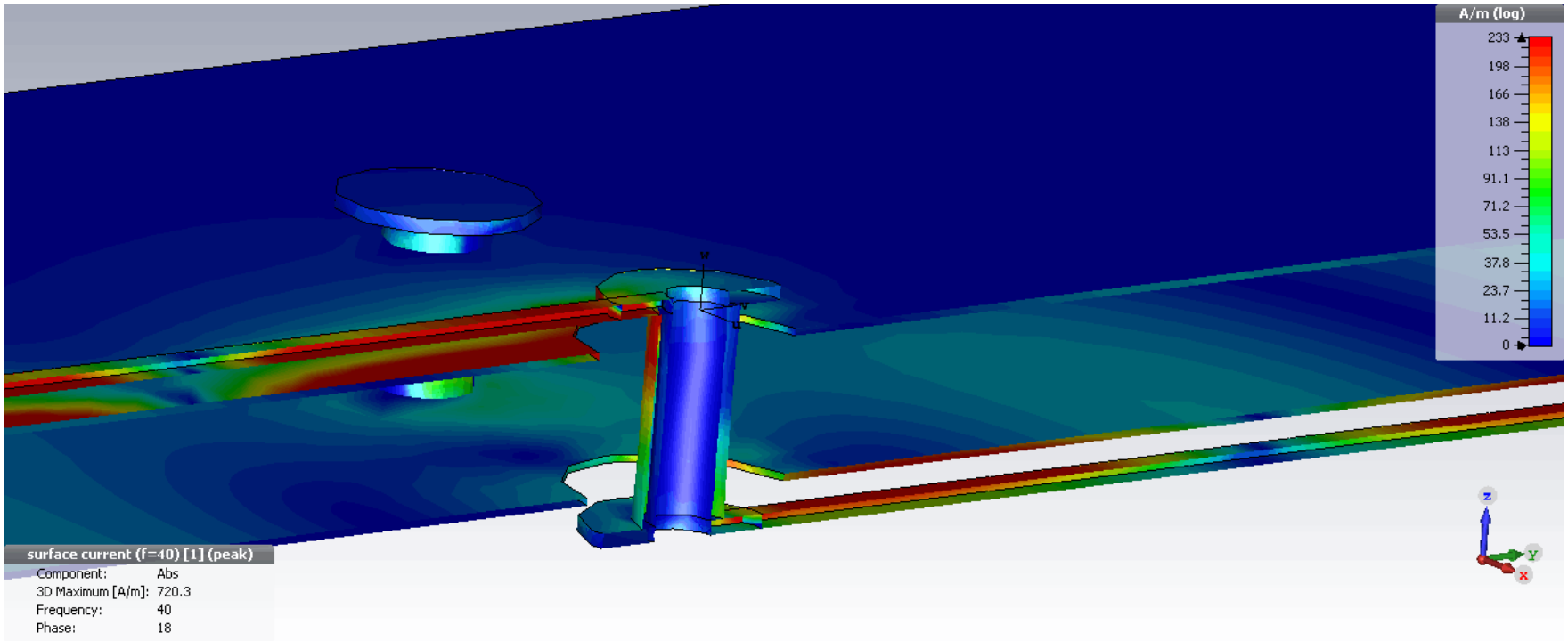
Stitching Vias for Return Currents

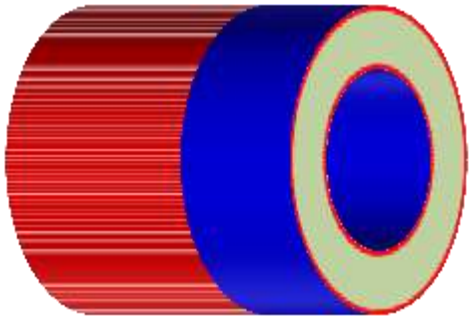


Differential pair with via stitching
Return current path close

AC Losses

Current in a Via

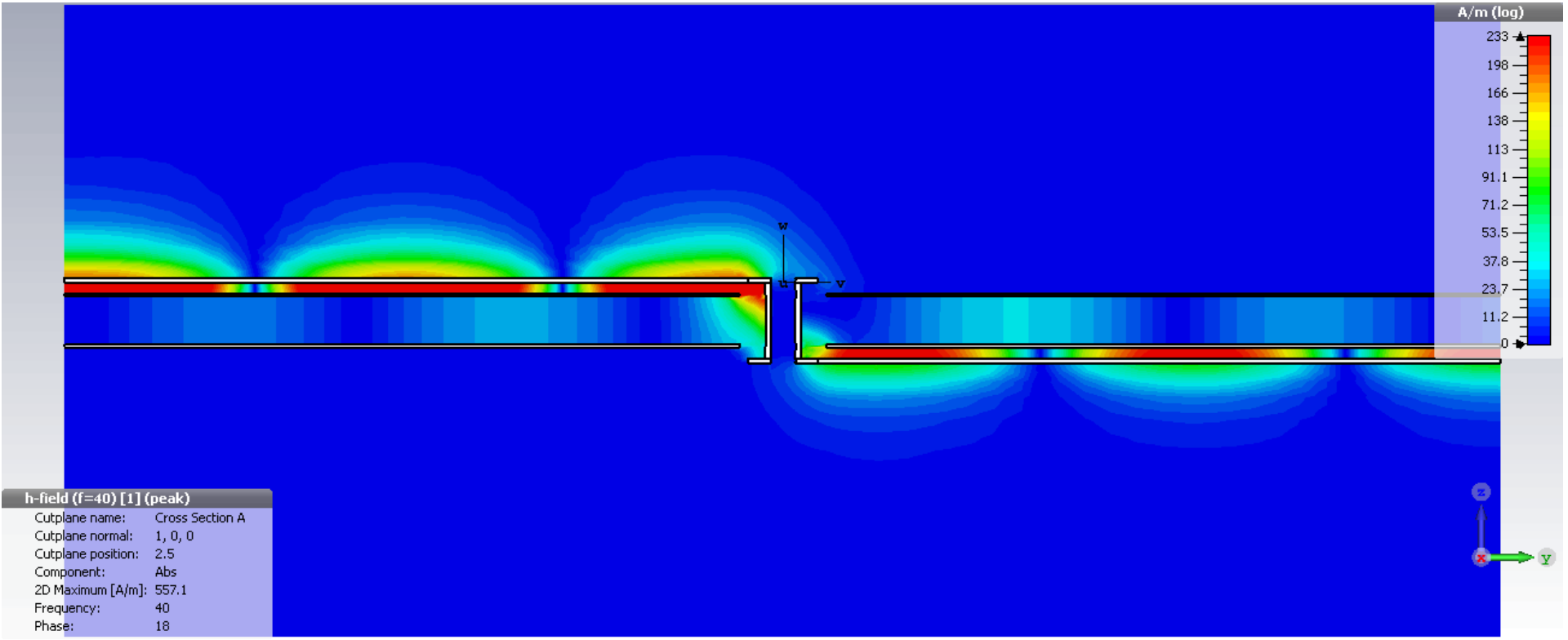




Drill size
Current flows on the outside of the hole

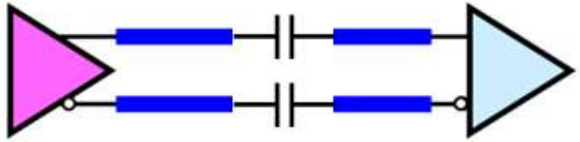
AC Losses

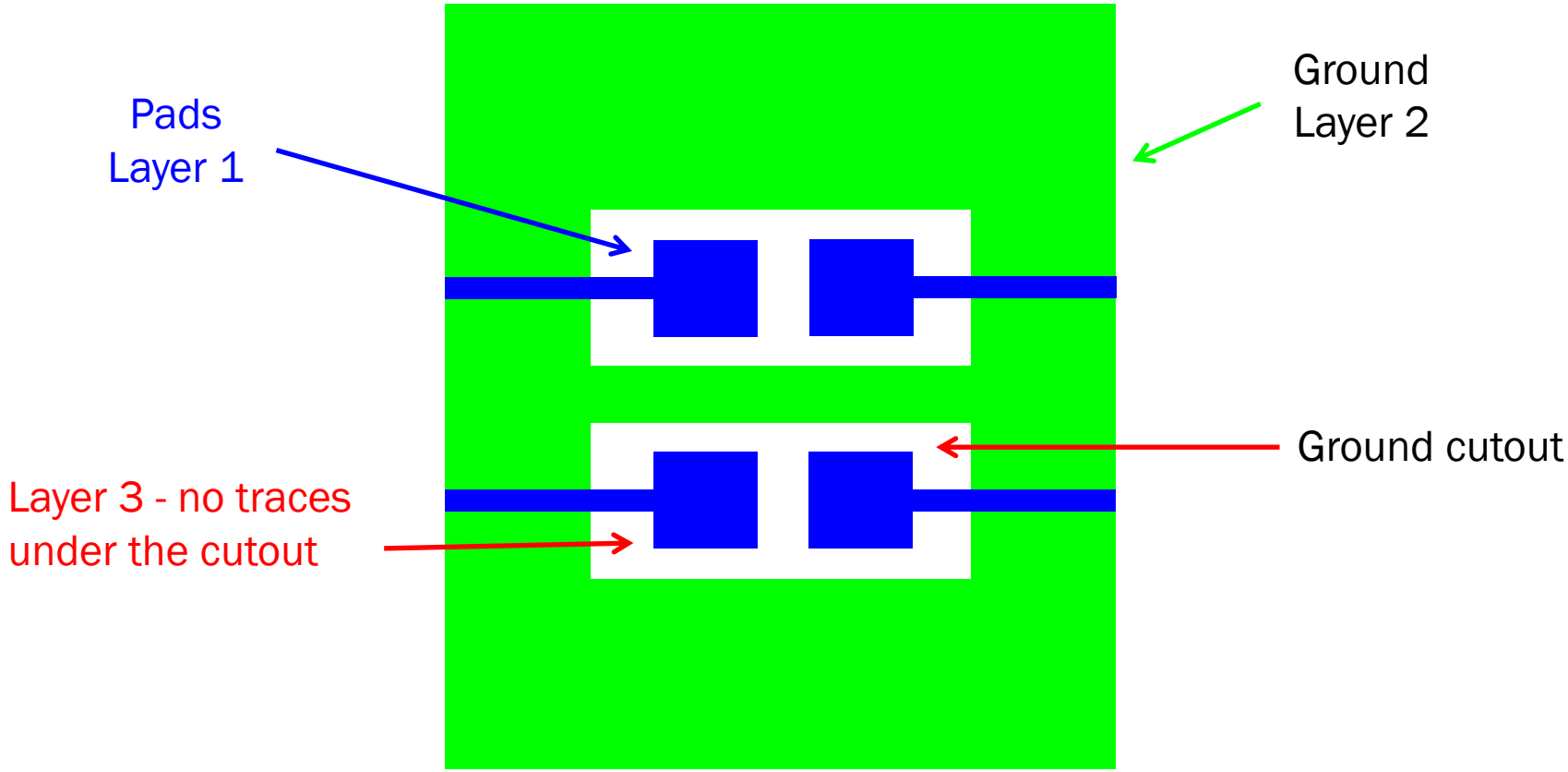
Current in a Via



Differential Pair Capacitors

Mounting Capacitance of Pads

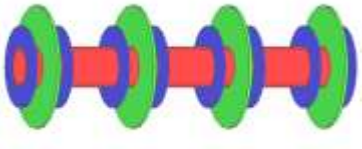


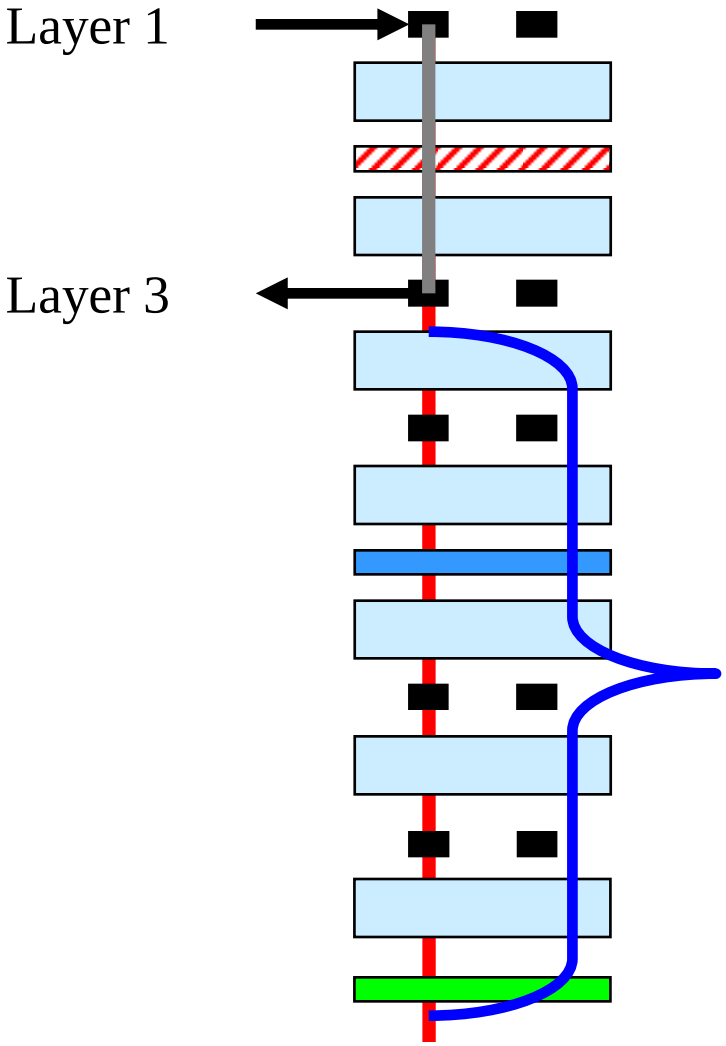


Do not forget placement tolerance

2 - 4mils / 50 - 100 µm

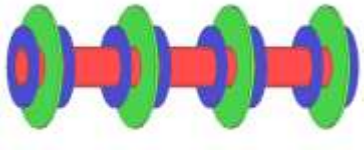
Via Properties
Stub Length

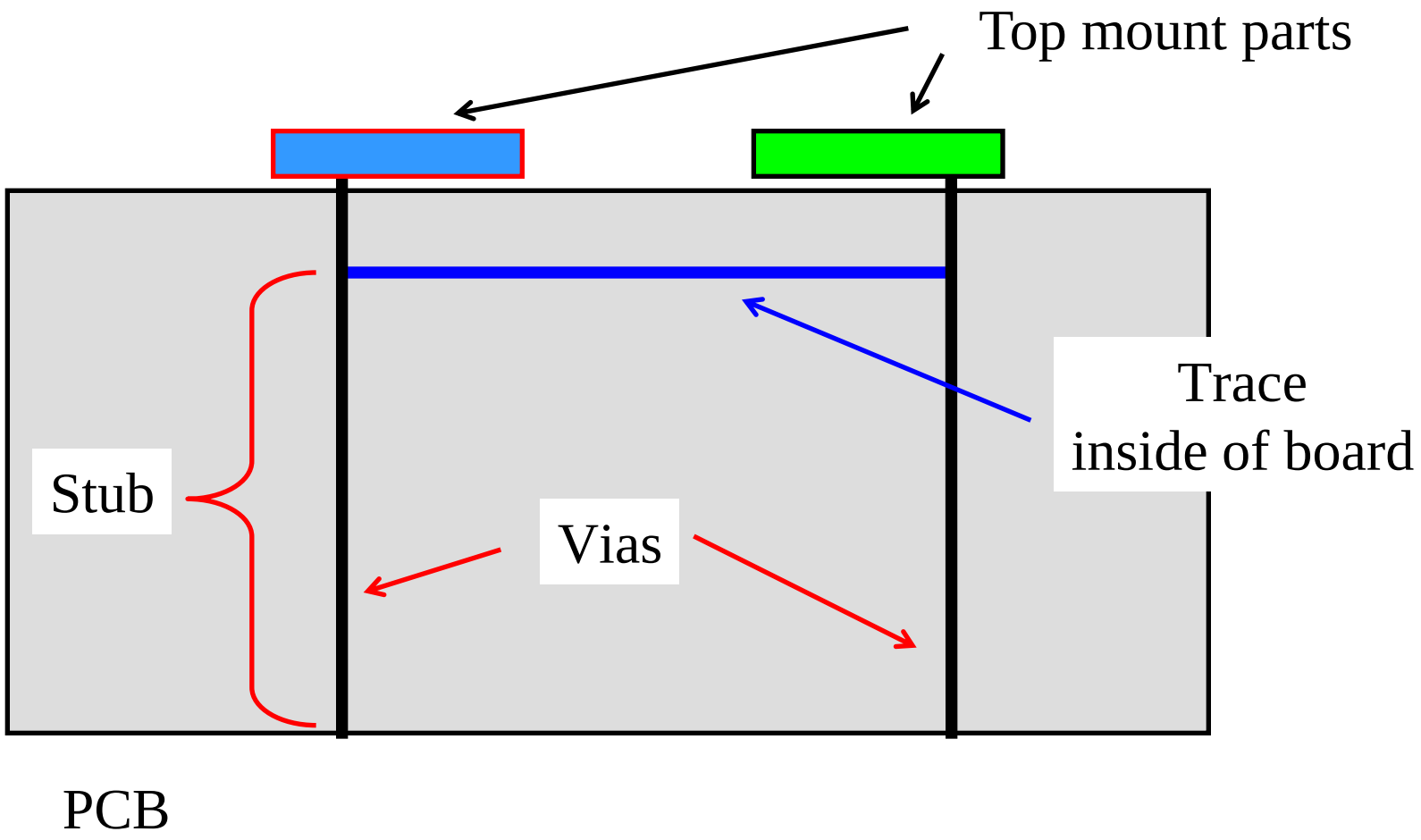




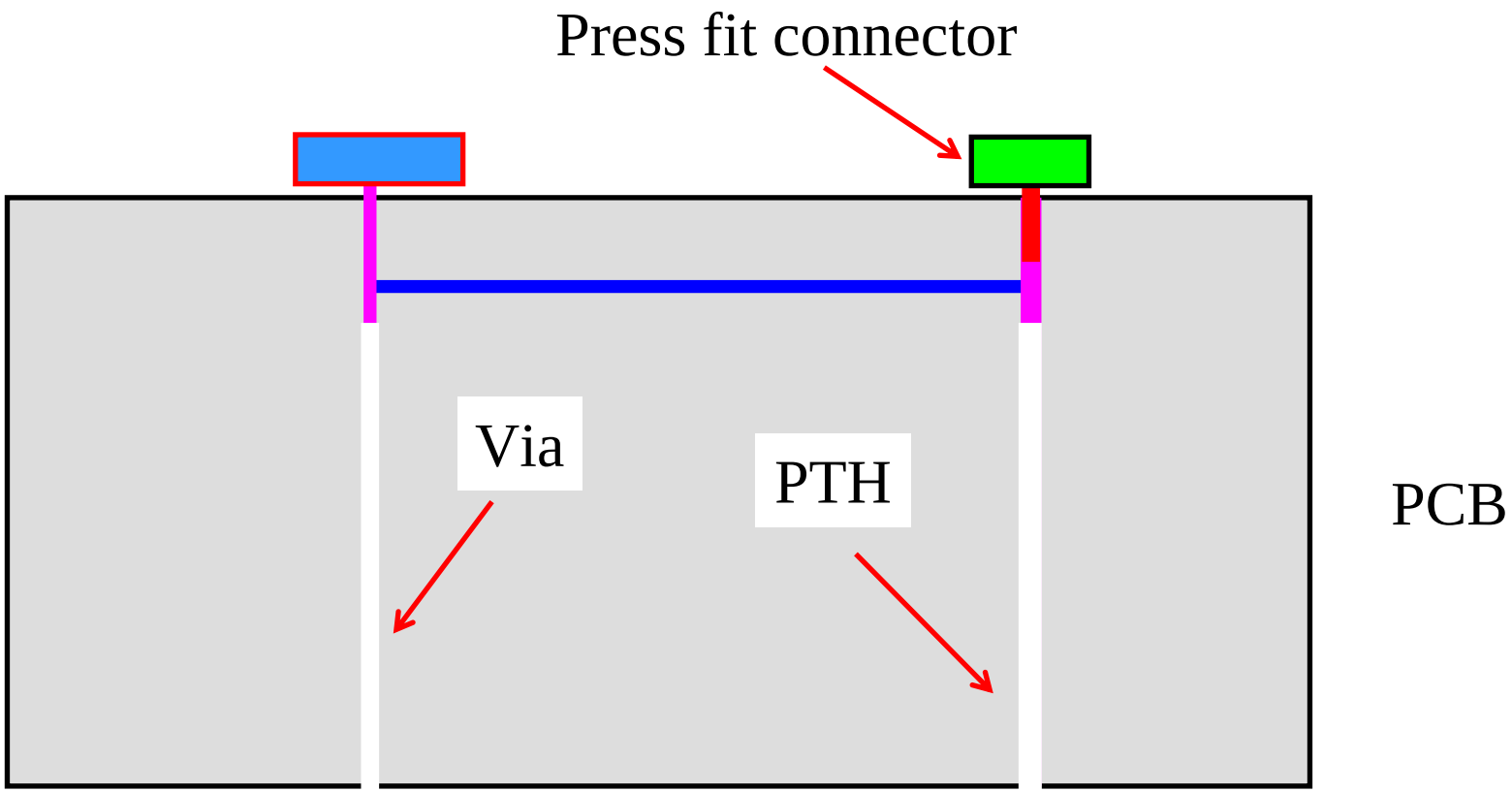
When is this length important

Via Stubs
Bad Routing

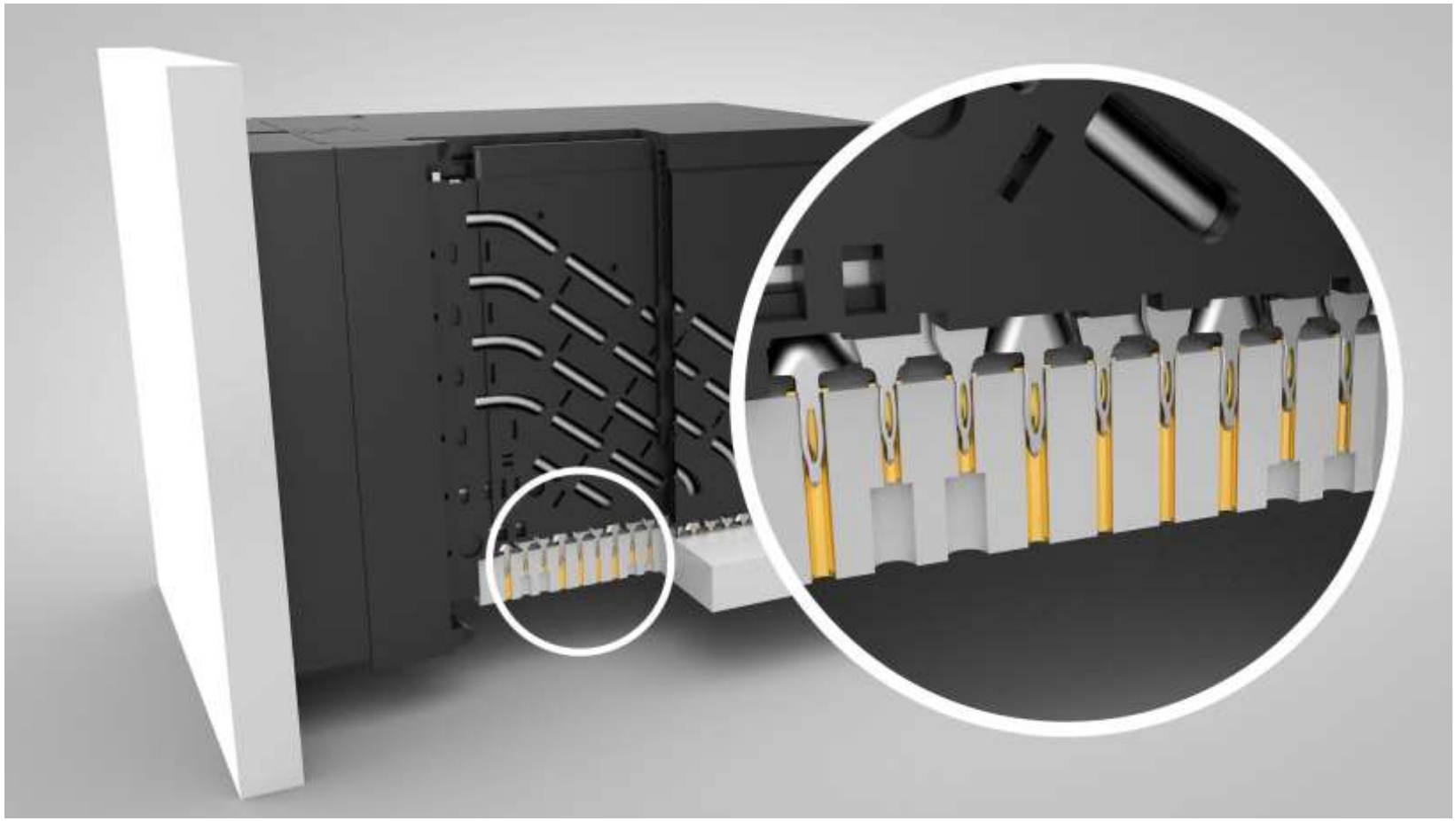




Via & PTH (Plated Thru Hole) Stubs
Backdrilling

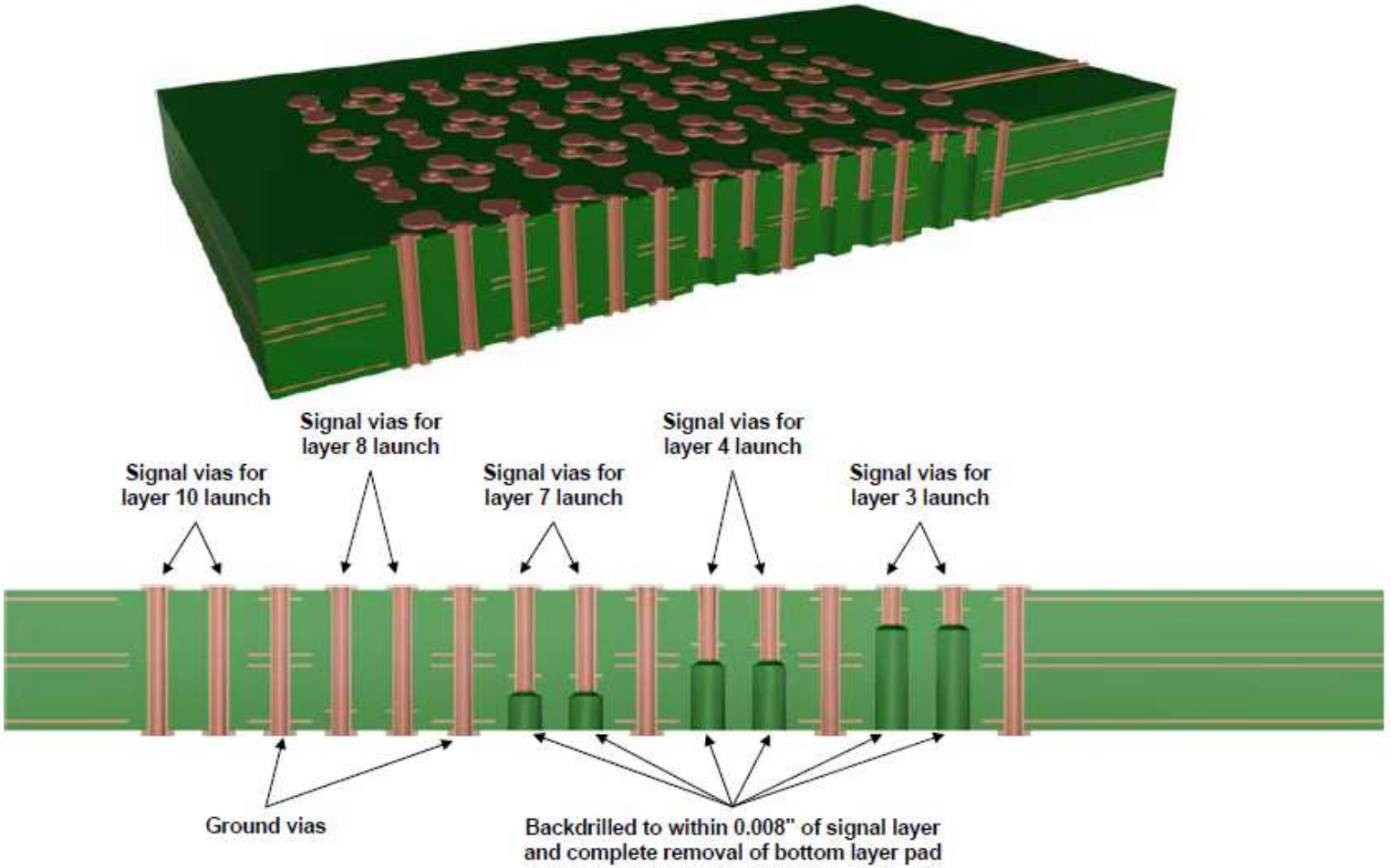


Via & PTH (Plated Thru Hole) Stubs
Press Fit Connectors



Samtec has many Press fit connectors

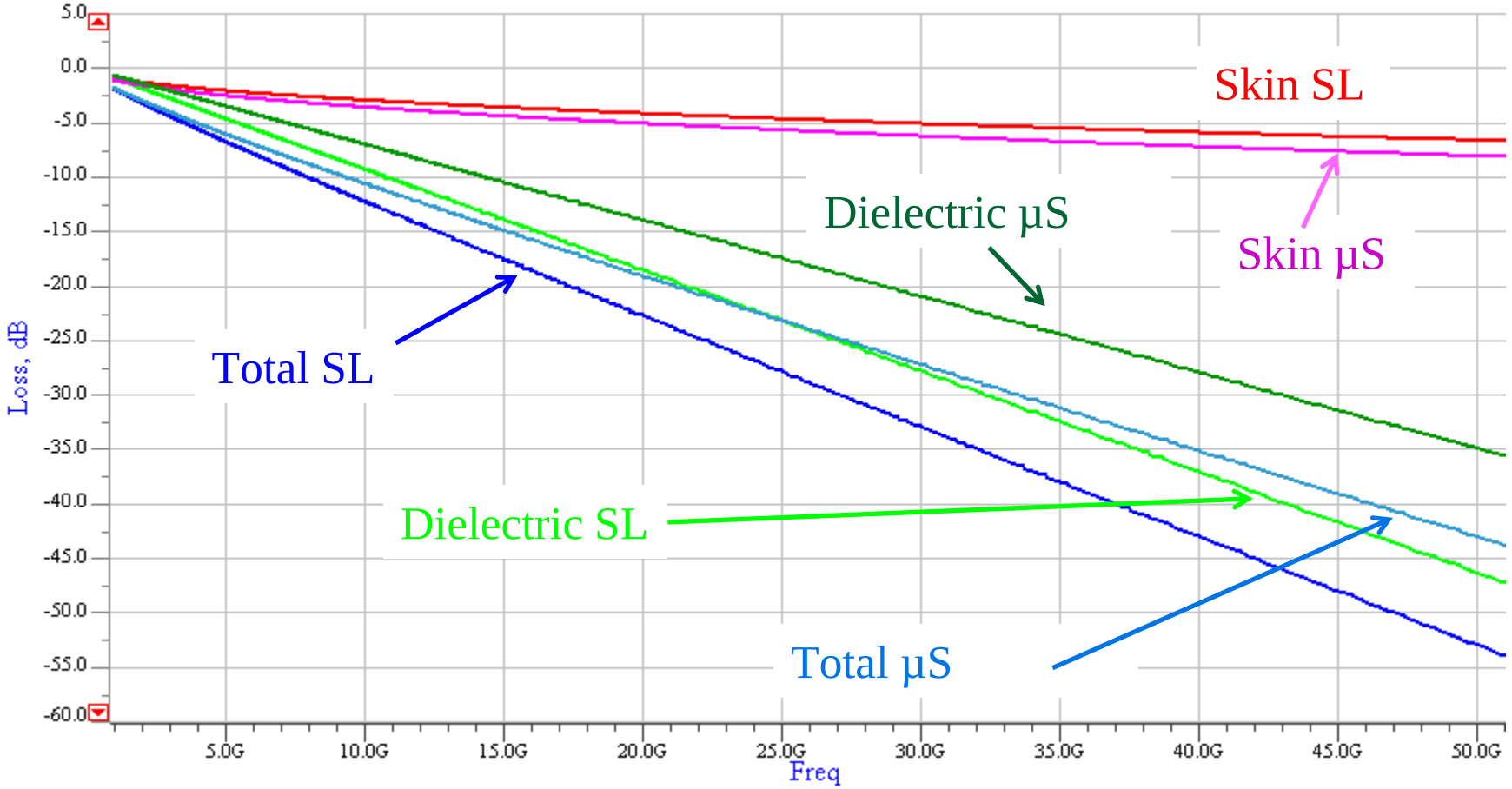
Backdrilling Options
Notice Layers 8 & 10



PCB Performance
Relative PCB Material Cost

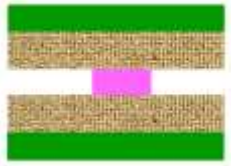
Material Name	Cost-Index-36 layer line card	Cost-Index-22 layer backplane	Loss-Df-10GHz	Skew Optmized
370-HR	1.00	1.00	0.02200	No
IS415	1.14	1.12	0.01200	No
FR408HR	1.65	1.62	0.00980	No
I-Speed	1.24	1.27	0.00700	No
Nelco-13 EP	2.37	2.30	0.00900	No
Megtron-4	1.63	1.69	0.00800	No
I-Speed IS	2.20	2.23	0.00550	Yes
Gigasync	2.86	2.90	0.00800	Yes
Nelco-13 EPSI	3.52	3.54	0.00800	No
I-Tera	2.82	2.82	0.00320	No
TerraGreen	3.03	3.02	0.00300	No
Megtron-6	3.32	3.51	0.00430	No
Tachyon/100G	4.09	4.39	0.00200	No

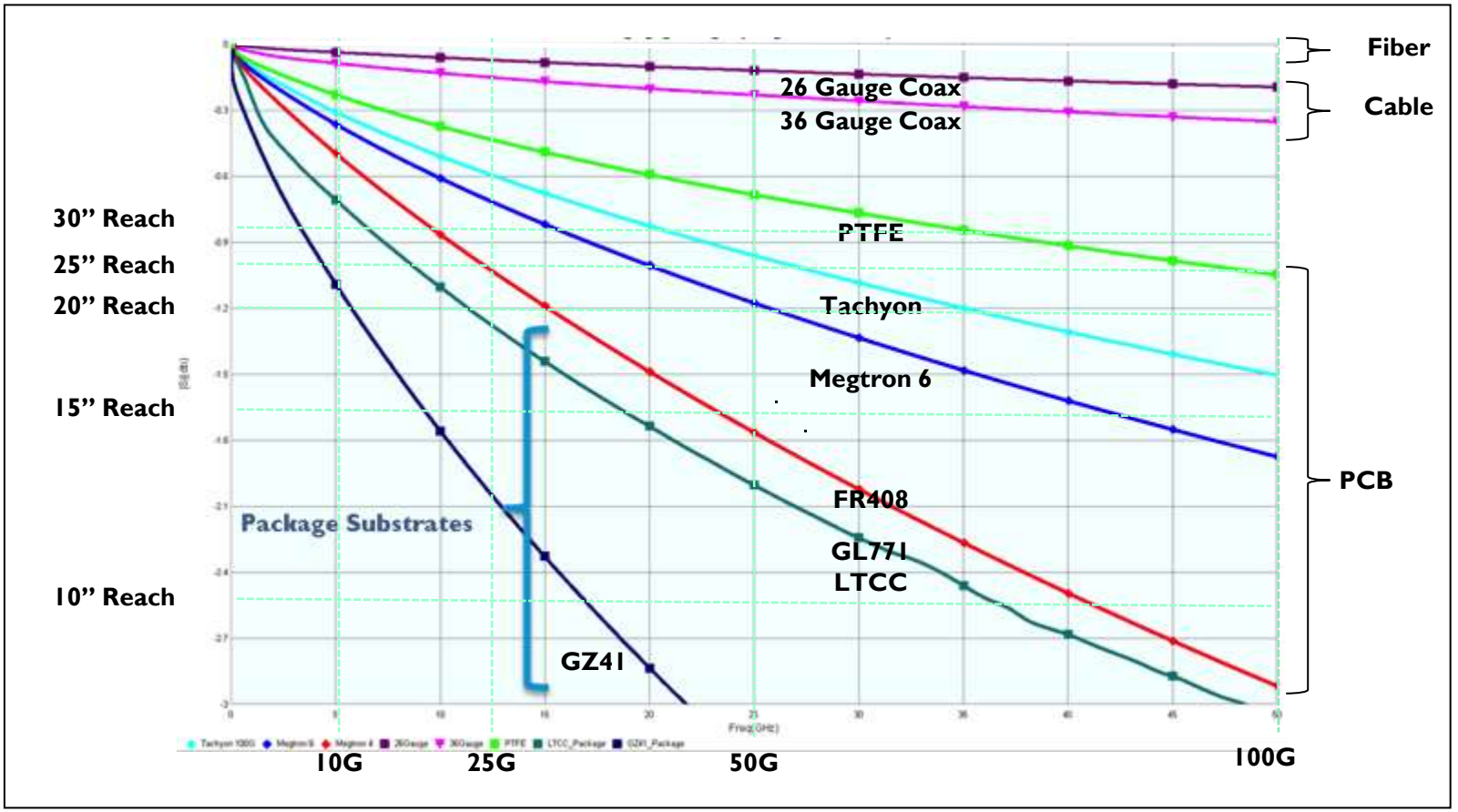
AC Losses 10 in / 25 cm Trace
Loss vs Frequency: 1 GHz → 50 GHz



Microstrip (µS) vs Stripline (SL)

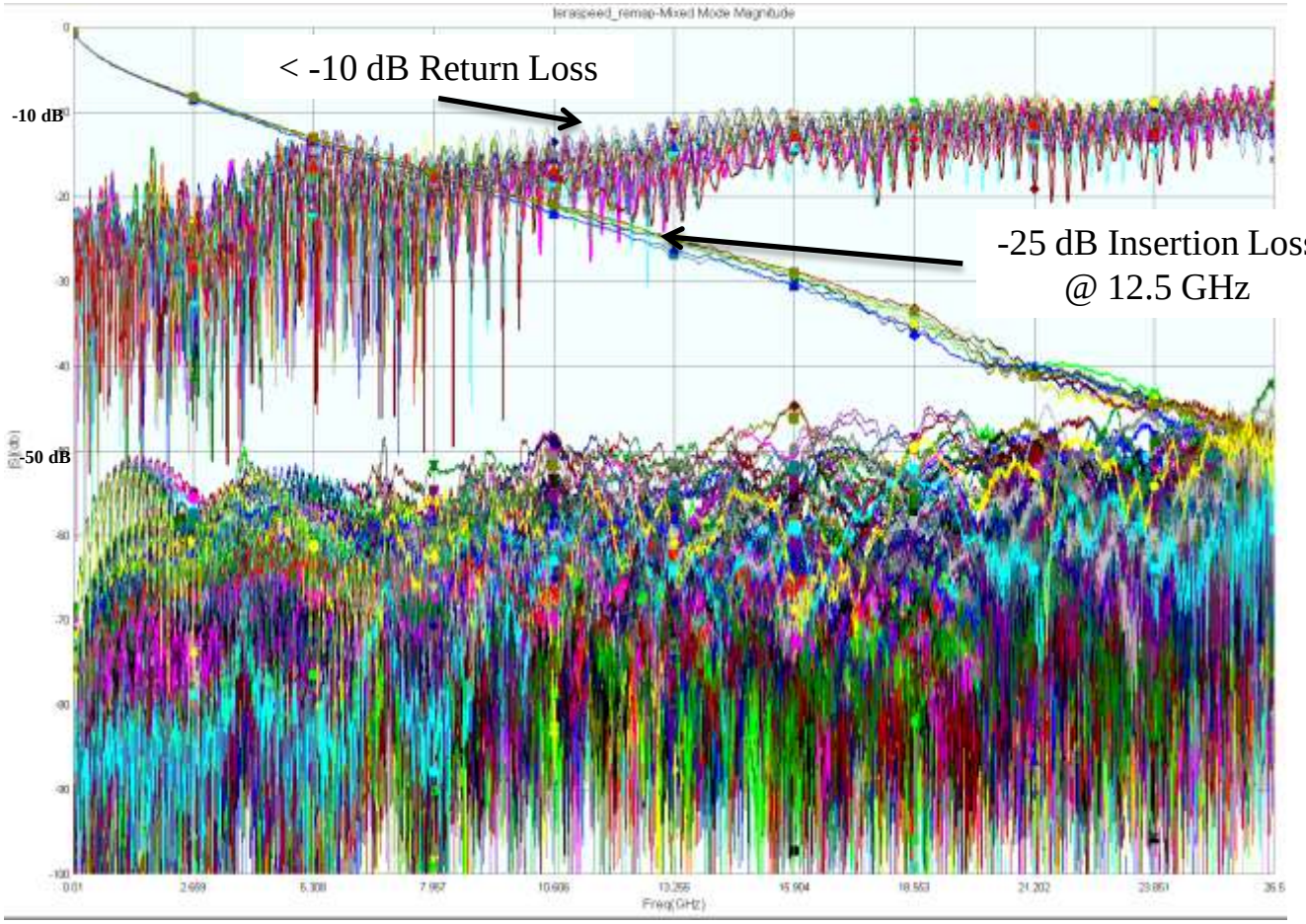
AC Losses Stripline Trace Normalized to One Inch





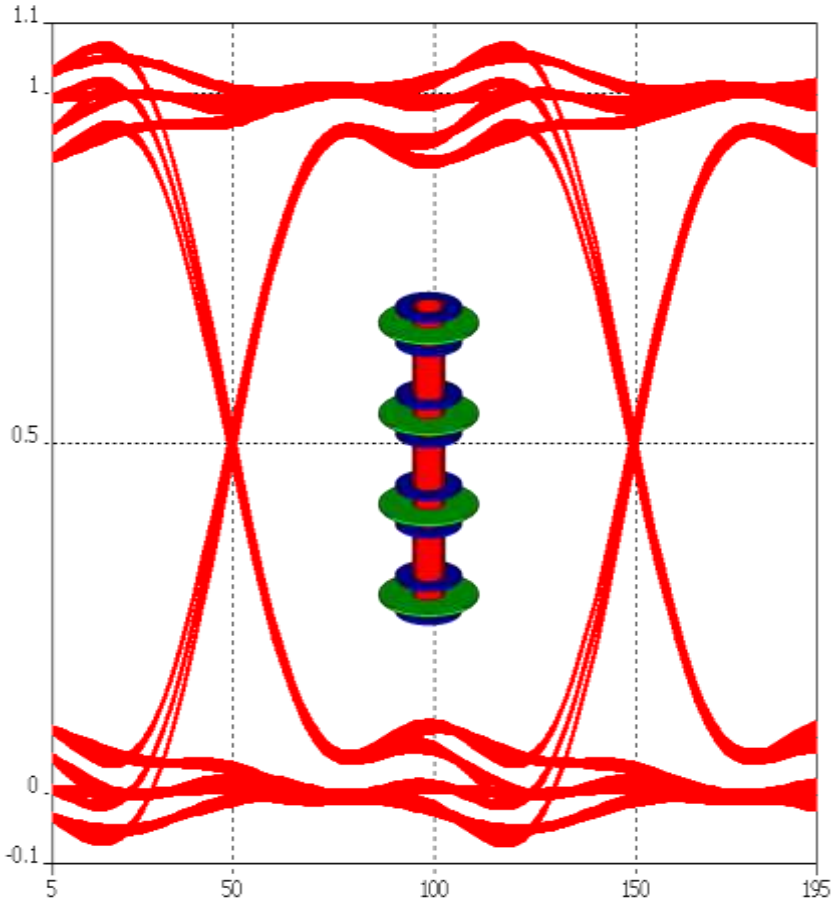
Normalized to 1 inch

Teraspeed Examax 29 Inch Total Length Backplane Eight Adjacent Differential Pairs

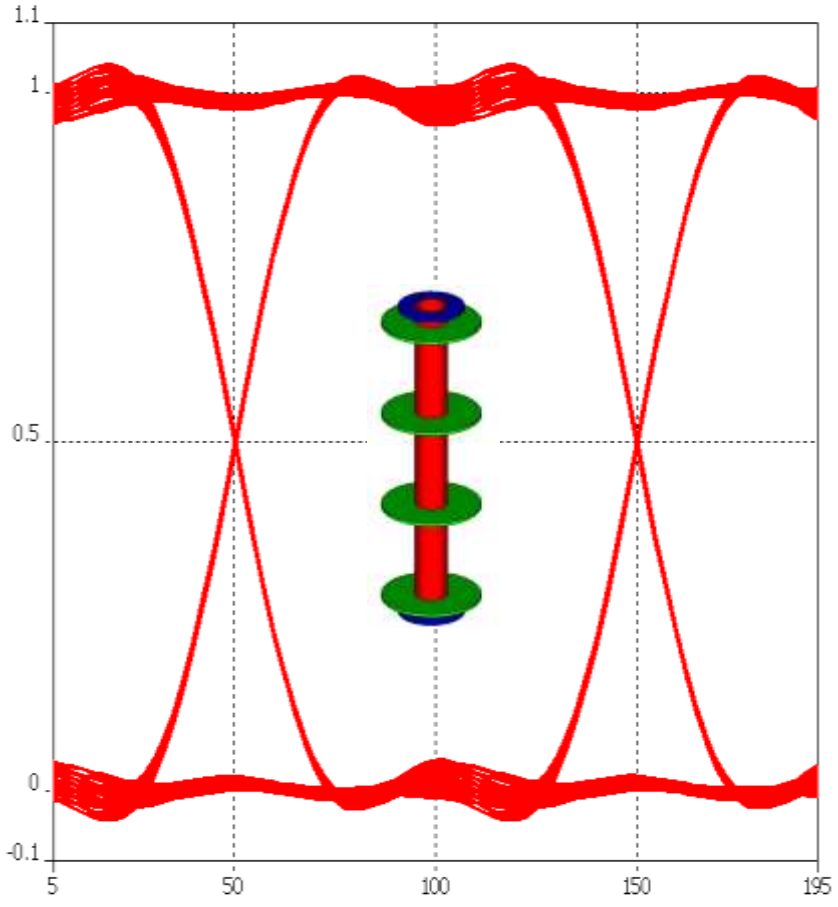


Low Crosstalk

Via Properties
12 Layer Better Pad Stack



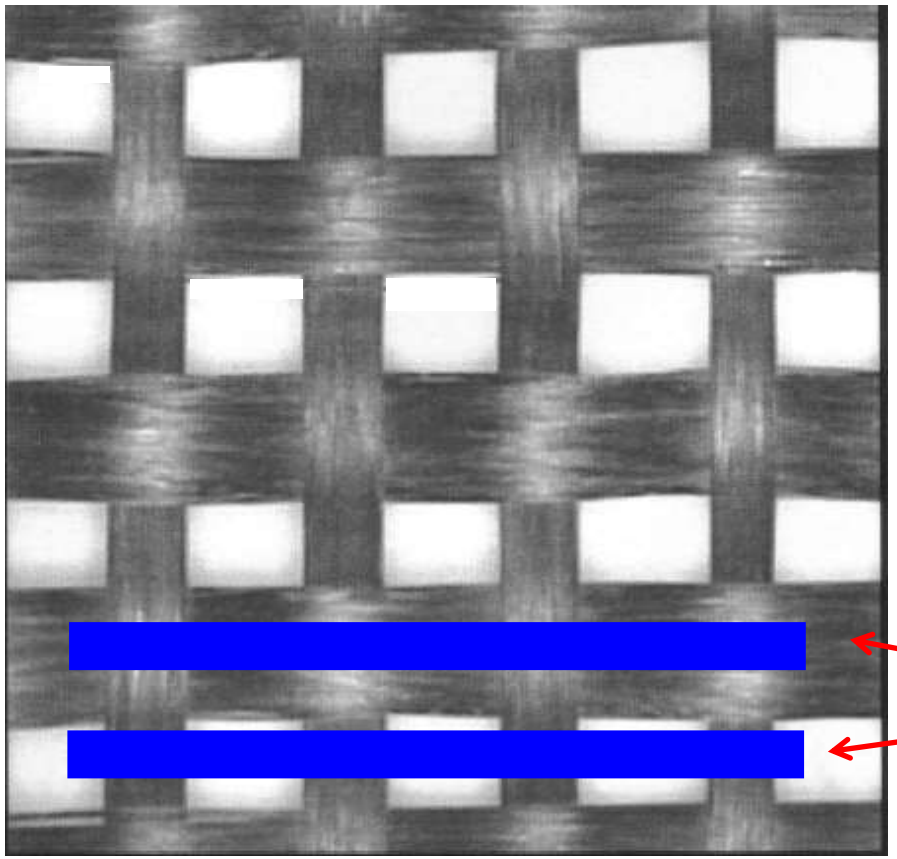
Normal via



High speed via

Fiber Weave Effect
FR4 Material Top View

$$v = \frac{v_{light}}{\sqrt{\varepsilon_r}}$$



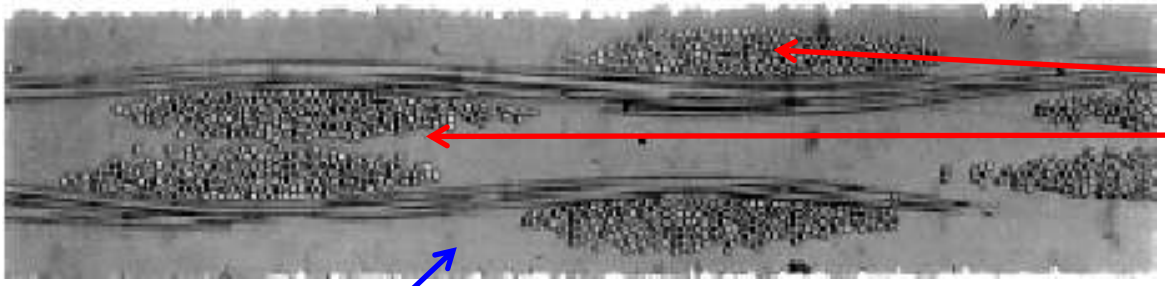
Pitch is 16.7 mils

Different ε_r 's then different trace velocity

1080

Fiber Weave Effect FWE

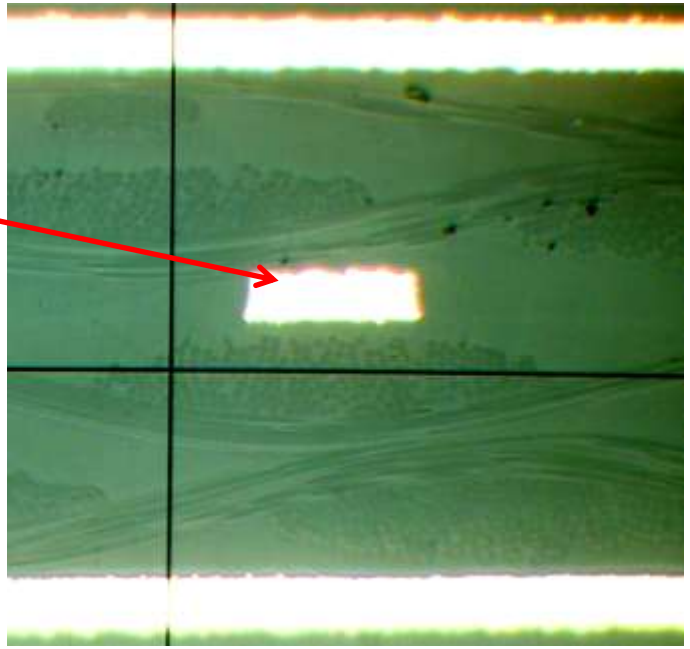
FR4 Material Side View



Fiberglass Bundles
$\varepsilon_r = 6.6$

Epoxy
$\varepsilon_r = 3.6$

5mil / 125 µm trace

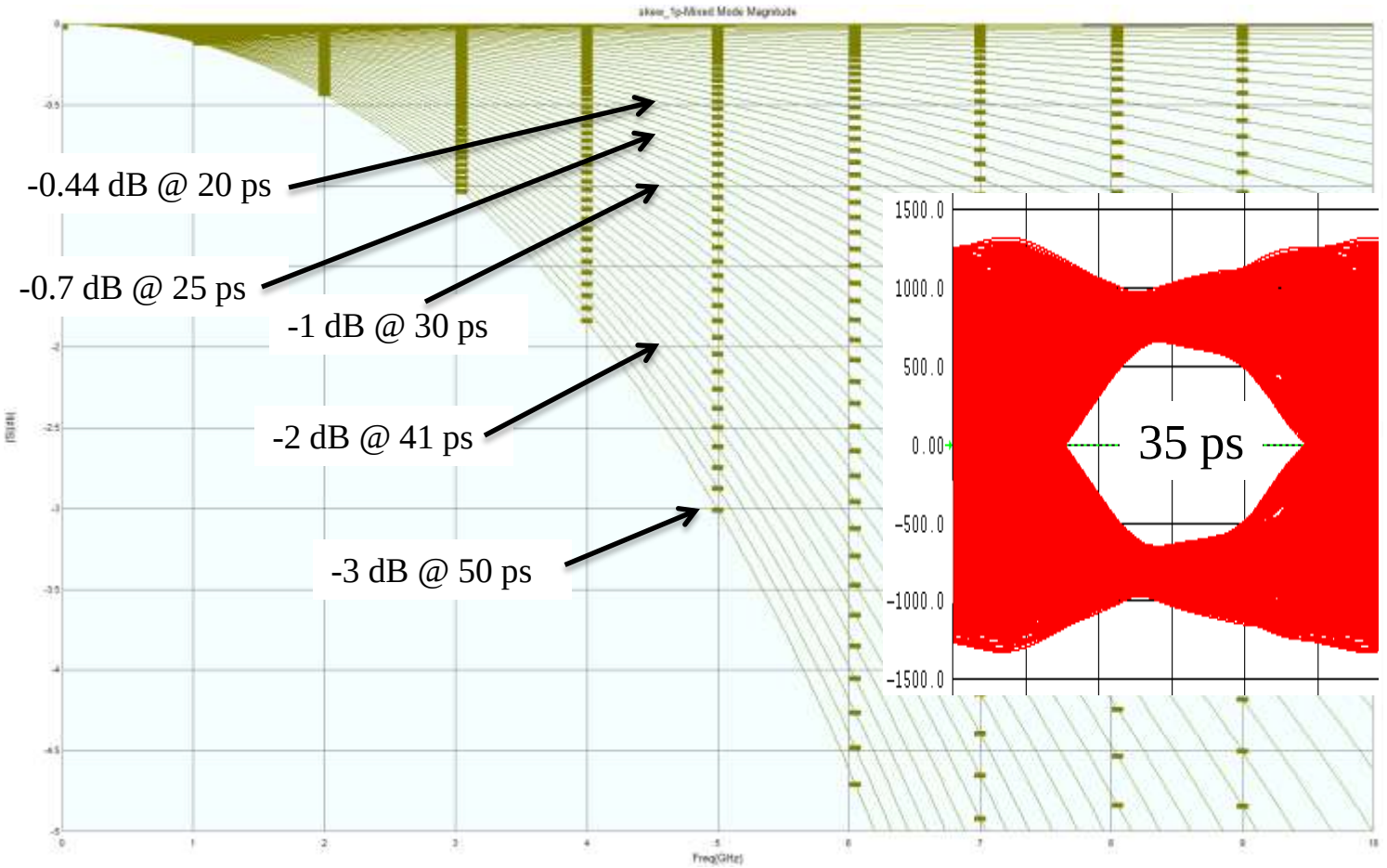


Non-homogeneous material has

ε_r variation due to glass/epoxy ratio

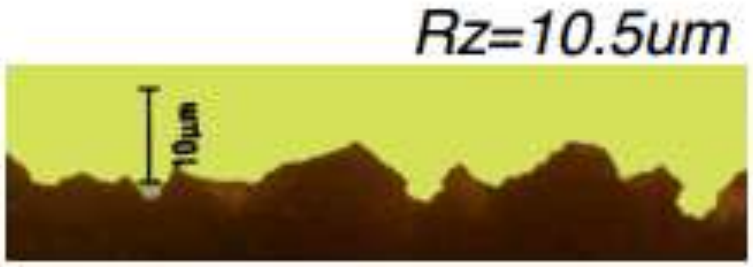
Fiber Weave Effect
Skew & Insertion Loss

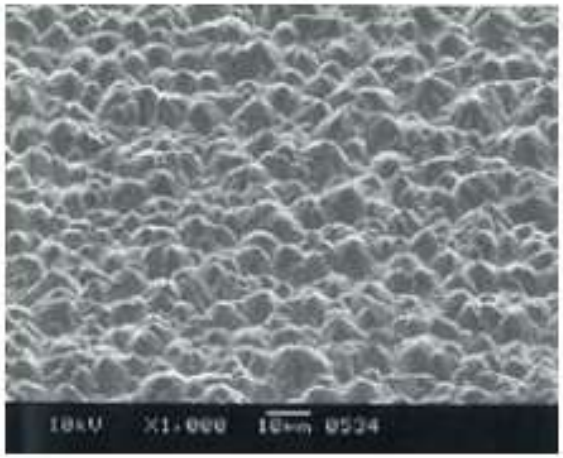
Ideal Insertion Loss Penalty vs. Skew (ps) for 10G



Skew loss becomes significant above 25 ps for 10 Gbps. These results can be scaled for different bit rates. For 6.25 Gbps -3 dB loss would occur at a skew of 80 ps, and -0.7 dB of loss at 40 ps of skew.

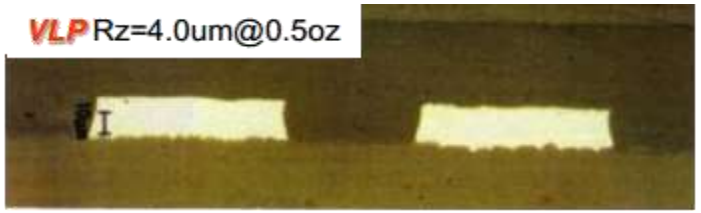
PCB Problems
Copper Roughness

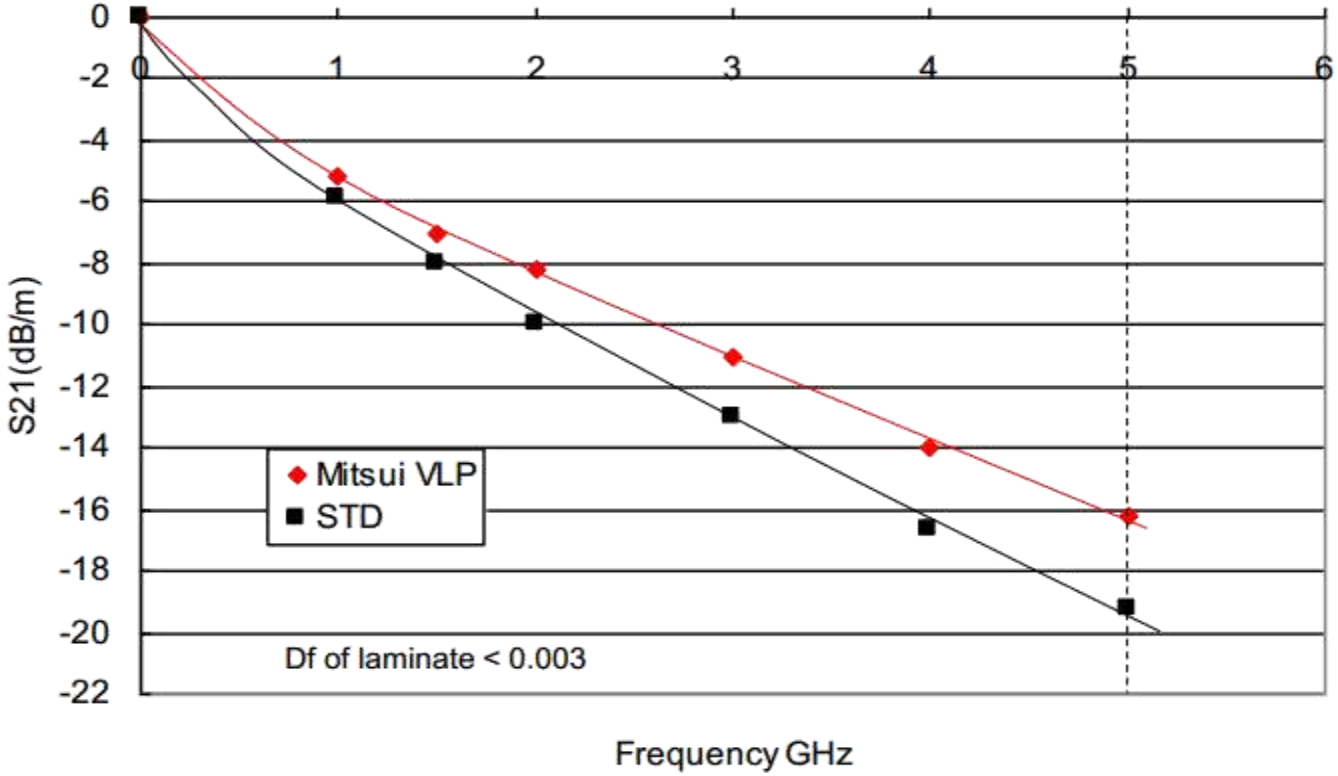




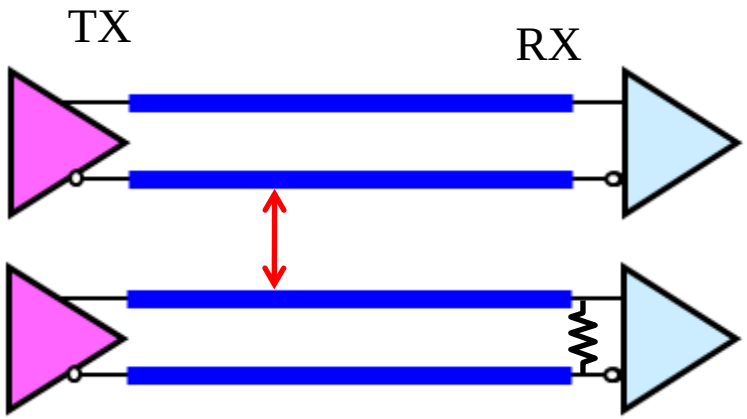
How "lossy" is the trace

PCB Problems
Copper Roughness - Losses





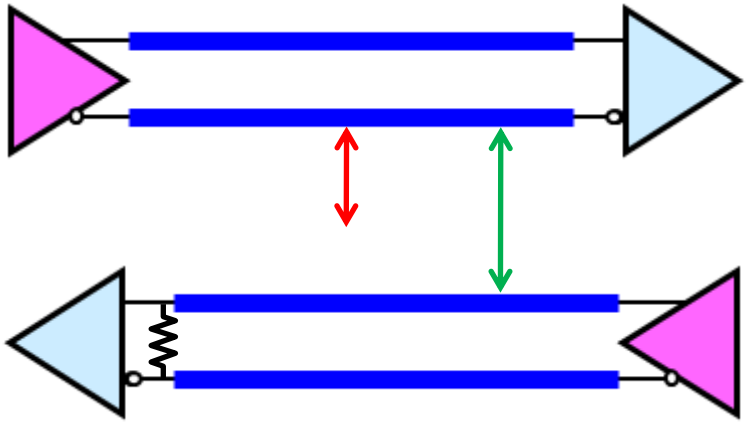
Differential Pair Rules
TX/TX, RX/RX or Larger Spacing



Crosstalk

TX aggressor to TX victim

- Reverse crosstalk is reflected by Rs of driver then smaller or Rs = Z_{odd} then no reflections
- Forward and reflected reverse are smaller at the receiver by board loss D_F



Crosstalk

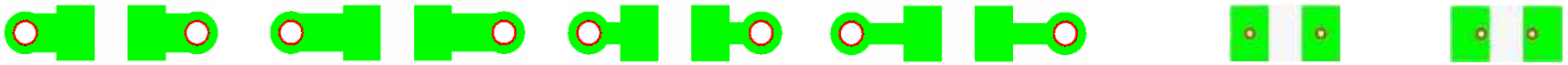
TX aggressor to RX victim

- Reverse crosstalk is terminated by Z_{Diff} so full voltage NEXT at RX

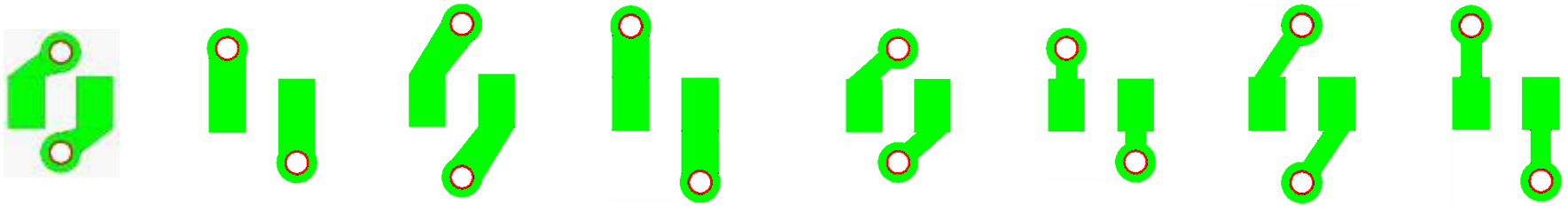
Capacitor Mounting Inductance
What Mounting Do You Use?

0402
pH

271 287 348 357 323 337 446 456



347 437 395 532 199 171



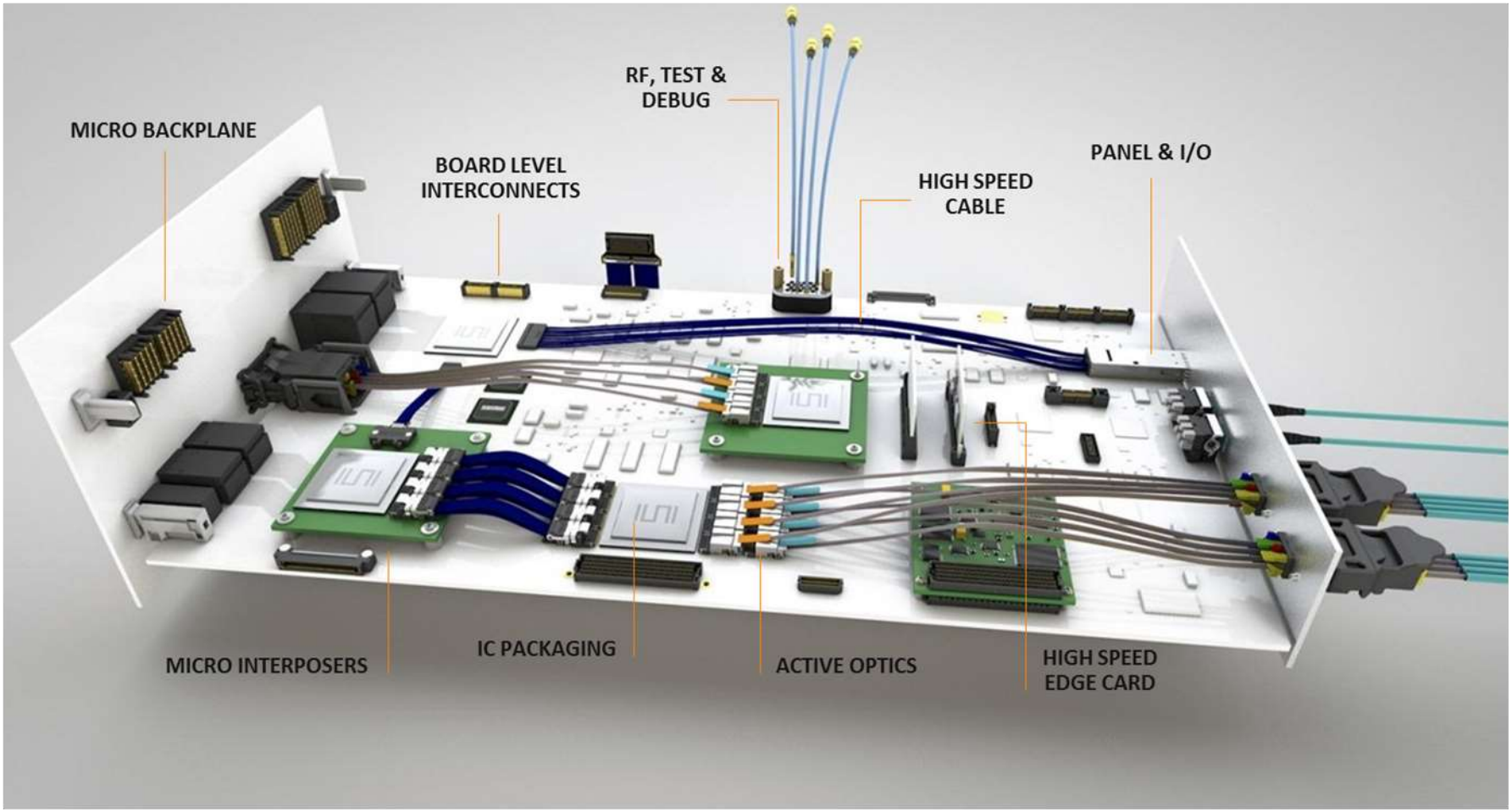
285 308 406 380 357 356 502 476

Functional or NOT

Simulate, Simulate and Simulate More

- How do you know if your design will work?
- Higher speeds means rules of thumb don't work
- Many PCB designers think that the rules that they used at 8 Gbp/s will work at 16, 20, 24, 28+
- Faster – need a SI/PI engineer
  - Part of the team
  - SI/PI consulting

Full Signal Channel Solutions



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