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RED320

Processor Board

Technical Reference Manual

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REVISION INFORMATION

DATE	REV	BY	CR	CHANGE
18/09/08	A00	CP/ELC	6309	This is the first version of this manual. It reflects the Rev B01 version of the PCB.

1 INTRODUCTION

The RED320, supporting components and software represent a powerful, easy to use embedded computing solution.

This document is the Hardware Technical Reference Manual for the RED320 product range including RED320 and REDCONN. It provides information on the board-level hardware and specifically includes:

- product specifications
- configuration information
- electrical characteristics
- interface pinouts
- details of EMC and ESD policies

Technical information on LaunchPad Application Development Kits for the RED320 is provided in separate documents. Specifically, details of hardware configuration and device driver implementations for a supported operating system can be found in the Platform Guide for that particular operating system. This Technical Reference Manual refers to the Platform Guide wherever hardware function is operating system dependent.

1.1 OVERVIEW

RED320 is a high performance credit card size single board computer optimized for use in embedded projects. RED320 combines the power of the Marvell® PXA320™ processor with a carefully selected set of peripherals optimized for high functionality, low power and small form factor. DSP Design has engineered the high risk elements of the system. You receive a fully tested module.

The RED320 is a RoHS compliant board. Low power consumption in normal operation and during sleep modes make the RED320 ideal for battery operated systems.

The RED320 operates as a standalone module requiring only a single 5V input. Alternatively customers can add the REDCONN - a services board for the RED320 - or use RED320 as a “super component” in their systems.

A preconfigured Windows CE operating system is available for the RED320. Development is speeded by the availability of the LaunchPad Application Development Kit for RED320.

1.2 RED320 FEATURES

- The PXA320 processor which uses the Intel XScale micro-architecture and complies with the ARM Architecture V5TE instruction set.
- High performance at very low power consumption.
- 128Mbytes of DDR SDRAM soldered to the board.
- 2Mbytes of NOR Flash, typically for boot loader.

- 512Mbytes of NAND Flash, typically for the operating system and file system.
- Two Secure Digital sockets allowing a range of SD cards to be used for memory or peripheral expansion.
- Three serial ports. COM1 is full function RS232, and COM2 and COM3 are limited function (Tx & Rx only) RS232 .
- 10/100 Base-T Ethernet port.
- Two USB 1.1 host ports.
- One USB 1.1 client port.
- 16-bit parallel TTL interface supporting a wide range of TFT LCDs at resolutions up to 800 x 600.
- AC97 codec providing mono microphone input, stereo line outputs, mono speaker output and four-wire resistive touch screen controller.
- Battery backed Real Time Clock.
- On-board temperature sensor.
- One I^2C multi-master serial bus providing simple expansion.
- 16-bit bus providing flexible expansion.
- 29 general purpose I/O signals for user I/O.
- Watchdog Timer generating cold and warm resets.
- The RED320 consumes very little power from a single 5V power supply even when operating at full speed. The operating system may switch off unused circuitry for extremely low power consumption in power managed states.
- 85mm x 65mm form factor.
- -20 to +85 deg C operating temperature range.

1.3 REDCONN SERVICES BOARD

The REDCONN connector board makes many of the interfaces on RED320 easy to use by routing them to standard connectors. This means that you can connect your RED320 directly to a wide range of peripherals including a serial port, audio, Ethernet network and USB devices.

REDCONN is available in two variants, which allows different powering schemes:

- REDCDC is powered from DC brick power supplies.
- REDCPOE is powered through Power over Ethernet (IEEE802.3af). PoE technology allows IP telephones, wireless LAN Access Points, webcams and many other appliances to receive power as well as data over existing LAN cabling, without needing to modify the existing Ethernet infrastructure.

REDCONN is an example interface board for RED320. Many projects will engineer an application-specific interface board with I/O suitable for the product. DSP Design call these interfaces “services boards”. Services boards can be produced by DSP Design or by the customer with assistance from DSP Design.

1.4 LAUNCHPAD APPLICATION DEVELOPMENT KIT

DSP Design strongly recommends that you begin your development project by using the LaunchPad Application Development Kit for RED320. This is a complete ready to use embedded computer system that is waiting for your application to be placed into the solid-state disk. Figure 1 shows the LaunchPad hardware. Not shown are the complete set of software, manuals and accessories (mouse, keyboard, PSU and cables) that are included in the LaunchPad Application Development Kit for RED320. The LaunchPad hardware comprises the following items mounted on a laptop style stand:

- RED320 processor board.
- REDCDC connector board.
- LCD and backlight inverter.
- Touch-screen.

FIGURE 1 - THE LAUNCHPAD FOR RED320

Using the LaunchPad Application Development Kit for RED320 will greatly reduce your development time, so your product will get to market sooner at a fraction of the engineering costs normally associated with products.

We have two objectives as you begin to use your new LaunchPad Application Development Kit for RED320. Firstly, we expect that within an hour of receiving your LaunchPad you will have set up the hardware, connected it to your LAN and run a simple demonstration. Secondly, we expect that within a day you will have installed the development tools, compiled a sample application, downloaded it to the target hardware, and experimented with debugging this application remotely from the host computer. So on

the second day you can begin developing your real application.

For full details of the LaunchPad Application Development kits see our web site at www.dspdesign.com/launchpad.

2 RED320 HARDWARE

2.1 BLOCK DIAGRAM

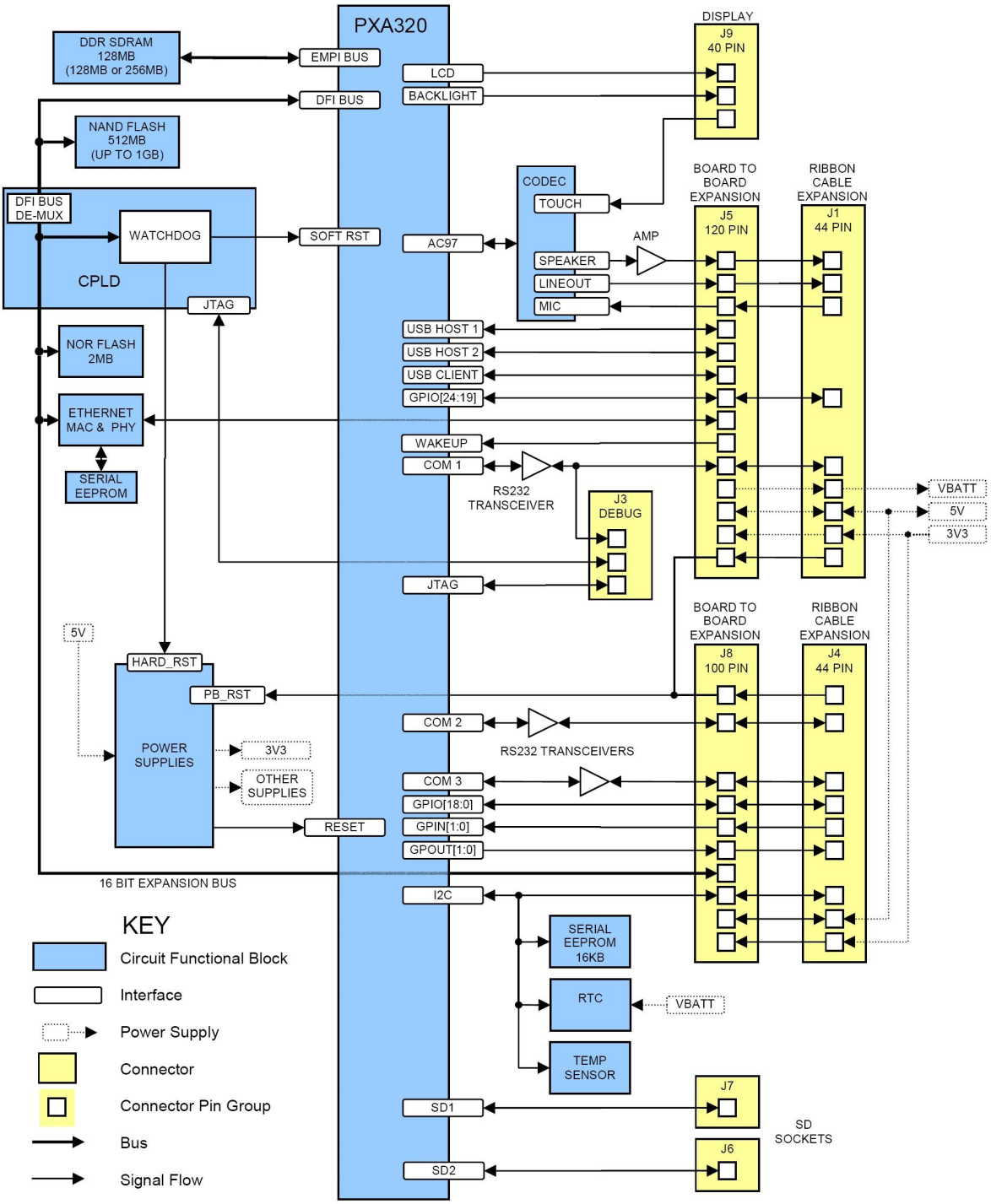

FIGURE 2 - RED320 BLOCK DIAGRAM

2.2 PROCESSOR AND MEMORY

2.2.1 Processor

The RED320 uses a PXA320 processor, which implements the Intel XScale micro-architecture and complies with the ARM Architecture V5TE instruction set (excluding the floating point instructions). This is an integrated system-on-a-chip microprocessor for high performance, dynamic, low-power portable hand-held and hand-set devices as well as embedded platforms. The chip contains a wide range of peripherals.

The PXA320 is available with clock rates of 624MHz and 806 MHz, and a 256 KB L2 cache. By default the 624MHz processor is fitted, but the 806MHz part is available for volume applications. Contact DSP Design if you require the faster part.

2.2.2 SDRAM

The PXA320 includes a 32-bit Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) memory interface.

The RED320 provides 128Mbytes of DDR memory as standard, soldered to the PCB. For volume applications there is an option for 256Mbytes. Contact DSP Design if you require more memory.

Some of the DDR SDRAM is allocated to the internal LCD controller, using a technique referred to as unified memory architecture (UMA).

2.2.3 Flash Memory

The RED320 provides 2Mbytes of NOR Flash as standard, soldered to the PCB. This is typically used for a boot loader. In the case of Windows CE the NOR flash contains the EBOOT loader (when then copies itself to RAM and executes from there).

The RED320 provides 512Mbytes of NAND Flash as standard, soldered to the PCB. There are options for 256M bytes and 1G bytes for volume applications. Contact DSP Design if you require more or less memory. The NAND Flash is connected to the PXA320 processor via the shared system bus.

The NAND Flash typically contains the operating system and non-volatile storage. In the case of Windows CE the NAND flash contains the NK.bin operating system image and file storage.

2.2.4 Serial EEPROM

The RED320 provides an option for a serial EEPROM connected to the I^2C bus, but this is not fitted as standard. A serial EEPROM could be fitted to provide up to 16Kbytes of storage, for users with a volume requirement. Contact DSP Design if you require a serial EEPROM.

2.3 SECURE DIGITAL SOCKETS

The RED320 provides two Secure Digital (SD) sockets suitable for 3.3V memory and I/O cards, providing both memory and peripheral expansion. SD cards can be fitted in the sockets J6 and J7. The high-capacity SDHC cards are supported by the hardware controller. Please refer to the Platform Guide for the relevant operating system for further details.

Power switching circuitry is provided to power down the SD cards, to reduce system power consumption and provide hot swap capability.

The RED320 provides ESD protection on all SD card signals. EMC filtering is not required or provided as the connections to the SD socket will remain within an enclosure. The metal parts of the SD sockets connect to a separate CHASSIS ground, which also connects to the mounting hole closest to J6.

2.4 DISPLAY

The RED320 provides a 16-bit TFT LCD interface. Table 1 lists the signals associated with the LCD interface. (Note that connector J9 also carries touch-screen signals. See section 2.5).

The LCD controller is implemented in the PXA320 processor. It is capable of driving colour LCD panels with resolutions up to 800 x 600.

The parallel digital interface has been designed to be compatible with a range of interface boards from DSP Design, allowing connection to a variety of common displays. At present DSP Design offers three TFT LCD interface boards which can be used with the RED320. The TFTIF31, TFTIF41 and TFTIFKYV boards interface to TFT LCDs with conventional parallel interfaces (6 bits of red, green and blue, plus timing signals). Details of the interface boards are provided in Appendix D.

The PXA320 produces 16 bits of display data (5 bits of red and blue and 6 bits of green). Many displays will have 18 or even 24 data bits. In this case the displays' least significant bits should be connected to GND. This is done automatically with the RED320 and DSP Design's LCD interface boards.

Several TFT panels from different manufacturers have been successfully tested with the RED320. Please refer to the Platform Guide for the relevant operating system for further details.

Solder link LK6 is used to route either VCC_5V or LCD_ADJ to J9 pin 33. By default VCC_5V is connected. However, the 2-3 position should be set if using the TFTIFKYV with Kyocera displays. LK6 is set as follows:

- Link 1-2 to connect VCC_5V to J9 pin 33 (default setting).
- Link 2-3 to connect LCD_ADJ to J9 pin 33.

Pin 1 of LK6 is that closest to RP14. It can be located using Figure B2 in Appendix B.

The LCD_ADJ signal is a pulse width modulated output which can be used to adjust the brightness of backlight inverters. It is configured by the operating system. Please refer to

the Platform Guide for the relevant operating system for further details.

This interface is intended to remain within an enclosure and not be accessible by the end user. EMC filtering and ESD protection is therefore not provided on the RED320, although series resistors are present on the LCD signals to reduce ringing. Connections to the LCD should be kept as short as possible to reduce electrical noise.

SIGNAL	J9 PIN	DESCRIPTION
BKL_EN	1	Backlight Enable
LCD_EN	2	LCD Power Enable
LCD_DCLK	4	Pixel Clock
LCD_HSYNC	6	Horizontal Sync
LCD_VSYNC	8	Vertical Sync
GND (R0) (1)	11	Red Colour Bus
LCD_R1	12	
LCD_R2	14	
LCD_R3	15	
LCD_R4	16	
LCD_R5	18	
LCD_G0	22	Green Colour Bus
LCD_G1	23	
LCD_G2	24	
LCD_G3	26	
LCD_G4	27	
LCD_G5	28	
GND (B0) (1)	32	Blue Colour Bus
LCD_B1	34	
LCD_B2	35	
LCD_B3	36	
LCD_B4	38	
LCD_B5	39	
LCD_DE	40	Data Enable
LCD_ADJ (2)	33	Backlight PWM Control

NOTES:

1) J9 supports a generic LCD interface used on all DSP Design processor boards, some of which support 18bpp. On the PXA320 the R0 and G0 signals are connected to GND.
2) See note on solder link LK6.

TABLE 1 - RED320 LCD SIGNALS

Table 2 provides the electrical characteristics for the LCD interface signals.

SIGNAL	PARAMETER	CONDITION	LIMITS			UNITS
			Min	Typ	Max	
LCD_DCLK, LCD_HSYNC, LCD_VSYNC, LCD_DE LCD_R[5:1], LCD_G[5:0], LCD_B[5:1], BKL_EN, LCD_EN, LCD_ADJ	V_{OH}	I_{OH} = -1mA	0.9 * VCC_3V3	-	VCC_3V3	V
	V_{OL}	I_{OL} = 1mA	GND	-	0.1 * VCC_3V3	V

TABLE 2 - RED320 LCD INTERFACE ELECTRICAL CHARACTERISTICS

2.5 TOUCH-SCREEN

The RED320 provides a four-wire resistive touch-screen interface. Table 3 lists the signals associated with the touch-screen. (Note that connector J9 also carries LCD signals. See section 2.4).

SIGNAL	J9 PIN	DESCRIPTION
TSXP	9	Touch-screen top contact
TSXN	10	Touch-screen bottom contact
TSYP	31	Touch-screen right contact
TSYN	30	Touch-screen left contact

TABLE 3 - RED320 TOUCHSCREEN SIGNALS

When the processor is placed into sleep mode it is possible for a touch on the touch-screen to wake the processor. Please refer to the Platform Guide for the relevant operating system for further details.

Figure 3 shows the RED320 touch-screen controller interfacing to a four-wire resistive touch-screen. The touch-screen controller is implemented within the WM9713 audio codec which interfaces to the PXA320 processor via the AC97 bus.

The touch screen signals are designed for connecting to a resistive four-wire touch screen. Do not connect them to anything else.

The RED320 provides EMC filtering and ESD protection on all touch-screen signals.

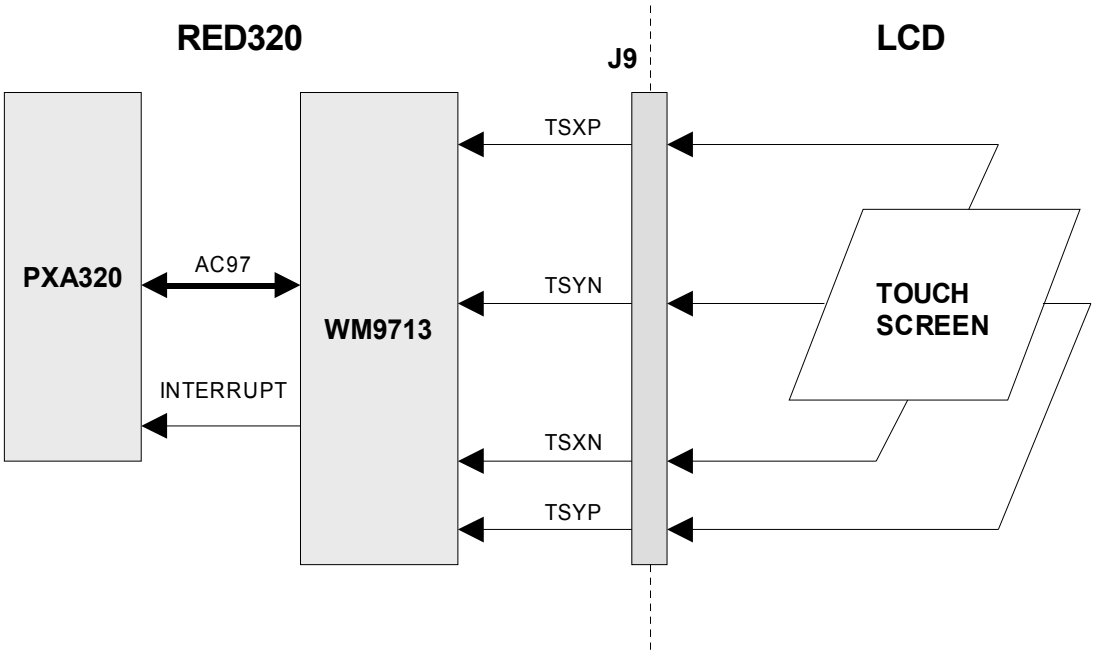

FIGURE 3 - RED320 TOUCH-SCREEN BLOCK DIAGRAM

2.6 SERIAL PORTS

The RED320 provides three RS232 serial ports labelled COM1, COM2 and COM3. Table 1 lists the signals associated with the three serial ports.

SIGNAL	CONNECTOR - PIN	DESCRIPTION
DCD1	J1-1, J5-1	COM1 RS232 carrier detect input
RXD1	J1-3, J5-2	COM1 RS232 receive data input
TXD1	J1-5, J5-3	COM1 RS232 transmit data output
DTR1	J1-7, J5-4	COM1 RS232 data terminal ready output
DSR1	J1-2, J5-61	COM1 RS232 data set ready input
RTS1	J1-4, J5-62	COM1 RS232 request to send output
CTS1	J1-6, J5-63	COM1 RS232 clear to send input
RI1	J1-8, J5-64	COM1 RS232 ring indicator input
TXD2	J4-42, J8-76	COM2 RS232 transmit data output
RXD2	J4-44, J8-77	COM2 RS232 receive data input
TXD3	J4-26, J8-85	COM3 RS232 transmit data output
RXD3	J4-28, J8-86	COM3 RS232 receive data input

TABLE 4 - RED320 SERIAL PORT SIGNALS

Each UART is functionally compatible with the industry standard 16550A UART and can be independently configured for 5-8 data bits, 1-2 stop bits, even, odd or no parity and baud rates supported by the operating system. The maximum baud rate is 115.2k baud.

COM1 is a standard full function eight-wire RS232 port, supporting three transmit signals (TXD, RTS and DTR) and five receive signals (RXD, CTS, DCD, DSR and RI).

COM2 and COM3 are two-wire RS232 ports supporting TXD and RXD only.

The serial ports can be powered off in order to conserve power. In this case the outputs become tri-state and the PXA320 sees all inputs as inactive. The default at reset is that the serial ports are enabled.

The serial ports are compliant with the EIA/TIA-232 and V.28/V.24 specifications. Typical voltage swings on the output signals are +/- 5V when loaded with 3kΩ to ground. Maximum short circuit output current is 60mA.

Damage may occur if voltages on input signals exceed +/-25V on input signals and +/-13V on output signals.

Each port uses ICL3243E transceivers, which provide ±15KV ESD protection (IEC61000-4-2 Air Gap and Human Body Model).

EMC filtering is not provided on these signals on the RED320. It is the user's responsibility to ensure that systems using the RED320 and a compatible services board are compliant with the appropriate EMC standards.

The REDCONN provides EMC filtering on all these signals.

2.7 ETHERNET

The RED320 provides a single IEEE 802.3/802.3u compliant 10/100-Base-TX Ethernet port. The Ethernet port is implemented in the LAN9215 Ethernet controller chip which has an integrated MAC and PHY.

Table 5 lists the signals associated with the Ethernet port.

SIGNAL	J5 PIN	DESCRIPTION
RDP	26	Differential pair receiving data positive
RDN	27	Differential pair receiving data negative
LAN_3V3A	86	3.3V power to centre-tap of receive transformer.
TDP	29	Differential pair transmitting data positive
TDN	30	Differential pair transmitting data negative
LINK#	89	Controls LINK status LED in the RJ45 connector.
10/100#	90	Controls LAN activity LED in the RJ45 connector.

TABLE 5 - RED320 ETHERNET SIGNALS

Figure 4 shows the RED320 Ethernet block diagram and a typical services board block diagram. The 16-bit LAN9215 Ethernet controller chip interfaces to the PXA320 processor via the 16-bit shared system bus. The transmit and receive differential pairs interface directly to expansion connector J5, from where they travel to an isolation transformer and then the RJ45 Ethernet connector.

The REDCONN Services Board includes the transformer and RJ45 socket. The socket contains two LEDs. The LINK# signal drives the green LED and the 10/100# signal drives the yellow LED. The LINK# and 10/100# signals are designed to connect to LEDs through a 470R series resistor, with the LED connected to VCC_3V3.

Typically, the LINK# LED is on when a link is established and flashes as an activity indicator, and the 10/100# LED is on when the operating speed is 100Mb/s, during auto-negotiation and when the cable is disconnected. Please refer to the Platform Guide for the relevant operating system for the exact details of operation.

Users who intend to design their own Ethernet interface should note that choice of transformer and tracking of the high-speed Ethernet signals are critical for reliable operation. The transformer must be positioned close to the RJ45 socket and must be compatible with the LAN9215. Please refer to the “Suggested Magnetics” application note available on the SMSC website. This application note provides a list of qualified parts and suggested parts.

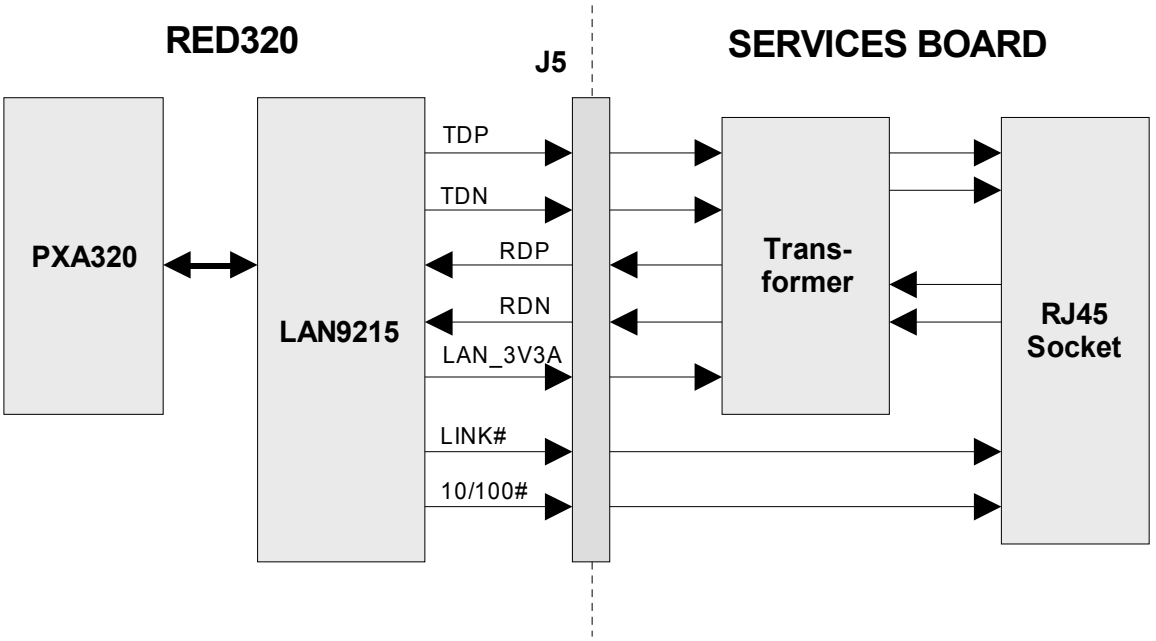

FIGURE 4 - RED320 AND SERVICES BOARD ETHERNET BLOCK DIAGRAM

The Ethernet signals must only be connected as described in the LAN9215 data sheet. Damage may occur if any of the signals is taken outside the range -0.3V to +5.5V.

EMC filtering and ESD protection is not provided on these signals on the RED320. It is the user’s responsibility to ensure that systems using the RED320 and a compatible services board are compliant with the appropriate EMC and ESD standards.

The REDCONN provides EMC filtering and ESD protection on all these signals.

2.8 USB HOST PORTS

The RED320 provides two USB host ports which are compliant with the USB1.1 specification. These are suitable for connecting to a wide range of USB peripherals, and will transfer data at up to 12Mb/s.

Table 10 lists the signals associated with each USB host port.

SIGNAL	J5 PIN	DESCRIPTION
USB1H1PB	46	Port 1 USB positive signal
USB1H1NB	47	Port 1 USB negative signal
USB1H1_PWR	107	Port 1 switched 500mA current limited +5V supply
USB1H2PB	104	Port 2 USB positive signal
USB1H2NB	105	Port 2 USB negative signal
USB1H2_PWR	106	Port 2 switched 500mA current limited +5V supply

TABLE 6 - RED320 USB HOST SIGNALS

Figure 5 shows the RED320 USB host block diagram and a typical services board block diagram.

Both host controllers are implemented in the PXA320 processor. The USB1H1 signals connect directly to a differential port at the processor. The USB1H2 signals are provided by the ISP1105W USB transceiver, which interfaces with the host controller in the processor via a single ended interface. The ISP1105 transceiver converts the single-ended interface from the processor into a standard USB differential pair. Both ports can connect directly to USB ICs or to standard USB connectors on the services board.

The USB host ports are compliant with the USB 1.1 specification. Please refer to the USB 1.1 specification for the electrical characteristics. Do not connect the signals to anything other than USB peripherals. Damage may occur is voltages exceed those given in Table 7.

USB1H1_PWR and USB1H2_PWR are 5V power supplies controlled by independent power distribution switches. Each switch is controlled by the operating system and has a nominal current limit threshold of 500mA. Due to tolerances in the switch, the current limit threshold can vary from 353mA to 640mA over the full temperature range.

EMC filtering and ESD protection is not provided on these signals on the RED320. It is the user's responsibility to ensure that systems using the RED320 and a compatible services board are compliant with the appropriate EMC and ESD standards.

The REDCONN provides EMC filtering and ESD protection on all these signals.

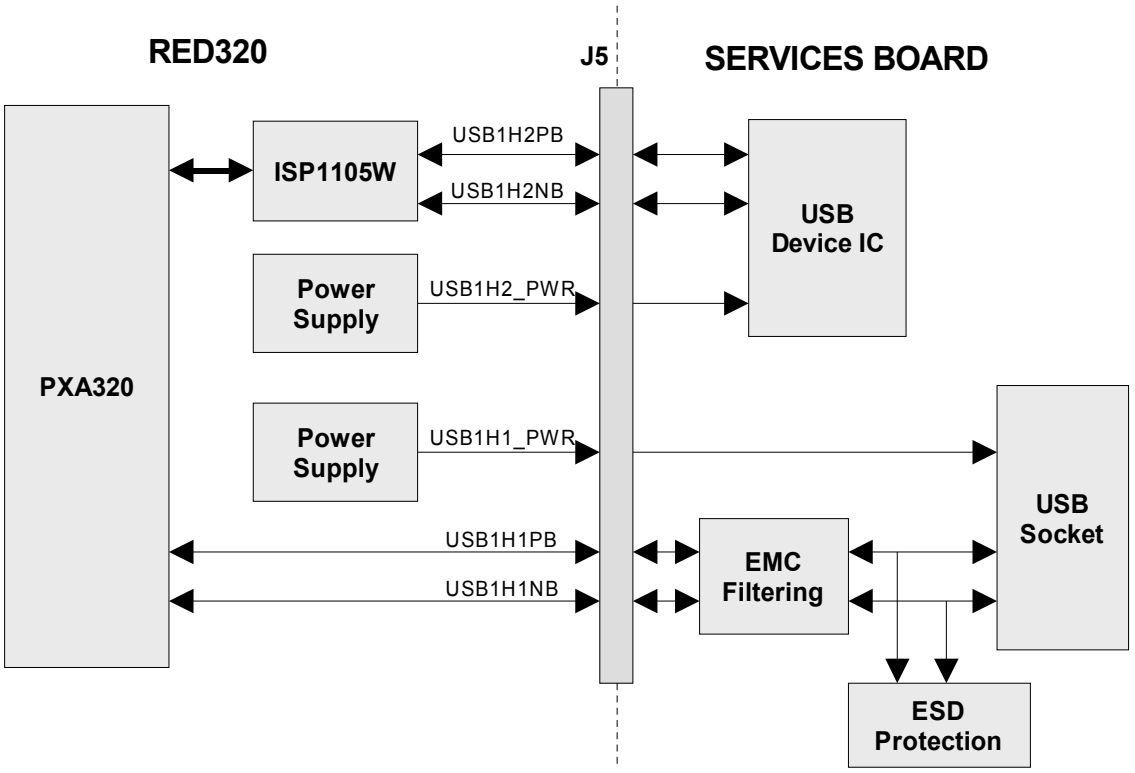

FIGURE 5 - RED320 AND SERVICES BOARD USB HOST BLOCK DIAGRAM

SIGNAL	ABSOLUTE MAX RATING (1)	
	MIN(2)	MAX
USB1H1NB	-0.3V	+4.0V(2)
USB1H1PB	-0.3V	+4.0V(2)
USB1H1_PWR	-0.3V	+6.0V(2)
USB1H2NB	-0.5V	+0.5(3)
USB1H2PB	-0.5V	+0.5(3)
USB1H2_PWR	-0.3V	+6.0V(2)

NOTES:

1) Exceeding the absolute max rating may damage the device.
2) These voltages are with respect to GND.
3) These voltages are with respect to VCC_3V3.

TABLE 7 - RED320 USB HOST PORT ABSOLUTE MAXIMUM RATINGS

2.9 USB DEVICE PORT

The RED320 can also operate as a USB device – that is, it can appear as a peripheral when plugged into a computer with a USB host controller. The USB device port is compliant with the USB 1.1 specification.

Table 8 lists the signals associated with the USB device port.

SIGNAL	J5 PIN	DESCRIPTION
USB1CPB	43	USB device positive signal
USB1CNB	44	USB device negative signal
VBUS	45	+5V input from USB host

TABLE 8 - USB DEVICE SIGNALS

The USB device indicates to a USB host that it is a Full Speed device, capable of operating at 12Mb/s, by means of a 1k5 pull-up resistor on the D+ (USB1CPB) signal. Note that this pull-up resistor is software controlled. If software disables this resistor then the USB device is not detected by a USB host.

The VBUS signal is connected to the +5V power supply of a USB host. The detector on the RED320 allows software to detect when the RED320 is connected to a USB host. The RED320 does not draw power from the VBUS signal.

Figure 6 shows the RED320 USB device port block diagram and a typical services board block diagram. The USB device controller is implemented in the PXA320 processor and interfaces to expansion connector J5. The USB device can connect to a standard USB connector on the services board.

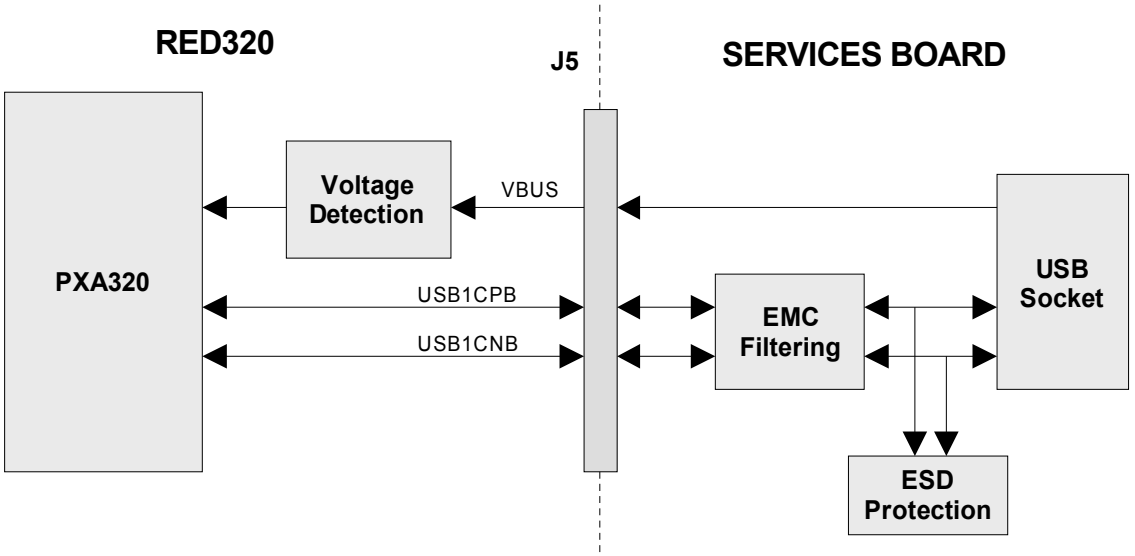

FIGURE 6 - RED320 AND SERVICES BOARD USB DEVICE BLOCK DIAGRAM

The USB device port is compliant with the USB 1.1 specification. Please refer to the USB 1.1 specification for the electrical characteristics. Do not connect the signals to anything other than a USB host port. Damage may occur is voltages exceed those given in Table 9.

EMC filtering and ESD protection is not provided on these signals on the RED320. It is the user's responsibility to ensure that systems using the RED320 and a compatible services board are compliant with the appropriate EMC and ESD standards.

The REDCONN provides EMC filtering and ESD protection on all these signals.

SIGNAL	ABSOLUTE MAX RATING (1)	
	MIN(2)	MAX(2)
VBUS	-0.5V	+7.0V
USB1CNB	-0.3V	+4.0V
USB1CPB	-0.3V	+4.0V

NOTES:

1) Exceeding the absolute max rating may damage the device.
2) All voltages are with respect to GND.

TABLE 9 - RED320 USB DEVICE ABSOLUTE MAXIMUM RATINGS

2.10 AUDIO

The RED320 provides an audio sub-system comprising a mono speaker output, mono microphone input and stereo line output. The audio sub-system is implemented in the WM9713 codec which interfaces to the PXA320 processor via the AC97 bus. An amplifier drives a small loudspeaker from the codec's headphone left output.

Table 10 lists the signals associated with the audio sub-system.

SIGNAL	CONNECTOR - PIN	DESCRIPTION
LINEOUTR	J1-39, J5-56	Right line output
LINEOUTL	J1-40, J5-116	Left line output
SPKR1	J1-41, J5-58	Mono speaker output
SPKR2	J1-42, J5-118	Mono speaker output
MIC	J1-44, J5-120	Microphone input
AGND	J1-37, J1-38, J1-43, J5-57, J5-59, J5-60, J9-115, J9-117, J9119	Analog GND, for referencing MIC and LINEOUT signals.

TABLE 10 - RED320 AUDIO SIGNALS

Figure 7 shows the RED320 audio block diagram and a typical services board block diagram.

The audio signals can connect to standard audio connectors on the services board.

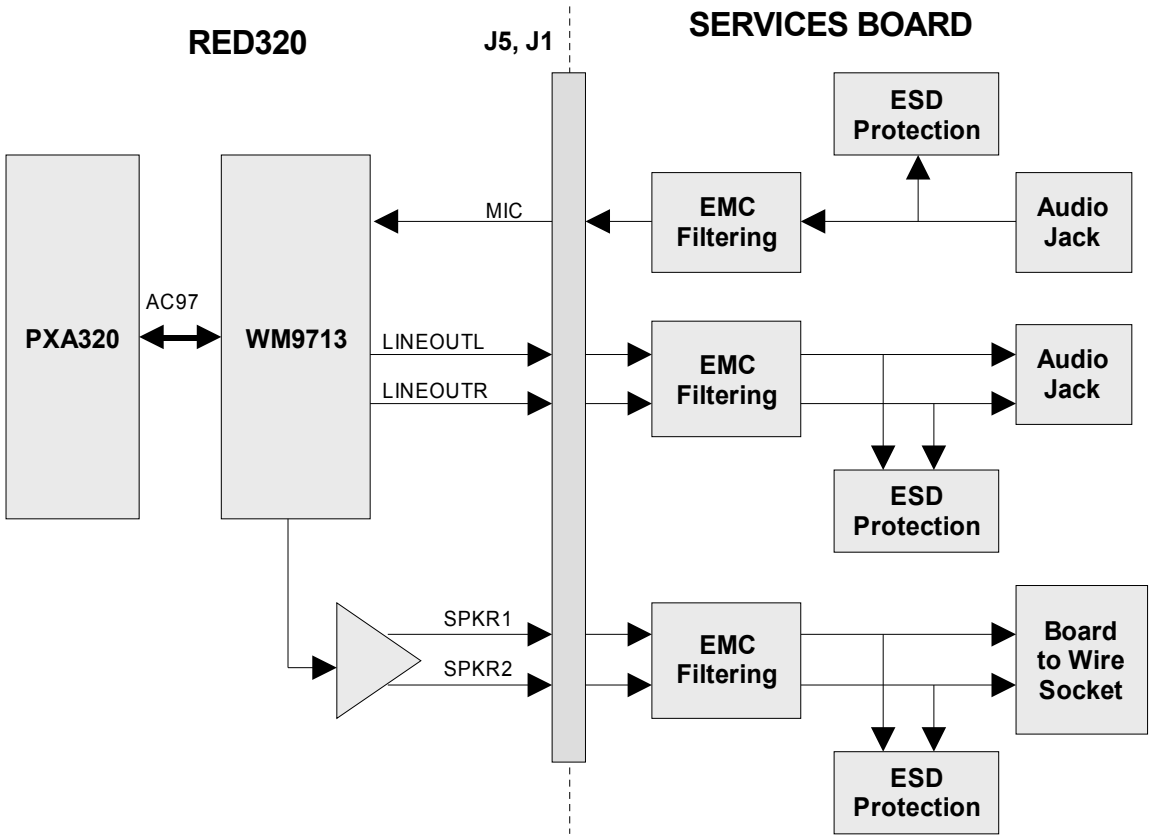

FIGURE 7 - RED320 AND SERVICES BOARD AUDIO BLOCK DIAGRAM

MIC is an input to the WM9713 audio codec. The WM9713 supports both self-powered and unpowered active microphones. Both types of microphone connect between MIC and AGND. Unpowered active microphones require a bias voltage on MIC, which is provided by the RED320 when LK1 is fitted. Self-powered active microphones containing an internal battery do not require a bias voltage. To prevent damage, ensure that LK1 is not fitted when using a self-powered microphone. By default LK1 is fitted.

LINEOUTL and LINEOUTR are outputs of the WM9713 audio codec. These are line level outputs intended to drive high impedance loads. DC blocking capacitors are provided on the RED320.

SPKR1 and SPKR2 are outputs of an LM4871 power amplifier capable of driving a 4Ω or 8Ω mono speaker. The amplifier will drive up to 2.5W into a 4Ω speaker or 1.5W into an 8Ω speaker. Figure 8 shows the required configuration. Note that the speaker must be driven in this differential fashion and must not be connected to GND.

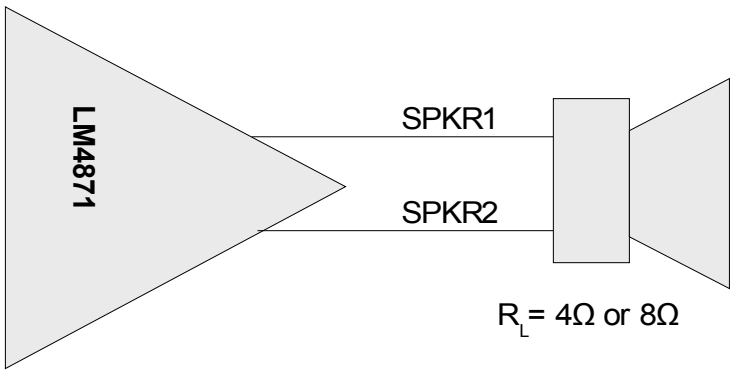

FIGURE 8 - MONO SPEAKER CONNECTION

The WM9713 codec also includes a 4-wire touch-screen controller. This is described in section 2.5.

Table 11 provides the electrical characteristics for the audio signals. The microphone and lineout signals are capacitively coupled.

EMC filtering and ESD protection are not provided on these signals on the RED320. It is the user's responsibility to ensure that systems using the RED320 and a compatible services board are compliant with the appropriate EMC and ESD standards.

The REDCONN provides EMC filtering and ESD protection on all these signals.

SIGNAL	PARAMETER	CONDITION	LIMITS (2)			UNITS
			Min	Typ	Max	
SPKR1, SPKR2	Output power	THD=1%, f=1kHz R_L = 4Ω R_L = 8Ω		 2 (1) 1.2 (1)		 W W
MIC	Full scale input voltage			1		Vrms
LINEOUTL, LINEOUTR	Full scale output voltage	R_L = 10kΩ		1		Vrms

NOTES:

1) The maximum output power must be de-rated to 1W at T_A = 85°C. The power amplifier includes thermal shut down protection.
2) The limits apply to T_A = 25°C.

TABLE 11 - RED320 AUDIO ELECTRICAL CHARACTERISTICS

2.11 REAL TIME CLOCK

The RED320 provides two real time clocks: one inside the PXA320 and another in a Dallas Semiconductor DS1338U connected to the I²C bus. Both RTCs have an accuracy better than 2 seconds a day.

The PXA320 maintains time and date during normal operation and sleep, but is not battery backed and will therefore loose its contents when +5V is removed from the PXA370.

The DS1338U RTC can be connected to an external 3V lithium battery using signal VBACK_BAT to maintain time and date under all power conditions. The RTC will operate with battery voltages in the range 1.3V to 3.7V. If a battery is not used then VBACK_BAT must be grounded. Damage may occur if the VBACK_BAT voltage is outside the range -0.3V to +6V.

The Dallas DS1338U has an I²C slave address of 0D0h. As well as the real-time clock function, it includes 56 bytes on non-volatile RAM.

The operation of the RTCs is operating system dependant. Please refer to the Platform Guide for the relevant operating system for further details.

Table 12 identifies the connectors where the VBACK_BAT can be accessed. This signal is intended to remain within an enclosure and not accessible by the end user. EMC filtering and ESD protection is therefore not provided on the RED320 or the REDCONN.

SIGNAL	CONNECTOR - PIN	DESCRIPTION
VBACK_BAT	J1-20, J5-66, J5-67	Battery backup

TABLE 12 - RED320 RTC BATTERY INPUT

2.12 TEMPERATURE SENSOR

The RED320 has provision for a temperature sensor connected to the I²C bus, but this is not fitted as standard. Contact DSP Design if you have a volume requirement for a temperature sensor. The temperature sensor chip is a Maxim MAX7504 which has an I²C slave address of 90h.

The temperature sensor provides ±2°C accuracy over the -20°C to +100°C temperature range and a resolution of 0.5°C.

2.13 WATCHDOG TIMER

The RED320 provides a watchdog timer implemented in hardware. The watchdog timer has a timeout period of 1.4s and can generate either warm or cold resets. The watchdog timer is disabled following power up or a cold reset and must be enabled by software. Please refer to the Platform Guide for the relevant operating system for further details.

2.14 GENERAL PURPOSE I/O

Twenty nine general purpose I/O signals are available on a number of different expansion connectors. Of these, 25 are connected to GPIO pins on the PXA320. These pins can be programmed to be inputs or outputs and at reset they are all inputs. There are two further input-only pins and two further output-only pins, that route to the PXA320 through a CPLD device.

With the exception of the two dedicated output-only signals, all signals have pull-up or pull-down resistors. In most cases these are the combination of a resistor internal to the PXA320 in parallel with a resistor external to the PXA320. The effective value of the resistance is the parallel combination of these. The internal resistor can be configured in software to be a pull-up, a pull-down or turned off. At reset either an internal pull-up or a pull-down is enabled, and the internal resistor pulls the same way as the external resistor. The effective value of the internal resistor is highly variable – it is nominally 45 kΩ but it may vary between 20 kΩ and 100 kΩ.

Note that the internal pull-up resistors may be changed from their reset state by software. Please refer to the Platform Guide for the relevant operating system for further details.

At reset GPOUT1 will be low and GPOUT0 will be high.

The GPIN1 input routes through the CPLD to the PXA320 EXT_WAKEUP0 input as well as to the GPIO50 pin. When the processor is placed into sleep mode it is possible for a transition on GPIN1 to wake the processor. Please refer to the Platform Guide for the relevant operating system for further details.

Table 13 lists the signals associated with the GPIO interface.

SIGNAL	PXA320 PIN	CONNECTOR - PIN	INTERNAL PU/PD	EXTERNAL PU/PD
UIO0	GPIO113	J4-1, J8-34	PD 45 kΩ	PD 100 kΩ
UIO1	GPIO121	J4-3, J8-46	PD 45 kΩ	PD 100 kΩ
UIO2	GPIO116	J4-5, J8-35	PD 45 kΩ	PD 10 kΩ
UIO3	GPIO118	J4-7, J8-36	PD 45 kΩ	PD 10 kΩ
UIO4	GPIO120	J4-9, J8-37	PD 45 kΩ	PD 10 kΩ
UIO5	GPIO84	J4-11, J8-88	PD 45 kΩ	PD 100 kΩ
UIO6	GPIO95	J4-13, J8-91	PD 45 kΩ	PD 100 kΩ
UIO7	GPIO93	J4-15, J8-87	PD 45 kΩ	PD 100 kΩ
UIO8	GPIO114	J4-2, J8-33	PD 45 kΩ	PD 100 kΩ
UIO9	GPIO115	J4-4, J8-47	PD 45 kΩ	PD 10 kΩ
UIO10	GPIO117	J4-6, J8-98	PD 45 kΩ	PD 10 kΩ
UIO11	GPIO119	J4-8, J8-48	PD 45 kΩ	PD 10 kΩ
UIO12	GPIO83	J4-10, J8-89	PD 45 kΩ	PD 100 kΩ
UIO13	GPIO94	J4-12, J8-90	PD 45 kΩ	PD 100 kΩ
UIO14	GPIO12	J4-14, J8-92	PD 45 kΩ	PD 100 kΩ
UIO15	GPIO89	J4-21, J8-38	PU 45 kΩ	-
UIO16	GPIO92	J4-23, J8-39	PD 45 kΩ	PD 100 kΩ
UIO17	GPIO91	J4-25, J8-40	PD 45 kΩ	-
UIO18	GPIO90	J4-27, J8-41	PU 45 kΩ	-
UIO19	GPIO88	J1-21, J5-41	PU 45 kΩ	–
UIO20	GPIO0_2	J1-24, J5-101	PU 45 kΩ	PU 4.7 kΩ
UIO21	GPIO5	J1-28, J5-72	PU 45 kΩ	PU 10 kΩ
UIO22	GPIO6	J1-30, J5-73	PU 45 kΩ	PU 10 kΩ
UIO23	GPIO7	J1-32, J5-74	PU 45 kΩ	PU 10 kΩ
UIO24	GPIO8	J1-34, J5-75	PU 45 kΩ	PU 10 kΩ
GPIN0	GPIO49	J4-30, J8-94	n/a	PD 100 kΩ
GPIN1	GPIO50	J4-32, J8-95	n/a	PU 100 kΩ
GPOUT0	GPIO45	J4-34, J8-96	n/a	none
GPOUT1	GPIO52	J4-36, J8-97	n/a	none

TABLE 13 - RED320 GPIO SIGNALS

Table 14 provides the electrical characteristics for the GPIO signals. The drive strength of the UIO output pins can be set by software. Please refer to the Platform Guide for the relevant operating system for further details.

Damage may occur if the GPIO pins are connected to voltages outside the range -0.5V to +4V.

EMC filtering and ESD protection is not provided on these signals on the RED320. It is the user's responsibility to ensure that systems using the RED320 and a compatible services board are compliant with the appropriate EMC and ESD standards.

SIGNAL	PARAM-ETER	CONDITION	LIMITS			UNITS
			Min	Typ	Max	
UIO[24:0] GPOUT[1:0]	V_{OH}	I_{OH} = -1mA	0.9 * VCC_3V3	-	-	V
	V_{OL}	I_{OL} = 1mA	-	-	0.1 * VCC_3V3	V
	V_{IH}	-	0.8 * VCC_3V3	-	VCC_3V3 + 0.3	V
	V_{IL}	-	-0.3	-	0.2 * VCC_3V3	V
GPIN[1:0]	V_{IH}	-	2.0	-	3.9	V
	V_{IL}	-	-0.3	-	0.8	V
GPOUT[1:0]	V_{OH}	I_{OH} = -8mA	VCC_3V3-0.4V	-	-	V
	V_{OL}	I_{OL} = 8mA	-	-	0.4	V

TABLE 14 - RED320 GPIO ELECTRICAL CHARACTERISTICS

2.15 I²C EXPANSION

The RED320 provides a two pin serial Inter-Integrated Circuit (I²C) expansion bus. The I²C bus interfaces to a large range of simple data acquisition/control devices available from a number of manufacturers.

Table 15 lists the signals associated with the I²C bus.

SIGNAL	CONNECTOR - PIN	DESCRIPTION
SCL	J4-22, J8-83	I²C clock
SDA	J4-24, J8-84	I²C data

TABLE 15 - RED320 I²C SIGNALS

The I²C bus controller is implemented in the PXA320 processor and is compliant with the I²C Bus Specification Version 2.0, supporting both standard-speed and fast-mode operation. There are 1.2 kΩ pull-up resistors fitted on the SDA and SCK signals.

Damage may occur if the I^2C pins are connected to voltages outside the range -0.3V to +4V.

Table 16 provides the electrical characteristics for the I^2C signals. These are compliant with the I^2C version 2.1 specification.

These signals are intended to remain within an enclosure and not accessible by the end user. EMC filtering and ESD protection is therefore not provided on the RED320.

SIGNAL	PARAM-ETER	CONDITION	LIMITS			UNITS
			Min	Typ	Max	
SDA, SCL	Vo_L	I_{OL} = 3mA	-	-	0.1 * VCC_3V3	V
SDA	V_{IH}	-	0.8 * VCC_3V3	-	VCC_3V3 + 0.3	V
	V_{IL}	-	-0.3	-	0.2 * VCC_3V3	V

TABLE 16 - I^2C ELECTRICAL CHARACTERISTICS

2.16 16-BIT EXPANSION BUS

The RED320 provides a 16-bit expansion bus. This can be used to interface to a wide range of 8 and 16-bit memory and I/O chips. Contact DSP Design to discuss how we can support you using this bus.

Table 17 lists the signals associated with the 16-bit expansion bus.

SIGNAL	J8 PIN	DESCRIPTION	SIGNAL	J8 PIN	DESCRIPTION
BA0	1	Address bus	BD0	51	Data bus
BA1	2		BD1	52	
BA2	3		BD2	53	
BA3	4		BD3	54	
BA4	5		BD4	55	
BA5	6		BD5	56	
BA6	7		BD6	57	
BA7	8		BD7	58	
BA8	9		BD8	59	
BA9	10		BD9	60	
BA10	11		BD10	61	
BA11	12		BD11	62	
BA12	13		BD12	63	
BA13	14		BD13	64	
BA14	15		BD14	65	
BA15	16		BD15	66	
BA16	17		BBE0#	67	Byte enable 0
BA17	18		BBE1#	68	Byte enable 1
BA18	19		BRD#	70	Buffered read output
BA19	20		BWR#	71	Buffered write output
BA20	21		EXPCS1#	72	Chip select output for expansion channel 1
BA21	22				
BA22	23		EXPCS2#	28	Chip select output for expansion channel 2
BA23	24		BRDY	25	Buffered ready input
			EXPINT1#	73	Interrupt input for expansion channel 1
EXPRST1#	26	Reset output for expansion channel 1	EXPINT2#	74	Interrupt input for expansion channel 2
EXPRST2#	27	Reset output for expansion channel 2	EXPDREQ	75	DMA request input

TABLE 17 - RED320 EXPANSION BUS SIGNALS

Table 18 provides the electrical characteristics for the 16-bit expansion bus signals. The RED320 may be damaged if voltages outside the range -0.3V – 4V are applied to any of these signals.

These signals are intended to remain within an enclosure and not accessible by the end user. EMC filtering and ESD protection is therefore not provided on the RED320.

SIGNAL	PARAM-ETER	CONDITION	LIMITS			UNITS
			Min	Typ	Max	
EXPINT1# EXPINT2#	V_{IH}	-	0.8 * VCC_3V3	-	VCC_3V3 + 0.3	V
	V_{IL}	-	-0.3	-	0.2 * VCC_3V3	V
BD[15:0] EXPDREQ BRDY	V_{IH}	-	2	-	3.9	V
	V_{IL}	-	-0.3	-	0.8	V
BA[23:0] BD[15:0] EXPRST1# EXPRST2# EXPCS1# EXPCS2# BBE0# BBE1# BRD# BWR#	V_{OH}	I_{OH} = -8mA	VCC_3V3 - 0.4	-	-	V
		I_{OH} = -0.1mA	VCC_3V3 - 0.2	-	-	V
	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
		I_{OL} = 0.1mA	-	-	0.2	V

TABLE 18 - RED320 16-BIT EXPANSION BUS ELECTRICAL CHARACTERISTICS

3 POWER SUPPLIES, POWER MANAGEMENT AND RESET

3.1 POWER INPUT

The RED320 operates from a single +5V input and generates all other supplies internally. Power can be applied to the RED320 by any of J1, J4, J5 and J8. To minimise voltage drop between the power supply and the RED320, power should be applied through short, low-resistance wires or PCB traces. If power is applied through the ribbon cable connectors J1 or J4 then all VCC_5V and GND pins should be connected to the power supply.

In the case of the inter-board connectors J5 and J8 all VCC_5V and GND pins of both connectors should be connected to the PCB power traces, which are preferably implemented as power planes on a multi-layer PCB.

The voltage supplied to the RED320 should be 5V +/-5%. The RED320 may be damaged in the voltage on the VCC_5V line is outside the range -0.3V to +6V.

Table 19 lists all the connector pins that can be used to supply power to the RED320.

SIGNAL	CONNECTOR - PIN
VCC_5V	J1-11, J1-12, J1-13, J1-14, J1-15, J1-17, J4-29, J4-31, J4-33, J4-35, J4-37, J5-6, J5-7, J5-8, J5-9, J5-76, J5-77, J5-78, J5-79, J5-80, J5-81, J5-82, J5-83, J5-84, J5-85, J8-29, J8-30, J8-42, J8-43, J8-44, J8-45, J8-49, J8-50
GND	J1-9, J1-10, J1-19, J1-25, J1-27, J1-29, J1-31, J1-33, J4-16, J4-18, J4-19, J4-20, J4-39, J4-43, J5-5, J5-10 through J5-25, J5-28, J5-31 through J5-40, J5-42, J5-48 through J5-54, J5-65, J8-79, J8-80, J8-81, J8-82, J8-93, J8-99, J8-100

TABLE 19 - RED320 POWER INPUT

3.2 POWER CONSUMPTION

The RED320 power consumption depends on what it is doing, as power management software can reduce power consumption when the processor is not required. Thus when executing an operating system such as Windows CE, the operating system will reduce clock speed or execute halt instructions when there is reduced user or application activity. On the other hand, power consumption will increase if processor-intensive operations, such as playing videos, are being performed. The RED320 can also enter a sleep state, where peripherals are powered down and the processor clock turned off.

In practical applications that use LCD panels, system power consumption will be influenced by the power taken by the display, in particular by the display's backlight.

Table 20 provides some typical figures for power consumption for the RED320.

CONFIGURATION	TYPICAL POWER CONSUMPTION	
	mA @ 5V	W
Standalone RED320 with no peripherals connected – operating system running	260	1.3
Standalone RED320 with no peripherals connected – suspended	2.7	0.014
RED320 and REDCDC connected to a VGA display and CFL backlight.	1500	7.5

TABLE 20 - RED320 CURRENT CONSUMPTION

3.3 POWER OUTPUT

The RED320 generates +3.3V on-board, and is able to supply up to 500mA from this 3.3V rail to external peripherals such as LCDs. Users must ensure that this current is not exceeded. Note that this limit applies to the peak current, and not the average current.

VCC_3V3 is output from RED320 on either J1, J4, J5, J8.

To minimise voltage drop between the RED320 and the peripheral, power should be applied through short, low-resistance wires or PCB traces. If power is applied through the ribbon cable connectors J1 or J4 then all VCC_3V3 and GND pins should be connected to the peripheral.

In the case of the inter-board connectors J5 and J8 all VCC_3V3 and GND pins of both connectors should be connected to the PCB power traces, which are preferably implemented as power planes on a multi-layer PCB.

Table 21 lists all the connector pins that can be used to supply external peripherals. Table 19 lists the GND pins.

SIGNAL	PIN
VCC_3V3	J1-16, J1-18, J4-17, J5-68, J5-69, J5-70 J8-31, J8-32

TABLE 21 - RED320 POWER OUTPUT

3.4 RESET INPUT AND OUTPUT

The RED320 can be reset by pulling the PB_RST# signal low. In this way a system reset can be generated by an external IC or switch. PB_RST# is an open-drain signal with a 100k pull-up resistor. It must be driven by an open drain driver or a switch to GND. The RED320 many be damaged if the voltage on this pin is outside the range -0.3V to 6.5V.

PB_RST# connects to a power management IC which generates a power-on reset to the processor, which in turn asserts the main board reset to all other peripherals during the power-up sequence and hardware reset events under operating system control.

Table 22 lists the connector pins the PB_RST# signal is available on.

SIGNAL	CONNECTOR - PIN	DESCRIPTION
PB_RST#	J1-23, J5-71, J8-69	Open drain reset input

TABLE 22 - RED320 RESET INPUT

The RST_OUT# output from the processor goes to a CPLD, where it is OR-ed with CPLD reset register outputs to drive the LAN_RST#, NOR_RST#, EXPRST1# and EXPRST2# signals. EXPRST1# and EXPRST2# are available as part of the 16-bit expansion bus and are intended to reset external peripherals on the 16-bit expansion bus. Each of these resets is asserted whenever RST_OUT# is asserted, or by software using registers in the CPLD.

3.5 POWER MANAGEMENT

The RED320 provides a very low power sleep mode and a number of wakeup options. DSP Design can discuss detailed technical support in this area to volume customers who are implementing their own operating system. Please refer to the Platform Guide for power management implementation details for supported operating systems.

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APPENDIX A - MECHANICAL, ENVIRONMENTAL, HANDLING

A.1 DIMENSIONS

- PCB dimensions are 85mm x 65mm.
- PCB thickness is 1.6mm.
- Maximum component height above the PCB is PCB 6.2mm.
- Maximum component height below the PCB is PCB 3.3mm.
- When mounted on a PCB using connectors J5 and J8 there is 4mm between the PCBs (assuming FX8-xxxP-SV1 connectors are used).

A.2 WEIGHT

36g.

A.3 OPERATING TEMPERATURE RANGE

-20°C to +85°C.

A.4 HUMIDITY

10% - 90%, non-condensing.

A.5 ELECTRO-STATIC SENSITIVE DEVICE (ESD)

The RED320 and REDCONN contain CMOS devices which can be damaged by static electricity discharging through the device. Please observe anti-static handling precautions when handling the RED320 and REDCONN or when adding or removing connectors.

For ESD protection to be effective any ESD protection components should be placed close to connectors or interfaces that are accessible by the end user. ESD protection is therefore best implemented on a services board where all the end-user accessible connectors are mounted. For that reason the RED320 lacks ESD protection components on many of its signals. Conversely, the REDCONN does include ESD protection components on most connectors. The nature of any ESD protection is noted elsewhere in this manual.

Although the RED320 and REDCONN utilise ESD protection techniques, it is the user's responsibility to ensure that systems using the RED320, REDCONN and any other sub-assemblies are compliant with the appropriate ESD standards and provide adequate protection for the application.

A.6 ELECTROMAGNETIC COMPATIBILITY (EMC)

Most finished products that use the RED320 will be subject to EMC regulations, such as those required by the EU's EMC Directive. Finished products may require EMC tests, and in order to pass these tests the product may need to be enclosed in a Faraday cage formed by the enclosure, and may need to have EMC filtering on conductors that pass through the enclosure.

User accessible connectors (such as Ethernet and USB) and interfaces (touch-screen) must break through the Faraday cage. For EMC filtering to be effective, any EMC filters must be placed close to these connectors and interfaces. EMC filtering is therefore best implemented on a services board where all the end user accessible connectors are mounted. For that reason the RED320 lacks filter components on many of its signals. Conversely, the REDCONN does include EMC filtering on most connectors. The nature of any EMC filtering is noted elsewhere in this manual.

Although the RED320 and REDCONN utilise EMC filtering techniques, it is the user's responsibility to ensure that systems using the RED320, REDCONN and any other sub-assemblies are compliant with the appropriate EMC standards.

A.7 CHASSIS

The RED320 provides four mounting holes. One is connected to a CHASSIS plane and three are isolated from all signals and planes. The metal parts of connectors J6 and J7 are connected to the CHASSIS plane.

The mounting hole connected to CHASSIS is the mounting holes closest to J6.

No connections are made between the CHASSIS plane and the GND plane on the RED320. EMC performance may be improved by ensuring a low impedance bond between the pad of the CHASSIS mounting hole and the conductive enclosure, and by connecting CHASSIS to GND at a single star point. REDCONN provides a single point connection between CHASSIS and GND using a single ferrite bead.

A.8 RoHS COMPLIANCE

The RED320 and REDCONN are only available as fully RoHS compliant products and do not contain any of the six banned substances above the levels specified in the RoHS Directive 2002/95/EC.

APPENDIX B - RED320 DRAWINGS

This appendix provides component placement diagrams and mechanical drawings for the RED320.

B.1 COMPONENT PLACEMENT

Figures B1 and B2 show the component placement for the top and bottom sides of the RED320 respectively. A high resolution PDF is available on the DSP Design website.

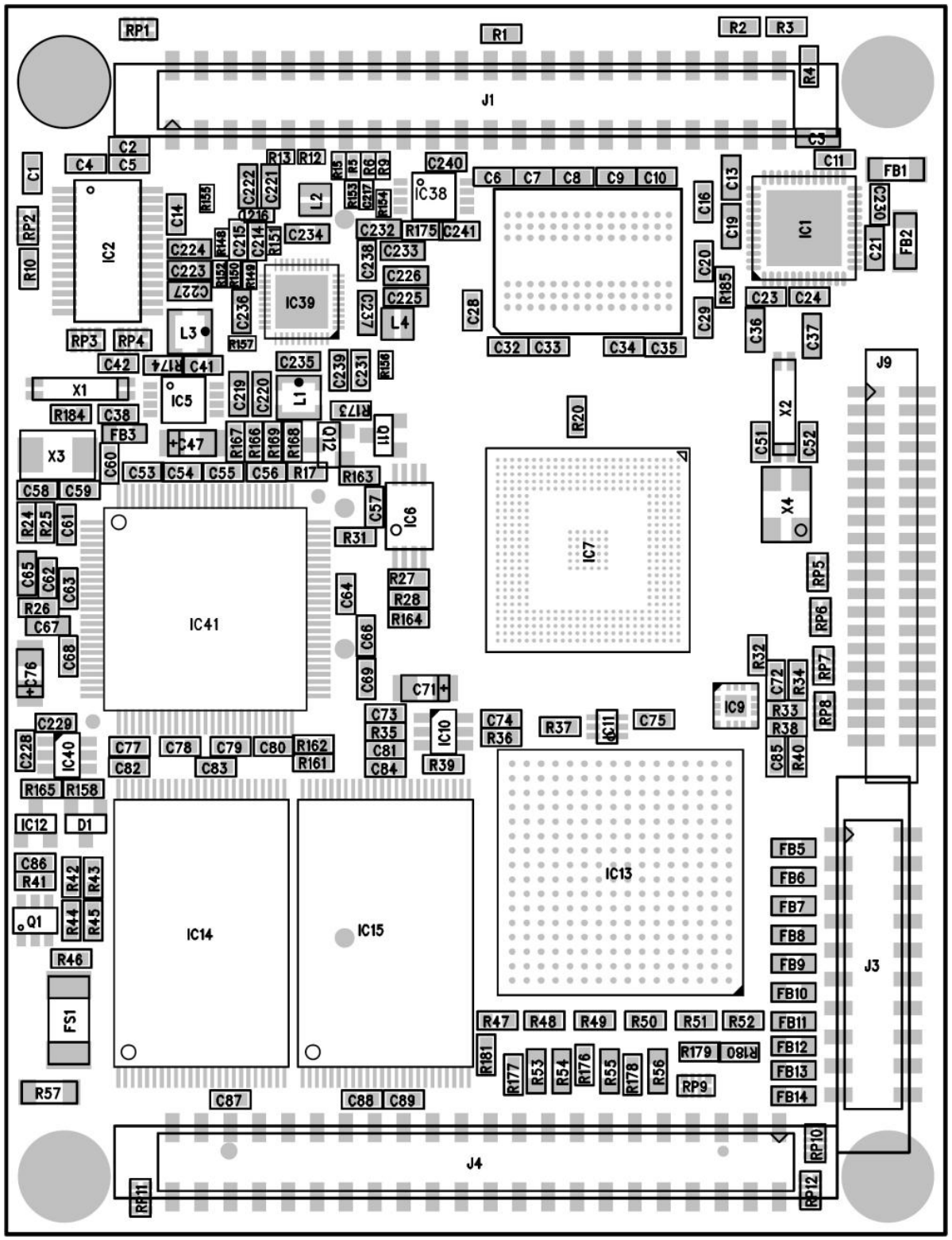

FIGURE B1 - RED320 COMPONENT PLACEMENT DIAGRAM – TOP SIDE

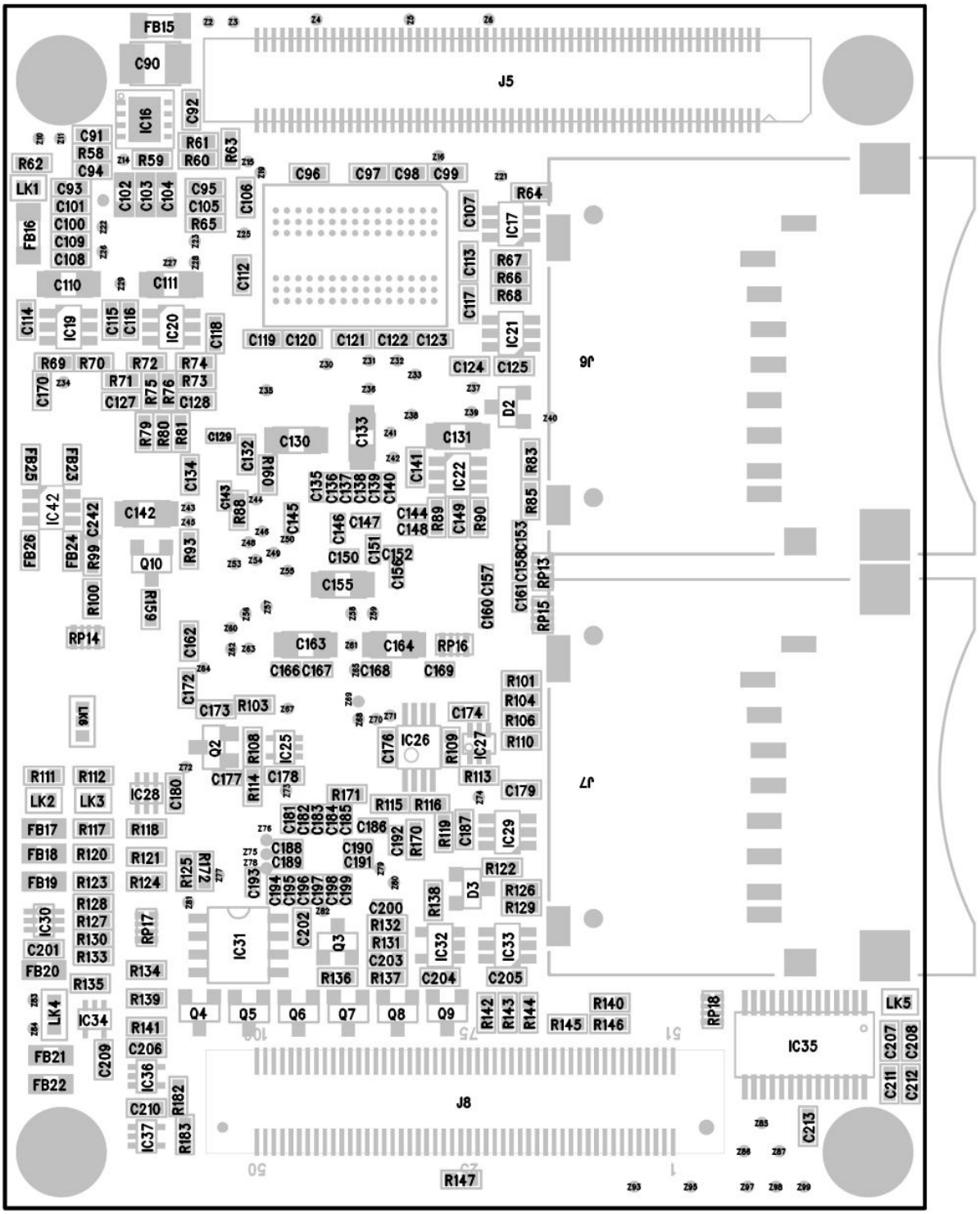

FIGURE B2 - RED320 COMPONENT PLACEMENT DIAGRAM – BOTTOM SIDE

B.2 MECHANICAL DIMENSIONS

Mechanical dimensions are shown in Figure B3. Connector positions are shown in Figures B4 and B5. All dimensions are to pad or hole centres. The four mounting holes are 3.2mm diameter. Board profile tolerance is +/- 0.5mm.

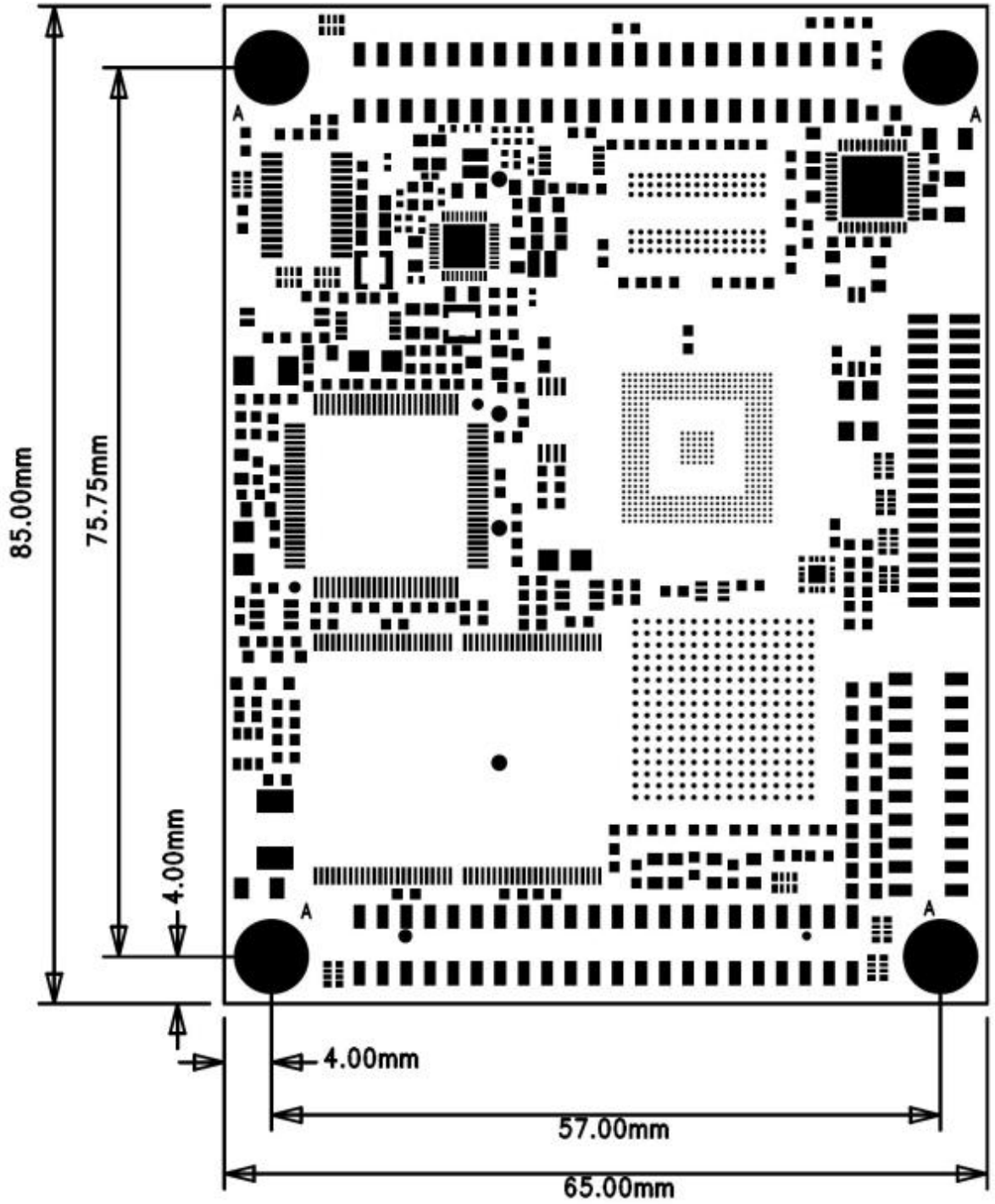

FIGURE B3 - RED320 BOARD PROFILE

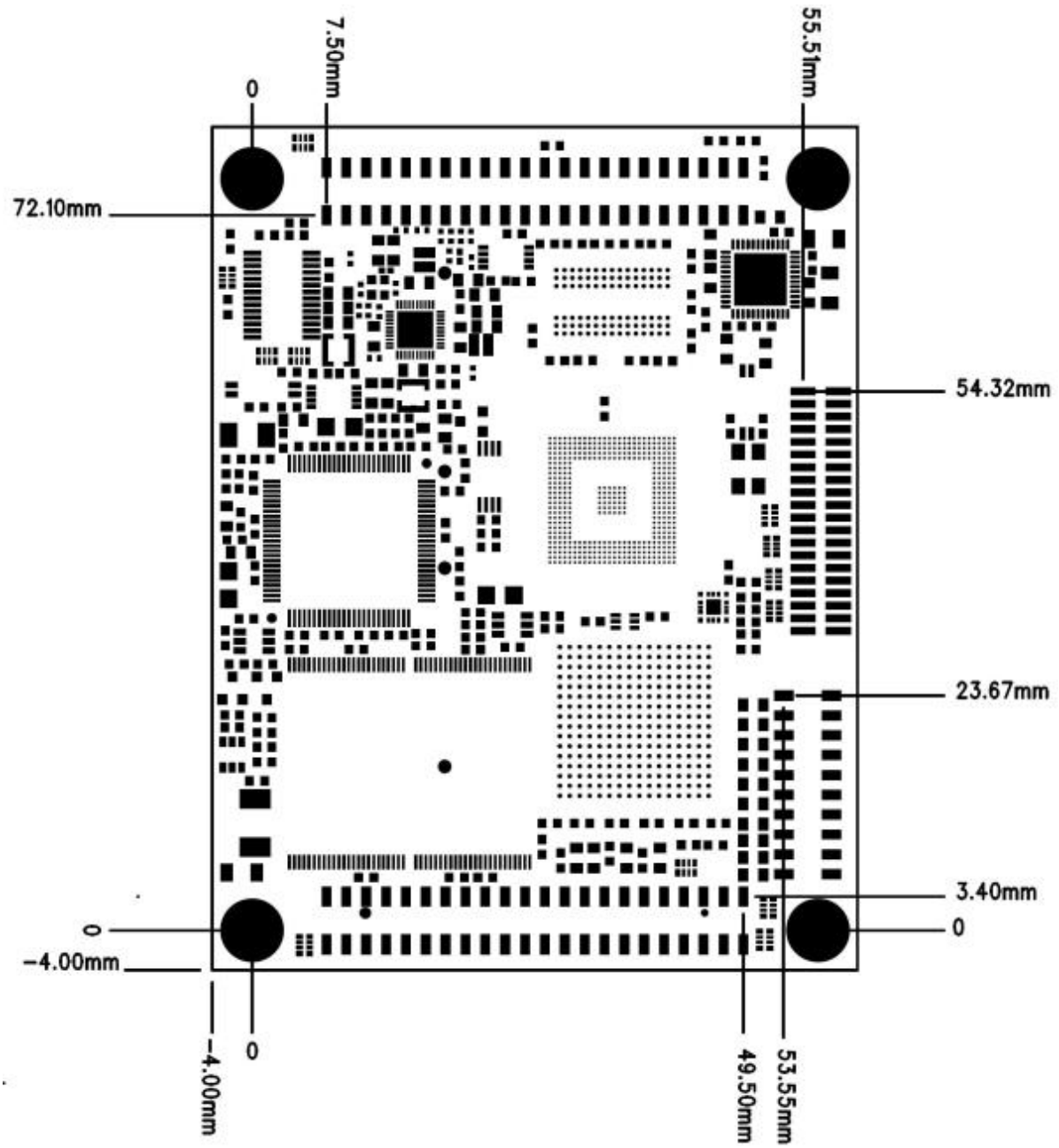

FIGURE B4 - TOP SIDE CONNECTOR POSITIONS

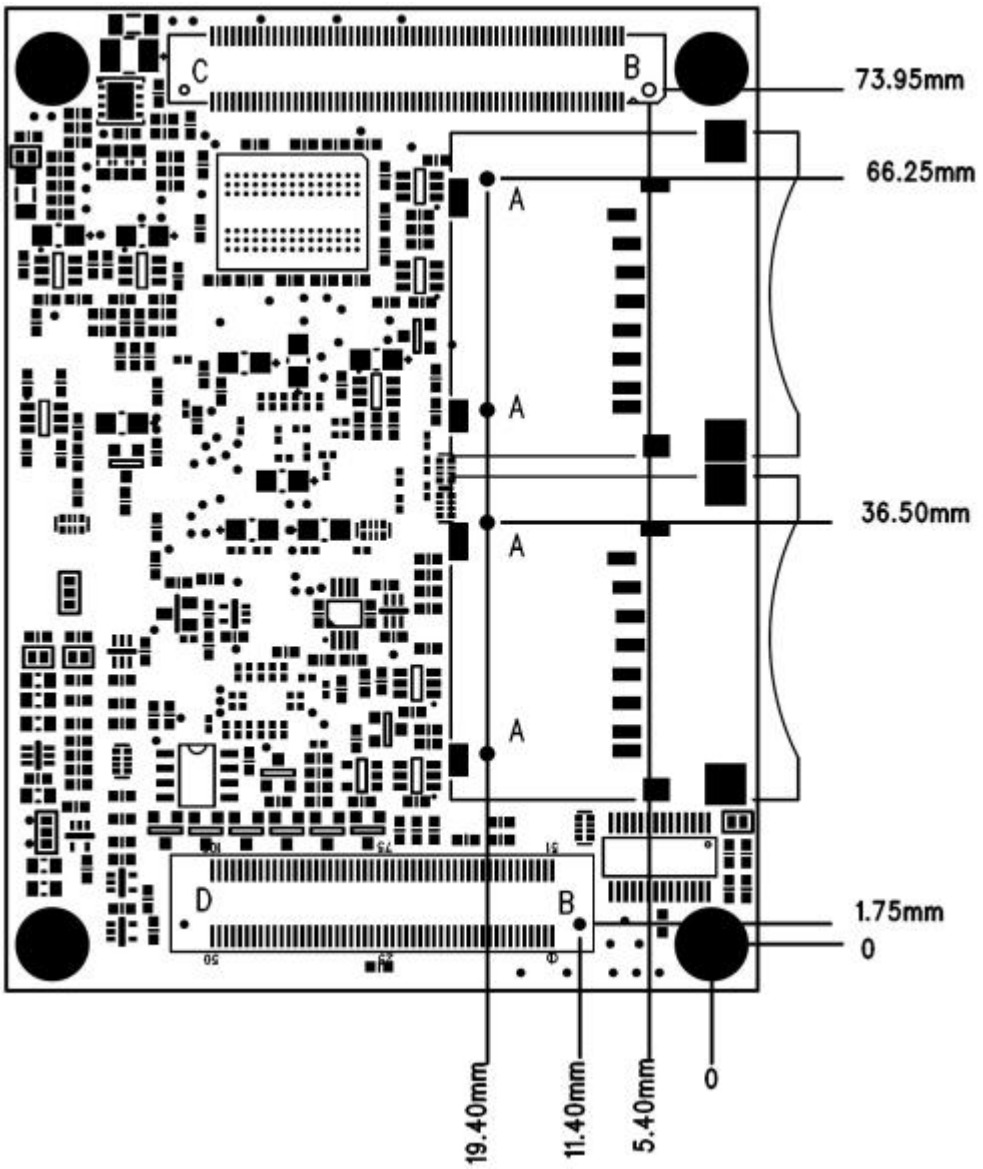

FIGURE B5 - BOTTOM SIDE CONNECTOR POSITIONS

Table B1 lists the holes sizes shown in Figure B5.

HOLE REFERENCE	DIAMETER
A	1.36mm
B	1.1mm
C	0.7mm
D	0.76mm

TABLE B1 - RED320 HOLE SIZES

APPENDIX C - OPTIONS AND ORDERING INFORMATION

This appendix lists the range of products available from DSP Design related to the RED320. Order codes prefixed with “DSP-” indicate the items are RoHS compliant.

C.1 PROCESSOR MODULES

Table C1 contains the order codes for the RED320 processor.

ITEM	DESCRIPTION
DSP-RED320CE	RED320 624MHz processor module with Windows Embedded CE 6.0

TABLE C1 - PROCESSOR MODULES

C.2 LAUNCHPAD APPLICATION DEVELOPMENT KITS

Table C2 contains the order codes for the LaunchPad Application Development Kit for RED320.

ITEM	DESCRIPTION
DSP-LPRED320CE	Windows Embedded CE 6.0 LaunchPad Application Development Kit for the RED320

TABLE C2 - LAUNCHPAD APPLICATION DEVELOPMENT KITS

C.3 DISPLAY ACCESSORIES

Table C3 contains the order codes for the cables and display interface boards for the RED320.

ITEM	DESCRIPTION
DSP-TFTIF-CAB7	40 way cable assembly for DSP-TFTIF31, DSP-TFTIF41 and DSP-TFTIFKYV boards, connectors at both ends, length 7 inches
DSP-TFTIF-CAB11	40 way cable assembly for DSP-TFTIF31, DSP-TFTIF41 and DSP-TFTIFKYV boards, connectors at both ends, length 11 inches
DSP-TFTIF31M	Display interface adapter. Connects 40-way ribbon cable to LCDs which use the 31-pin Hirose DF9 connector.
DSP-TFTIF41	Display interface adapter. Connects 40-way ribbon cable to LCDs which use the 41-pin Hirose DF9 connector.
DSP-TFTIFKYV	Display interface adapter. Connects 40-way ribbon cable to Kyocera LCDs.
TRM-TFTIFKYV	Printed and bound Technical Reference Manual for the TFTFIFKYV.
DSP-TFTKYV75	A Kyocera V-series 640 X 480 7.5” TFT display.
DSP-TFTKYV75-KIT	A display kit, comprising the TFTKYV75, TFTIFKYV, backlight inverter and cables.
DSP-AAVGA	Display interface adapter for VGA CRTs. Connects 40-way ribbon cable to a video D/A converter and 15-pin D-type connector.

TABLE C3 - DISPLAY ACCESSORIES

C.4 OTHER ACCESSORIES

Table C4 contains the order codes for miscellaneous accessories for the RED320.

ITEM	DESCRIPTION
DSP-TCONN-PSU	20W 5V 4A AC-DC PSU for the REDCDC.
DSP-REDCDC	Connector breakout board for the RED320 with DC input power jack.
DSP-REDCPOE	Connector breakout board for the RED320 with PoE capability.
DSP-SD2G	2 Gbyte SD card.

TABLE C4 - OTHER ACCESSORIES

APPENDIX D - TFTIF LCD INTERFACE BOARDS

This appendix describes some options for connecting LCDs to the RED320.

D.1 INTRODUCTION

DSP Design provides four LCD interface boards which are compatible with the RED320:

- TFTIF31
- TFTIF41
- TFTIFKYV
- AAVGA (generates analog RGB signals on a 15-way VGA connector)

The LCD interface boards connect to the 40-way parallel digital interface connector J9 on the RED320. These LCD interface boards allow a wide variety of LCDs and monitors to be interfaced with RED320. Please refer to the Platform Guide for the relevant operating system for a full list of supported LCDs.

Each interface board uses a slightly different set of signals on the RED320 LCD connector J9. Table D1 lists the signals used by each interface board and how they map onto the RED320.

NOTES FOR TABLE D1 (overleaf):

1) The RED320 has a 16-bit colour bus interface in a 5-6-5 format. The R0 and B0 bits are not used and therefore are connected to GND.
2) The RED320 can be configured to supply either VCC_5V or LCD_ADJ to the LCD interface board. Setting LK6 on the RED320 to position 1-2 configures J9 pin 33 to VCC_5V. Setting LK6 to 2-3 configures J9 pin 33 to LCD_ADJ. By default VCC_5V is selected, as this is necessary for compatibility with the TFTIF31 and TFTIF41.
3) The TFTIF31 and TFTIF41 support LCDs with either 3.3V or 5V power requirements. This pin is used to supply 5V to the LCD from the RED320. Configure LK6 on the RED320 to position 1-2 for TFTIF31 and TFTIF41.
4) Configure LK6 on the RED320 to position 2-3 for the TFTIFKYV.

J9 PIN	RED320	TFTIF31/TFT41 (J1)	TFTIFKYV (J4)	AAVGA (J2)
1	BKL_EN	BKL_EN	BKL_EN	NC
2	LCD_EN	LCD_EN	LCD_EN	NC
3	GND	GND	GND	GND
4	LCD_DCLK	LCD_DCLK	LCD_DCLK	LCD_DCLK
5	GND	GND	GND	GND
6	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC
7	GND	GND	GND	GND
8	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC
9	TSXP	NC	TSXP	NC
10	TSXN	NC	TSXN	NC
11	GND (1)	LCD_R0	LCD_R0	GND
12	LCD_R1	LCD_R1	LCD_R1	LCD_R1
13	GND	GND	GND	GND
14	LCD_R2	LCD_R2	LCD_R2	LCD_R2
15	LCD_R3	LCD_R3	LCD_R3	LCD_R3
16	LCD_R4	LCD_R4	LCD_R4	LCD_R4
17	GND	GND	GND	GND
18	LCD_R5	LCD_R5	LCD_R5	LCD_R5
19	NC	NC	NC	NC
20	NC	NC	NC	NC
21	GND	GND	GND	GND
22	LCD_G0	LCD_G0	LCD_G0	LCD_G0
23	LCD_G1	LCD_G1	LCD_G1	LCD_G1
24	LCD_G2	LCD_G2	LCD_G2	LCD_G2
25	VCC_3V3	VCC_3V3	VCC_3V3	VCC_3V3
26	LCD_G3	LCD_G3	LCD_G3	LCD_G3
27	LCD_G4	LCD_G4	LCD_G4	LCD_G4
28	LCD_G5	LCD_G5	LCD_G5	LCD_G5
29	VCC_3V3	VCC_3V3	VCC_3V3	VCC_3V3
30	TSYN	NC	TSYN	NC
31	TSYP	NC	TSYP	NC
32	GND (1)	LCD_B0	LCD_B0	GND
33	VCC_5V / LCD_ADJ (2)	VCC_5V (3)	LCD_ADJ (4)	NC
34	LCD_B1	LCD_B1	LCD_B1	LCD_B1
35	LCD_B2	LCD_B2	LCD_B2	LCD_B2
36	LCD_B3	LCD_B3	LCD_B3	LCD_B3
37	VCC_5V	VCC_5V	NC	NC
38	LCD_B4	LCD_B4	LCD_B4	LCD_B4
39	LCD_B5	LCD_B5	LCD_B5	LCD_B5
40	LCD_DE	LCD_DE	LCD_DE	LCD_DE

TABLE D1 - LCD INTERFACE BOARD SIGNAL COMPARISON

D.2 TFTIF31

The TFTIF31 is designed to interface with a number of TFT LCDs, from Sharp and other manufacturers that use a 31-way Hirose DF9 connector.

The TFTIF31 plugs into J9 on the RED320 using a ribbon cable, the TFTIF-CAB7 or TFTIF-CAB11 available from DSP Design.

This section describes the TFTIF31, listing the display pin assignments and the solder link settings.

D.2.1 31-pin Connector Pin Assignments

Table D2 shows the pin assignments for the TFTIF31 display connector. Note that this connector supports 18-bit LCDs (displays with six bits each of red, green and blue data). The PXA320 generates only 16 bits of RGB data: five bits each of red and blue and six bits of green. Thus the LCD_R0 and LCD_B0 signals in the TFTIF31 connector are connected to GND at the RED320 J9.

PIN	LCD SIGNAL	PIN	LCD SIGNAL
1	GND	2	LCD_DCLK
3	LCD_HSYNC	4	LCD_VSYNC
5	GND	6	LCD_R0
7	LCD_R1	8	LCD_R2
9	LCD_R3	10	LCD_R4
11	LCD_R5	12	GND
13	LCD_G0	14	LCD_G1
15	LCD_G2	16	LCD_G3
17	LCD_G4	18	LCD_G5
19	GND	20	LCD_B0
21	LCD_B1	22	LCD_B2
23	LCD_B3	24	LCD_B4
25	LCD_B5	26	GND
27	LCD_DE	28	LCDVCC
29	LCDVCC	30	LEFT/RIGHT
31	UP/DOWN	-	-

TABLE D2 - TFTIF31 DISPLAY PIN ASSIGNMENTS

D.2.2 Power Supply Selection: LK1

The TFTIF31 accepts VCC_3V3 and VCC_5V from the RED320. One or other of these voltages is selected by solder link LK1 and routed to the LCD. This supply voltage is intended to power the LCD electronics, but not the backlight inverter.

From LK1 the selected voltage is then routed to a transistor switch, which turns on the power to the LCD (LCDVCC) under control of the RED320 LCD_EN signal. LK1 can be set to one of two positions. The position marked "5" is for 5V LCDs. The position marked "3.3" is for 3.3V LCDs. You may need to change the solder link to match your display.

D.2.3 Pin 30 and 31 Configuration: LK2 and LK3

LK2 and LK3 are connected to the 31-way connector pins 30 and 31 respectively. The links can be used to change the display orientation, at least on some Sharp displays. For a normal image both should be left open, or linked in the 2-3 position. For an upside-down image both should be linked in the 1-2 position. Some other LCDs use pins 30 and 31 for other purposes, such as additional power supply pins. LK2 and LK3 should therefore be linked to match the requirement of each display.

Table D3 shows the connections of the LK2 and LK3 pins, thus allowing suitable connections to be made.

LK2 PIN	LK2 CONNECTION	LK3 PIN	LK3 CONNECTION
1	GND	1	GND
2	PIN 30	2	PIN 31
3	LCDVCC	3	LCDVCC

TABLE D3 - TFTIF31 PIN 30 AND PIN 31 CONNECTIONS

LCDVCC is the LCD display voltage selected by LK1, as described in the previous section.

D.2.4 Backlight Enable Signal

The RED320 generates a logic-level signal intended to turn on and off the backlight inverter. This signal is called BKL_EN, and is 0V low for “off” and 3.3V for “on”. The BKL_EN signal can be taken to a backlight inverter from the TFTIF31 connector J3. J3 is a Molex 53261-0390 connector. Pin assignments are given in Table D4. Note that some backlight inverters specify a 5V signal to turn on the backlight, so BKL_EN may not work with all inverters.

J3 PIN	SIGNAL
1	VCC_5V
2	BKL_EN
3	GND

TABLE D4 - TFTIF31 J3 PIN ASSIGNMENTS

D.3 TFTIF41

The TFTIF41 is designed to interface with a small number of TFT LCDs, principally from Sharp, that use a 41-way Hirose DF9 connector.

The TFTIF41 plugs into J9 on the RED320 using a ribbon cable, the TFTIF-CAB7 or TFTIF-CAB11 available from DSP Design.

This section describes the TFTIF41, listing the display pin assignments and the solder link settings.

D.3.1 41-pin Connector Pin Assignments

Table D5 shows the pin assignments for the TFTIF41 display connector. Note that this connector supports 18-bit LCDs (displays with six bits each of red, green and blue data). The PXA320 generates only 16 bits of RGB data: five bits each of red and blue and six bits of green. Thus the LCD_R0 and LCD_B0 signals in the TFTIF41 connector are connected to GND at the RED320 J9.

PIN	LCD SIGNAL	PIN	LCD SIGNAL
1	GND	2	LCD_DCLK
3	GND	4	LCD_HSYNC
5	LCD_VSYNC	6	GND
7	GND	8	GND
9	LCD_R0	10	LCD_R1
11	LCD_R2	12	GND
13	LCD_R3	14	LCD_R4
15	LCD_R5	16	GND
17	GND	18	GND
19	LCD_G0	20	LCD_G1
21	LCD_G2	22	GND
23	LCD_G3	24	LCD_G4
25	LCD_G5	26	GND
27	GND	28	GND
29	LCD_B0	30	LCD_B1
31	LCD_B2	32	GND
33	LCD_B3	34	LCD_B4
35	LCD_B5	36	GND
37	ENABLE	38	LEFT/RIGHT
39	LCDVCC	40	LCDVCC
41	UP/DOWN	-	-

TABLE D5 - TFTIF41 DISPLAY PIN ASSIGNMENTS

D.3.2 Power Supply Selection: LK1

The TFTIF41 accepts VCC_3V3 and VCC_5V from the RED320. One or other of these voltages is selected by solder link LK1 and routed to the LCD. This supply voltage is intended to power the LCD electronics, but not the backlight inverter.

From LK1 the selected voltage is then routed to a transistor switch, which turns on the

power to the LCD (LCDVCC) under control of the RED320 LCD_EN signal. LK1 can be set to one of two positions. The position marked "5" is for 5V LCDs. The position marked "3.3" is for 3.3V LCDs. You may need to change the solder link to match your display.

D.3.3 Pin 41 and 38 Configuration: LK2 and LK3

LK2 and LK3 are connected to the 41-way connector pins 41 and 38 respectively. The links can be used to change the display orientation, at least on some Sharp displays. For a normal image both should be left open, or linked in the 2-3 position.

For an upside-down image both should be linked in the 1-2 position. Some other LCDs may use pins 41 and 38 for other purposes, such as additional power supply pins. LK2 and LK3 should therefore be linked to match the requirement of each display. Table D6 lists the connections of the LK2 and LK3 pins, thus allowing suitable connections to be made.

LK2 PIN	LK2 CONNECTION	LK3 PIN	LK3 CONNECTION
1	GND	1	GND
2	PIN 41	2	PIN 38
3	LCDVCC	3	LCDVCC

TABLE D6 - TFTIF41 PIN 41 AND PIN 38 CONNECTIONS

LCDVCC is the LCD display voltage selected by LK1, as described in the previous section.

D.3.4 Backlight Enable Signal

The RED320 generates a logic-level signal intended to turn on and off the backlight inverter. This signal is called BKL_EN, and is 0V low for “off” and 3.3V for “on”. The BKL_EN signal can be taken to a backlight inverter from the TFTIF41 connector J3. J3 is a Molex 53261-0390 connector. Pin assignments are given in Table D7. Note that some backlight inverters specify a 5V signal to turn on the backlight, so BKL_EN may not work with all inverters.

J3 PIN	SIGNAL
1	VCC_5V
2	BKL_EN
3	GND

TABLE D7 - TFTIF41 J3 PIN ASSIGNMENTS

D.4 TFTIFKYV

The TFTIFKYV is designed to interface with a small number of LCDs, principally from Kyocera, that use a 33-way Molex connector.

The TFTIFKYV plugs into J9 on the RED320 using a ribbon cable, the TFTIF-CAB7 or TFTIF-CAB11 available from DSP Design.

The RED320's four touch-screen signals are routed from the TFTIFKYV main connector J4, to two touch-screen connectors J2 and J5 via four solder links, LK4-7. J2 is FFC connector and J5 is a board to wire connector. LK4-7 need to be fitted for the touch-screen interface to be enabled.

The TFTIFKYV interfaces to Microsemi backlight inverters, which have an input to control the backlight brightness. The Microsemi brightness input can be controlled by either a potentiometer or the LCD_ADJ PWM signal. The LCD_ADJ signal is routed to RED320 connector J9 pin 33 through solder link LK6 on the RED320, which must be set to the 2-3 position (even if you are not using LCD_ADJ). Please refer to the Platform Guide for the relevant operating system for details of LCD_ADJ LCD brightness control support for the RED320.

To configure the TFTIFKYV for PWM control:

- set LK1 on the TFTIFKYV to position 1-2
- set LK6 on the RED320 to 2-3.

To configure the TFTIFKYV for potentiometer control:

- set LK1 on the TFTIFKYV to position 2-3.
- set LK6 on the RED320 to 2-3.

The TFTIFKYV has its own Technical Reference Manual, which provides more information on this product, including further solder link options..

D.5 AAVGA CRT / VGA INTERFACE BOARD

A VGA CRT or LCD monitor can be driven with the addition of the AAVGA adapter board. The AAVGA plugs directly into J9 on the RED320 and provides a standard 15-way D-type VGA connector. The AAVGA converts the parallel data from the RED320 to analog RGB signals displaying up to 64k colours.

APPENDIX E - RED320 CONNECTOR PIN ASSIGNMENTS

E.1 RED320 CONNECTOR SUMMARY

Table E1 provides a summary of the connectors used on the RED320. Note that the mating connector for the 100-way and 120-way connectors are the Hirose FX8-100P-SV1 and FX8-120P-SV1.

NAME	FUNCTION	TYPE	MANUFACTURER / PART NUMBER
J1	Peripherals	2 x 22 way 2mm pitch pin header	ETC SS2-044-H064/1-55/2A
J2	(There is no connector labelled J2 on this PCB revision)		
J3	JTAG and debug	2 x 10-way 2mm pitch header	ETC SS2-020-H064/2-55/2A
J4	Peripherals	2 x 22 way 2mm pitch pin header	ETC SS2-044-H064/1-55/2A
J5	Inter-board	120 way board to board	Hirose FX8-120S-SV
J6	Secure Digital 2	SD socket with push/push mechanism	Molex 500998-0900
J7	Secure Digital 1	SD socket with push/push mechanism	Molex 500998-0900
J8	Inter-board	100 way board to board	Hirose FX8-100S-SV
J9	Display and touch screen	2 x 20 way 1.27mm pitch pin header	ETC SS2-040-H70/0-55/11A

TABLE E1 - RED320 CONNECTOR SUMMARY

Figures E1 and E2 show the connector positions on the RED320.

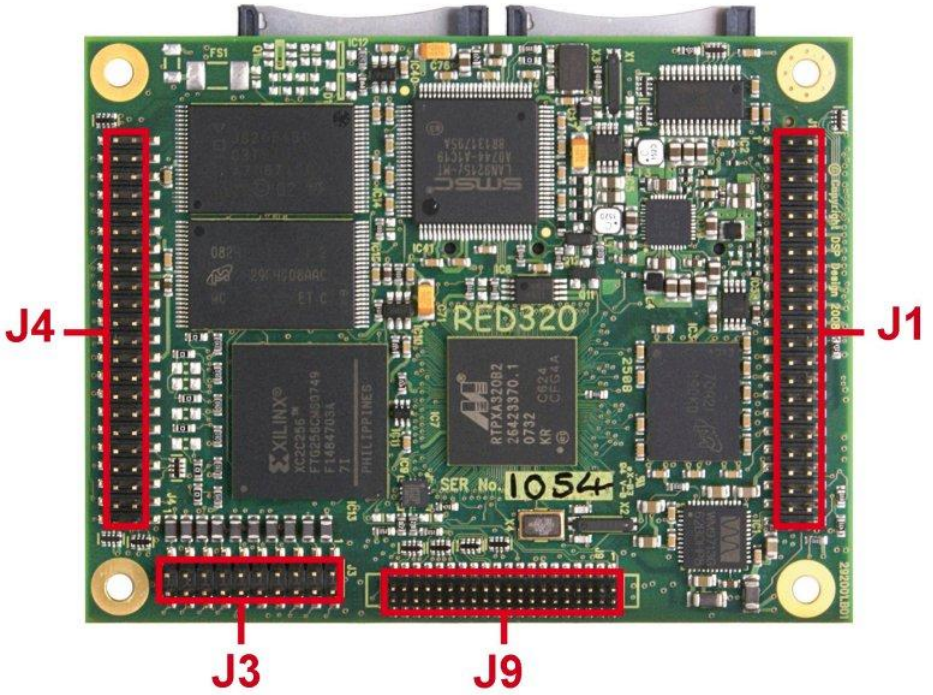

FIGURE E1 - RED320 CONNECTOR POSITIONS – TOP SIDE

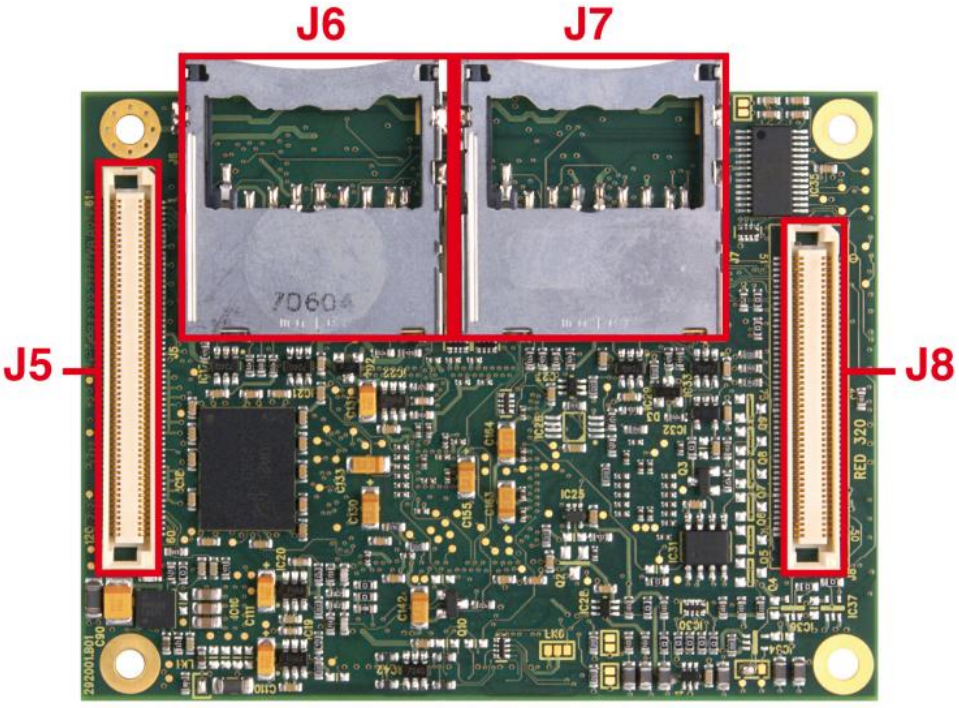

FIGURE E2 - RED320 CONNECTOR POSITIONS – BOTTOM SIDE

E.2 PERIPHERAL CONNECTOR J1

Connector J1 allows access to some of the peripherals and power supplies:

- Serial port COM1
- Some GPIO signals
- Audio signals
- Push-button reset
- 3.3V, 5V and battery voltages

To connect to J1 use 1mm pitch ribbon cable and a 2 x 22 way 2mm pitch ribbon cable connector. Pin 1 is identified in Figure B1 in Appendix B by a triangle. **Take care not to confuse J1 and J4, which use the same connectors.**

Some pins are reserved for future use. Do not make any connection to these pins.

PIN	SIGNAL	PIN	SIGNAL
1	DCD1	2	DSR1
3	RXD1	4	RTS1
5	TXD1	6	CTS1
7	DTR1	8	RI1
9	GND	10	GND
11	VCC_5V	12	VCC_5V
13	VCC_5V	14	VCC_5V
15	VCC_5V	16	VCC_3V3
17	VCC_5V	18	VCC_3V3
19	GND	20	VBACK_BAT
21	UIO19	22	VCC_EXP (do not connect)
23	PB_RST#	24	UIO20
25	GND	26	Reserved
27	GND	28	UIO21
29	GND	30	UIO22
31	GND	32	UIO23
33	GND	34	UIO24
35	Reserved	36	Reserved
37	AGND	38	AGND
39	LINEOUTR	40	LINEOUTL
41	SPKR1	42	SPKR2
43	AGND	44	MIC

TABLE E2 - J1 PERIPHERAL CONNECTOR PIN ASSIGNMENTS

E.3 PERIPHERAL CONNECTOR J4

Connector J4 allows access to some of the peripherals and power supplies:

- Serial ports COM2 and COM3
- Some GPIO signals
- I²C bus
- 3.3V and 5V voltages

To connect to J4 use 1mm pitch ribbon cable and a 2 x 22 way 2mm pitch ribbon cable connector. Pin 1 is identified in Figure B1 in Appendix B by a triangle. **Take care not to confuse J1 and J4, which use the same connectors.**

Some pins are reserved for future use. Do not make any connection to these pins.

PIN	SIGNAL	PIN	SIGNAL
1	UIO0	2	UIO8
3	UIO1	4	UIO9
5	UIO2	6	UIO10
7	UIO3	8	UIO11
9	UIO4	10	UIO12
11	UIO5	12	UIO13
13	UIO6	14	UIO14
15	UIO7	16	GND
17	VCC_3V3	18	GND
19	GND	20	GND
21	UIO15	22	SCL
23	UIO16	24	SDA
25	UIO17	26	TXD3
27	UIO18	28	RXD3
29	VCC_5V	30	GPIN0
31	VCC_5V	32	GPIN1
33	VCC_5V	34	GPOUT0
35	VCC_5V	36	GPOUT1
37	VCC_5V	38	Reserved
39	GND	40	Reserved
41	VCC_EXP (do not connect)	42	TXD2
43	GND	44	RXD2

TABLE E3 - J4 PERIPHERAL CONNECTOR PIN ASSIGNMENTS

E.4 INTER-BOARD CONNECTORS J5 AND J8

Connectors J5 and J8 enable the RED320 to plug onto another PCB. They contain some of the signals available on the ribbon cable connectors J1, J2, J4 and J9 and also other signals such as the 16-bit expansion bus. Do not connect to the “Reserved” pins.

Pin 1 is identified in Figure B2 in Appendix B by a triangle or a “1”. J5 pins are numbered 1-60 on one row and 61-120 on the other, with pins 1 and 61 opposite each other. J8 pins are numbered 1-50 on one row and 51-100 on the other.

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DCD1	31	GND	61	DSR1	91	Reserved
2	RXD1	32	GND	62	RTS1	92	Reserved
3	TXD1	33	GND	63	CTS1	93	Reserved
4	DTR1	34	GND	64	RI1	94	Reserved
5	GND	35	GND	65	GND	95	Reserved
6	VCC_5V	36	GND	66	VBACK_BAT	96	VCC_EXP
7	VCC_5V	37	GND	67	VBACK_BAT	97	Reserved
8	VCC_5V	38	GND	68	VCC_3V3	98	Reserved
9	VCC_5V	39	GND	69	VCC_3V3	99	Reserved
10	GND	40	GND	70	VCC_3V3	100	Reserved
11	GND	41	UIO19	71	PB_RST#	101	UIO20
12	GND	42	GND	72	UIO21	102	Reserved
13	GND	43	USB1CPB	73	UIO22	103	Reserved
14	GND	44	USB1CNB	74	UIO23	104	USB1H2PB
15	GND	45	VBUS	75	UIO24	105	USB1H2NB
16	GND	46	USB1H1PB	76	VCC_5V	106	USB1H2_PWR
17	GND	47	USB1H1NB	77	VCC_5V	107	USB1H1_PWR
18	GND	48	GND	78	VCC_5V	108	Reserved
19	GND	49	GND	79	VCC_5V	109	Reserved
20	GND	50	GND	80	VCC_5V	110	Reserved
21	GND	51	GND	81	VCC_5V	111	Reserved
22	GND	52	GND	82	VCC_5V	112	Reserved
23	GND	53	GND	83	VCC_5V	113	Reserved
24	GND	54	GND	84	VCC_5V	114	Reserved
25	GND	55	Reserved	85	VCC_5V	115	AGND
26	RDP	56	LINEOUTR	86	LAN_3V3A	116	LINEOUTL
27	RDN	57	AGND	87	EXT_WAKEUP1	117	AGND
28	GND	58	SPKR1	88	Reserved	118	SPKR2
29	TDP	59	AGND	89	LINK#	119	AGND
30	TDN	60	AGND	90	10/100#	120	MIC

TABLE E4 - J5 INTER-BOARD CONNECTOR PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	BA0	26	EXPRST1#	51	BD0	76	TXD2
2	BA1	27	EXPRST2#	52	BD1	77	RXD2
3	BA2	28	EXPCS2#	53	BD2	78	VCC_EXP
4	BA3	29	VCC_5V	54	BD3	79	GND
5	BA4	30	VCC_5V	55	BD4	80	GND
6	BA5	31	VCC_3V3	56	BD5	81	GND
7	BA6	32	VCC_3V3	57	BD6	82	GND
8	BA7	33	UIO8	58	BD7	83	SCL
9	BA8	34	UIO0	59	BD8	84	SDA
10	BA9	35	UIO2	60	BD9	85	TXD3
11	BA10	36	UIO3	61	BD10	86	RXD3
12	BA11	37	UIO4	62	BD11	87	UIO7
13	BA12	38	UIO15	63	BD12	88	UIO5
14	BA13	39	UIO16	64	BD13	89	UIO12
15	BA14	40	UIO17	65	BD14	90	UIO13
16	BA15	41	UIO18	66	BD15	91	UIO6
17	BA16	42	VCC_5V	67	BBE0#	92	UIO14
18	BA17	43	VCC_5V	68	BBE1#	93	GND
19	BA18	44	VCC_5V	69	PB_RST#	94	GPIN0
20	BA19	45	VCC_5V	70	BRD#	95	GPIN1
21	BA20	46	UIO1	71	BWR#	96	GPOUT0
22	BA21	47	UIO9	72	EXPCS1#	97	GPOUT1
23	BA22	48	UIO11	73	EXPINT1#	98	UIO10
24	BA23	49	VCC_5V	74	EXPINT2#	99	GND
25	BRDY	50	VCC_5V	75	EXPDREQ	100	GND

TABLE E5 - J8 INTER-BOARD CONNECTOR PIN ASSIGNMENTS

E.5 DISPLAY CONNECTOR J9

Connector J9 is for connection to an LCD. As well as the LCD signals it carries signals for a touchscreen and backlight inverter control.

To connect to J9 use 0.025-inch pitch ribbon cable and a 2 x 20 way 1.27mm (0.05-inch) pitch ribbon cable connector. Pin 1 is identified in Figure B1 in Appendix B by a triangle.

Some pins are reserved for future use. Do not make any connection to these pins.

PIN	SIGNAL	PIN	SIGNAL
1	BKL_EN	2	LCD_EN
3	GND	4	LCD_DCLK
5	GND	6	LCD_HSYNC
7	GND	8	LCD_VSYNC
9	TSXP	10	TSXN
11	GND (R0) (1)	12	LCD_R1
13	GND	14	LCD_R2
15	LCD_R3	16	LCD_R4
17	GND	18	LCD_R5
19	Reserved	20	Reserved
21	GND	22	LCD_G0
23	LCD_G1	24	LCD_G2
25	VCC_3V3	26	LCD_G3
27	LCD_G4	28	LCD_G5
29	LCD_3V3	30	TSYN
31	TSYP	32	GND (B0) (1)
33	VCC_5V / LCD_ADJ (2)	34	LCD_B1
35	LCD_B2	36	LCD_B3
37	VCC_5V	38	LCD_B4
39	LCD_B5	40	LCD_DE

NOTES:

1) The RED320 provides a 16-bit colour bus. Some LCD interface boards available from DSP Design support an 18-bit colour bus. The unused pins on RED320 (R0 and B0) are connected to GND.
2) VCC_5V is selected by default but can be changed at LK6.

TABLE E6 - J9 DISPLAY CONNECTOR PIN ASSIGNMENTS

E.6 JTAG AND DEBUG CONNECTOR

The RED320 provides a JTAG connector J3 to support for the PXA320 processor and Xilinx CPLD. J3 is therefore reserved for manufacturing use by DSP Design only.

APPENDIX F - REDCONN SERVICES BOARD FOR THE RED320

F.1 INTRODUCTION

The REDCONN is a services board for the RED320 processor board. It breaks out the interfaces from RED320 to standard connectors.

The REDCONN provides the following standard PC connectors mounted along two edges of the board for easy mounting in an enclosure:

- One RJ45 Ethernet socket.
- Two USB host Type-A connectors in a single stacked package.
- One USB device Mini-AB connector.
- One 9-way male D-type connector.
- Two 3.5mm audio jacks for line-out (green) and microphone (pink).
- One 2mm power jack.

The REDCONN also provides two board-to-wire connectors for interfacing to a speaker and backlight inverter within an enclosure.

There are two variants of the REDCONN available:

- The REDCPOE includes PoE capability and excludes the DC input power jack.
- The REDCDC includes the DC input power jack and excludes PoE capability.

The differences are described in more detail in section F.6. Unless otherwise described in the following sections, the two variants will be referred to as the REDCONN.

F.2 BLOCK DIAGRAM

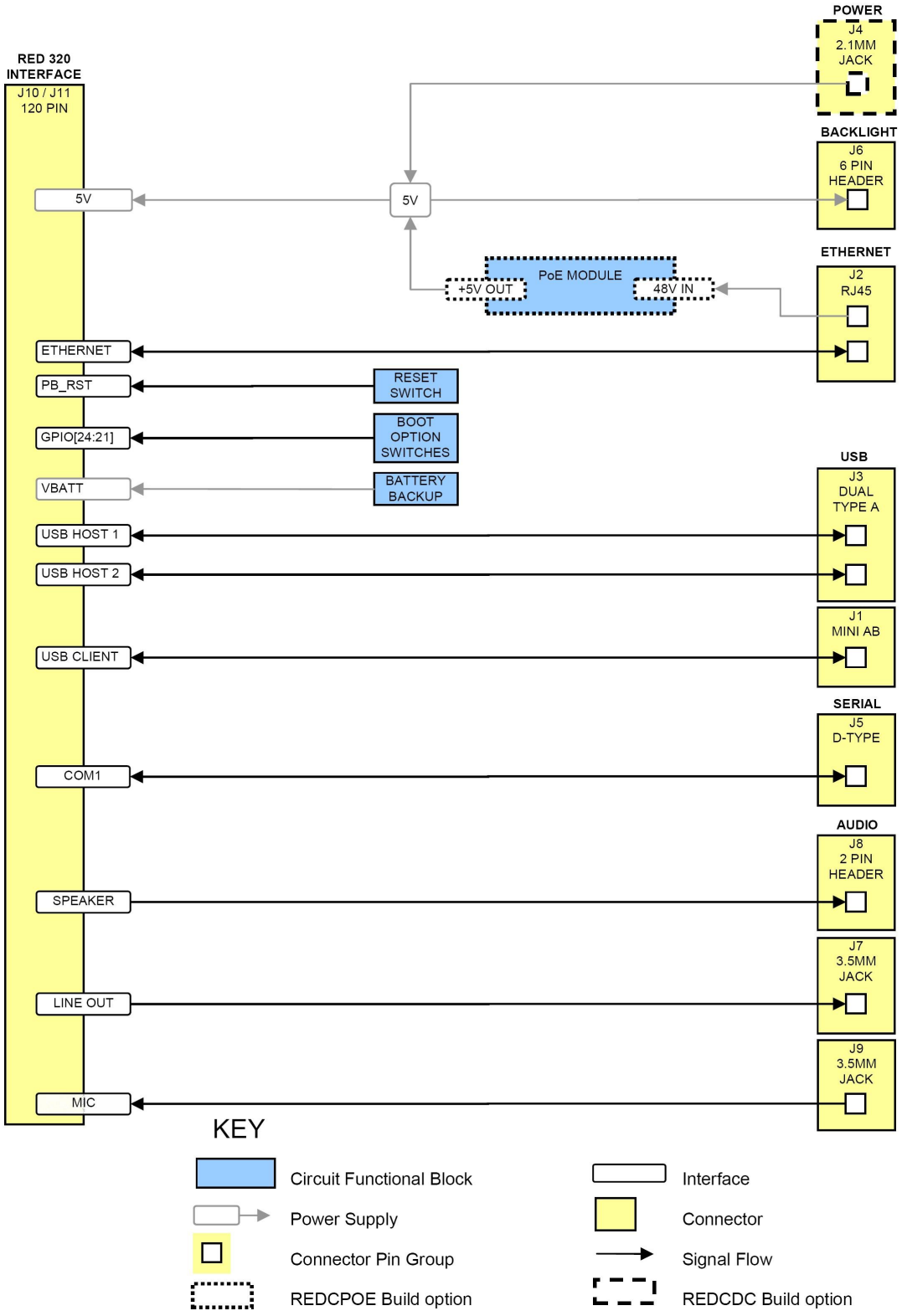

FIGURE F1 - REDCONN BLOCK DIAGRAM

F.3 INTERFACING REDCONN TO RED320

The RED320 connects to the REDCONN through the 120-way connectors. If the REDCONN is to be fitted end to end with the RED320 then connector J5 of the RED320 mounts with J10 of the REDCONN as shown in Figure F2. If the REDCONN is to be fitted underneath the RED320 then connector J5 of the RED320 mounts with J11 of the REDCONN as shown in Figure F3.

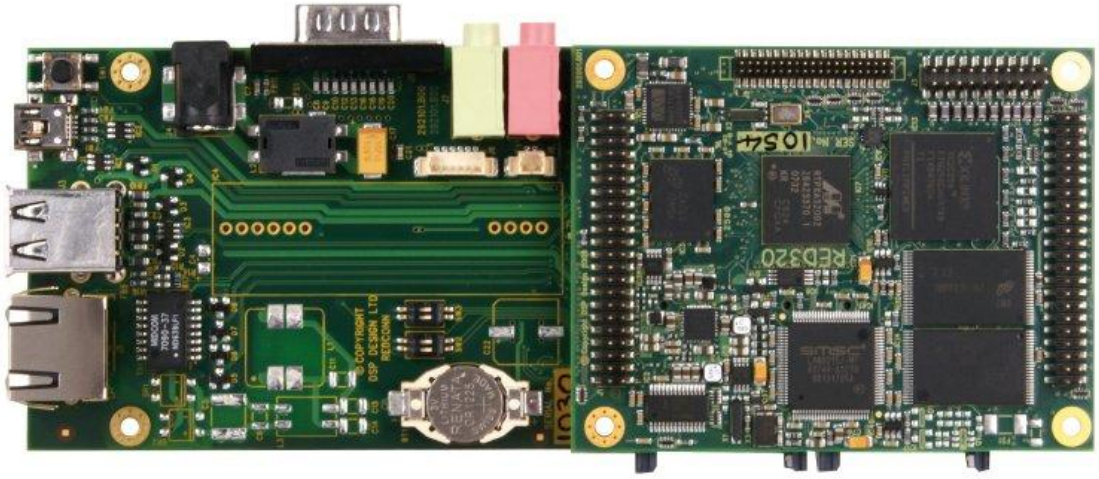

FIGURE F2 - RED320 AND REDCONN CONNECTED END-TO-END

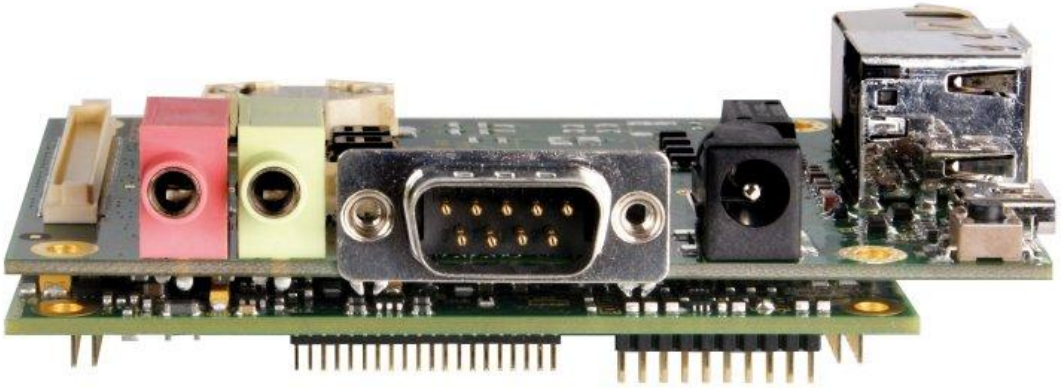

FIGURE F3 - RED320 AND REDCONN CONNECTED BACK-TO-BACK

F.4 REDCONN CONNECTOR SUMMARY

Table F1 provides a summary of the connectors on the REDCONN. Figures F4 and F5 show their positions.

The function and pin assignment for the backlight connector J6 and speaker connector J8 are detailed in subsequent sections of this appendix. The function and pin assignment for connectors J10 and J11 are identical to that given in Appendix F for the RED320 connector J5. The remaining connectors use standard pin allocations and are not detailed in this document.

NAME	FUNCTION	TYPE	MANUFACTURER / PART NUMBER
J1	USB Device	Mini AB USB socket	Samtec MUSB-05-S-AB-SM-A
J2	Ethernet	RJ45 socket	Kycon KYC-GWLX-S9-88-G/Y
J3	USB Host	Dual (stacked) USB Type A socket	AMP 5787617-1
J4	Power	2mm power jack (REDCDC only)	Kycon KLDX-SMT2-0202-A
J5	COM1 serial port	9 way male D-type	ETC-SDM-009-US91-95/N
J6	LCD backlight	6 way 1.25mm pitch pin header	Molex 53398-0671
J7	Audio line out	3.5mm audio jack (3-terminal, green)	Connect-Tech CTP-322-1-LG
J8	Speaker	2 way 1.25mm pitch pin header	Molex 53398-0271
J9	Microphone	3.5mm audio jack (3-terminal, pink)	Connect-Tech CTP-322-1-PK
J10	RED320 interface	120-way board to board	Hirose FX8-120P-SV1
J11	RED320 interface	120-way board to board	Hirose FX8-120P-SV1

TABLE F1 - RECONN CONNECTOR SUMMARY

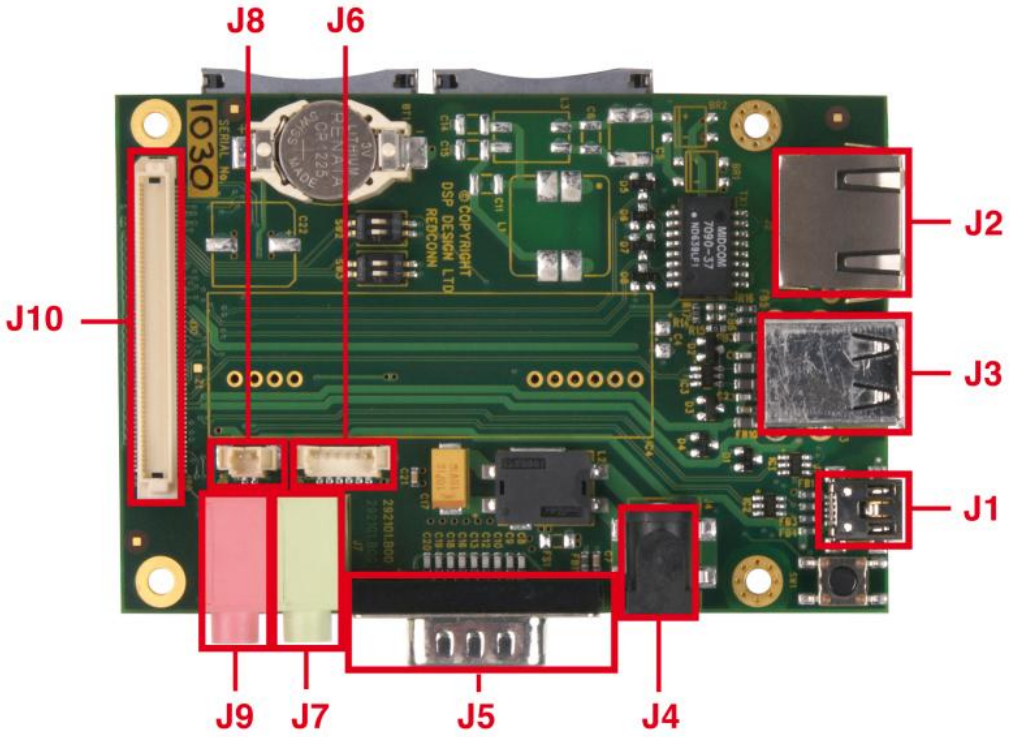

FIGURE F4 - REDCONN CONNECTOR LOCATIONS – TOP SIDE

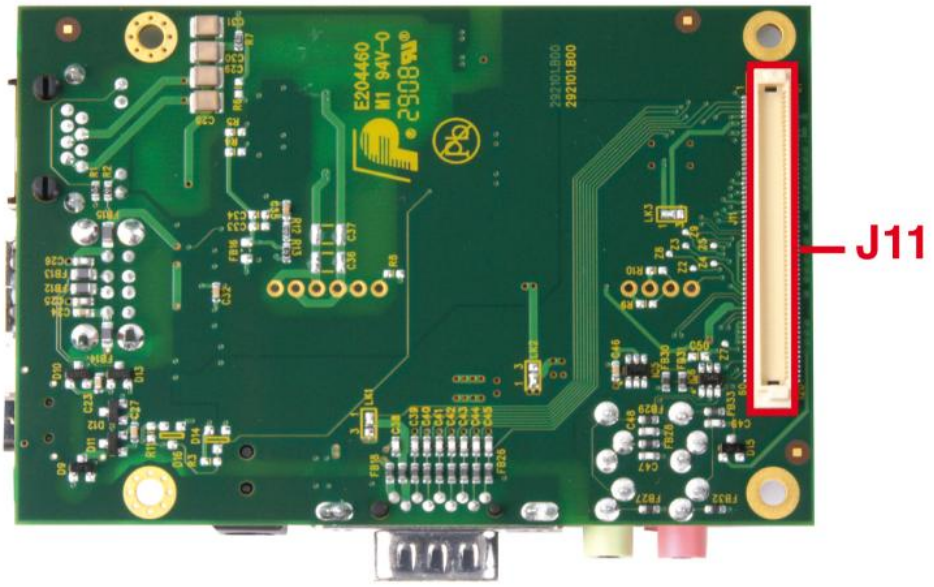

FIGURE F5 - REDCONN CONNECTOR LOCATIONS – BOTTOM SIDE

F.5 COM1 SERIAL PORT

The REDCONN provides a full function 9-pin D-type socket J5 for COM1.

The REDCONN provides EMC filtering on all pins of J5. The REDCONN does not provide ESD protection on any of the COM1 signals. However the ICL3243E transceiver on the RED320 provides ESD protection. See section 2.6 for more details.

There is a solder link option to connect pin 9 of this connector to VCC_5V through a fuse. Contact DSP Design if you have a volume requirement for this feature.

F.6 ETHERNET AND POWER

The REDCONN provides an RJ45 socket J2 for Ethernet. This includes two LEDs that indicate LAN activity. The RJ45 socket connects to the RED320 via one of the board-to-board connectors J10 or J11 and an isolation transformer and the necessary passive components.

The REDCONN provides EMC filtering and ESD protection on all pins of J2.

The REDCDC variant provides a DC jack, J4, for connecting to standard brick power supplies, such as the TCONN-PSU available from DSP Design. In this case the Ethernet interface is a conventional type. Figure F6 shows a block diagram of the REDCDC Ethernet circuit and its interface with the RED320. The REDCDC provides EMC filtering on the DC jack input. The REDCDC does not provide ESD protection on the DC jack input.

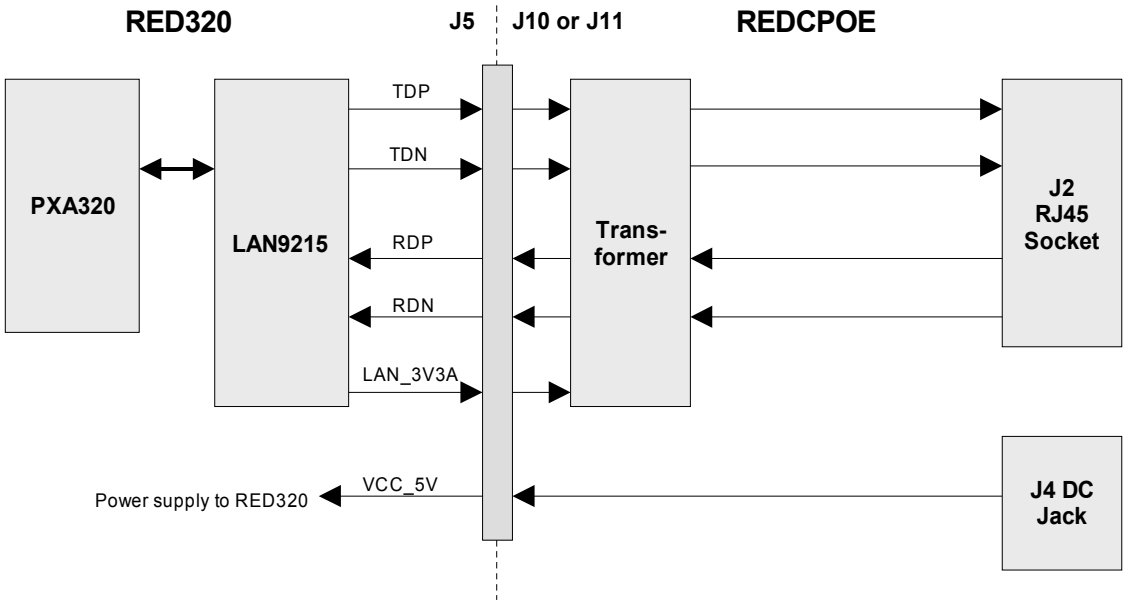

FIGURE F6 - REDCDC ETHERNET BLOCK DIAGRAM

The REDCPOE variant allows power to be sourced using IEEE802.3af Power Over Ethernet technology. This technology superimposes a 48V DC voltage on the Ethernet cable. Components on the REDCPOE feed this 48V through an isolated power supply and provide a regulated 5V for the RED320. Figure F7 shows a block diagram of the

REDCPOE Ethernet circuit and its interface with the RED320. Note that power is derived from the centre-taps of the TX and RX transformers, and may also be supplied on the spare pairs.

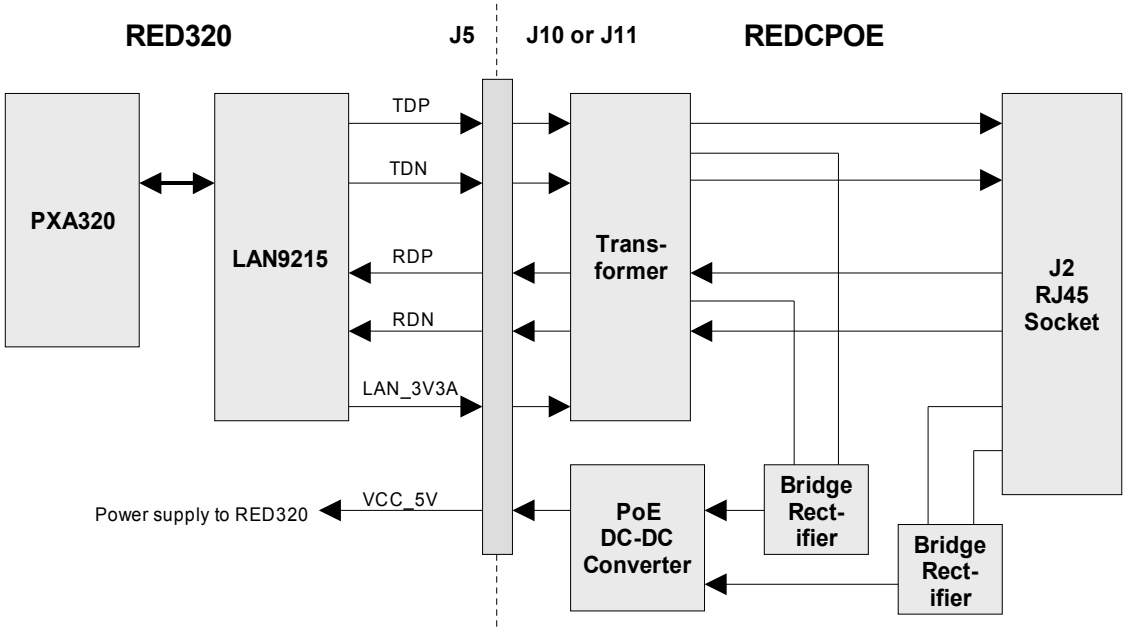

FIGURE F7 - REDCPOE ETHERNET AND POE BLOCK DIAGRAM

F.7 USB HOST

The REDCONN provides two Type-A USB host ports in a single socket J3. The bottom socket corresponds to USB port 1 signals, and the top socket to USB port 2 signals.

The REDCONN provides EMC filtering on all pins of J3 including power and ground.

The REDCONN provides ESD protection on all pins of J3 except ground. The USB data pairs have clamping diodes to VCC_3V3 and GND. The switched USB power rail has clamping diodes to VCC_5V and GND.

F.8 USB DEVICE

The REDCONN provides a USB device port socket J1.

The REDCONN provides EMC filtering on all pins of J1 including VBUS and ground. The REDCONN provides ESD protection on all pins of J1 except ground. The USB data pairs have clamping diodes to VCC_3V3 and GND. The VBUS input has clamping diodes to VCC_5V and GND.

F.9 AUDIO

The REDCONN provides two 3.5mm audio jacks J7 and J9 and a speaker connection J8.

J7 provides stereo line output and uses the standard green identification. J9 provides mono microphone input and uses the standard pink identification.

The REDCONN provides a two pin board to wire connector J8 which allows for direct connection to a 4Ω or 8Ω mono speaker.

The REDCONN provides EMC filtering on all pins of J7, J8 and J9 including ground.

The REDCONN provides ESD protection on all signals connected to J7, J8 and J9. The microphone and line out signals have clamping diodes to VCC_3V3 and GND. The mono speaker outputs have clamping diodes to VCC_5V and GND.

F.10 SWITCHES

The REDCONN provides four DIL switches. The switches connect to four of the GPIOs (UIO21, UIO22, UIO23 and UIO24). The switch positions may be read by the operating system to select different boot options. Please refer to the Platform Guide for the relevant operating system for further details.

F.11 RESET

The REDCONN provides a push button reset switch SW1. The switch connects to the PB_RST# input on the RED320. When pressed, the switch will force a cold reset on the RED320.

F.12 RTC BATTERY

The REDCONN provides a 3.0V lithium CR1225 battery in a battery holder BT1. The battery connects to the VBACK_BAT input on the RED320 via one of the board-to-board connectors J10 or J11. The battery provides backup for the RTC when power is removed from the RED320.

The REDCONN provides a solder link, LK3, which provides the following options:

- Fitted 1-2, battery connected to VBACK_BAT. This is the default setting
- Fitted 2-3, battery isolated, VBACK_BAT connected to GND.
- Not fitted, battery isolated, VBACK_BAT not connected on the REDCONN.

All links are located on the bottom side of the REDCONN, and are clearly marked - pin 1 and pin 3 are identified on the silkscreen for each link.

If short circuited may explode or leak, causing injury or damage to the equipment. To prevent short circuits, observe the following guidelines:

- Remove the battery when changing the setting of LK3.
- Use insulated tools when removing the battery from the holder.
- Ensure the battery is not placed on a conductive surface.
- After changing the setting of LK3 and before reinstalling the battery ensure all three pads are not connected together.

F.13 BACKLIGHT POWER

The REDCONN provides a six pin board to wire connector J6. The connector provides either 5V or 3.3V to backlight inverters. Table F2 lists connector J6 pin allocations.

SIGNAL	J6 PIN	DESCRIPTION
VCC_5V or VCC_3V3	4, 5, 6	5V or 3.3V selected by solder link LK2
GND	1, 2, 3	Ground

TABLE F2 - BACKLIGHT CONNECTOR J6 PIN ASSIGNMENTS

The REDCONN provides a solder link, LK2, which provides the following options:

- Fitted 1-2: J6 is connected to VCC_5V. This is the default setting.
- Fitted 2-3: J6 is connected to VCC_3V3.
- Not fitted: J6 pins 3, 4 and 5 are not connected on the REDCONN.

All links are located on the bottom side of the REDCONN, and are clearly marked - pin 1 and pin 3 are identified on the silkscreen for each link.

After changing the setting of LK2 ensure all three pads are not connected together.

F.14 CHASSIS

The REDCONN provides four mounting holes. Two are connected to a CHASSIS plane and two are isolated from all signals and planes. The metal parts of connectors J1, J2, J3 and J5 are connected to the CHASSIS plane.

The two mounting holes connected to CHASSIS are the mounting holes closest to the USB and RJ45 sockets.

The CHASSIS plane connects to the GND plane via a single ferrite bead.

F.15 ASSEMBLY AND MECHANICAL DRAWINGS

High resolution REDCONN assembly and mechanical drawings are available on the DSP Design website.

F.16 REDCONN DIMENSIONS

- PCB dimensions are 97.5mm x 65.0mm.
- PCB thickness is 1.6mm.
- Maximum component height above the PCB is 16.20mm.
- Maximum component height below the PCB is 2.5mm.

F.17 WEIGHT

- DSP-REDCDC 48g.
- DSP-REDCPOE 64g.

F.18 OPERATING TEMPERATURE RANGE

-20°C to +85°C.

F.19 HUMIDITY

10% - 90% non-condensing.

APPENDIX G - FAULT REPORTING

DSP Design makes every effort to ship products and documentation that are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a “Product Fault Report” form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to DSP Design with the faulty product.

Prior to returning a faulty product, please check the following:

3) The board has been correctly configured for the intended application (see earlier appendix for board installation details).
4) The power supplies are providing correct voltage levels.
5) Cabling to the board is sound and connected correctly.
6) Other cards in the system are known to be correctly configured and functioning.
7) PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT			
CUSTOMER INFORMATION:		**PRODUCT INFORMATION:**	
Company Name:		Product Name:	
Contact Name:		Serial No.:	
Phone No:		Date of return:	
SYMPTOMS OBSERVED:			
SYSTEM CONFIGURATION (e.g. other boards present, operating system and software):			
For DSP Design Use:			
Product Test Report:			
Date of Receipt:		Repaired by:	
Charges to be invoiced:			
Date of Return:		Returned by:	

TABLE G1 - PRODUCT FAULT REPORT FORM

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