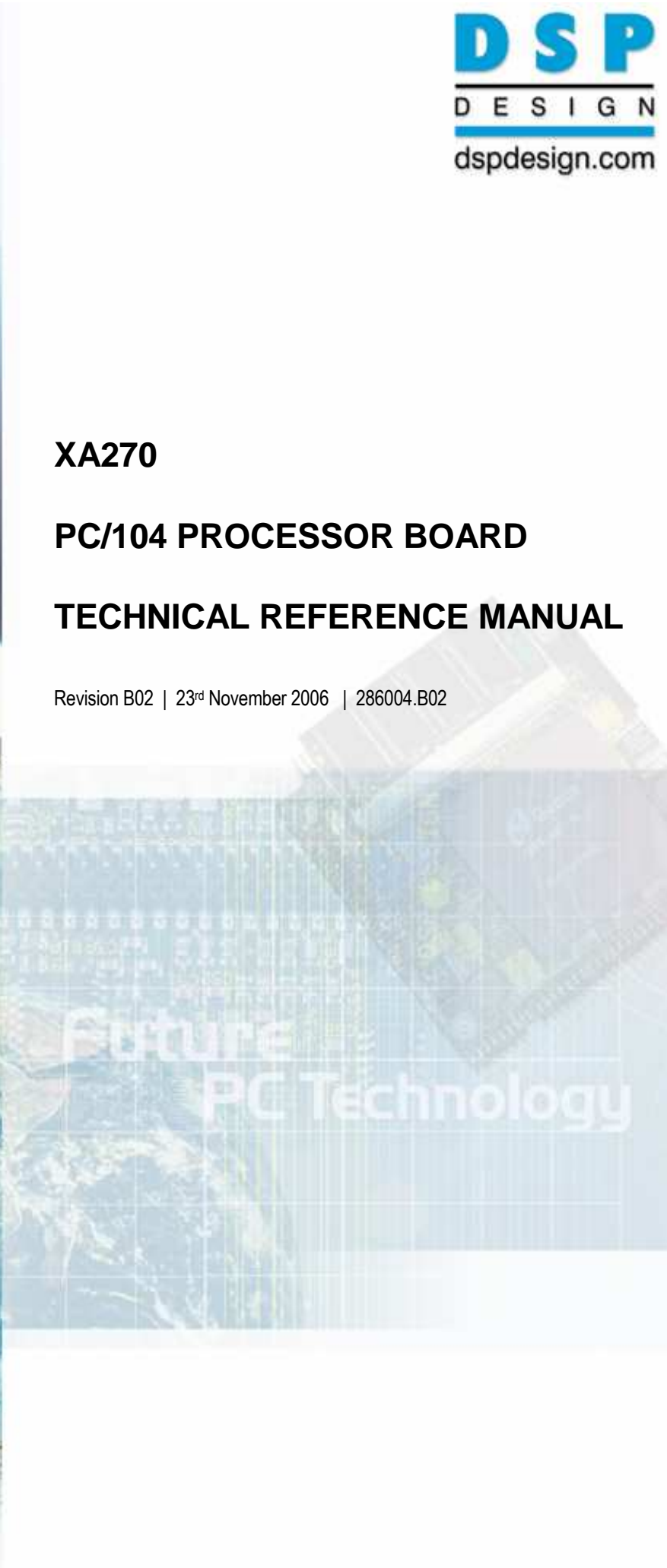


XA270

PC/104 PROCESSOR BOARD

TECHNICAL REFERENCE MANUAL

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REVISION HISTORY

Date	Rev	By	CR No	Change
31/10/06	B00	IKD	5601	This is the first release of this manual.
1/11/06	B01	IKD	5602	ISA I/O and memory cycles amended.
23/11/06	B02	IKD	5609	8-bit and 16-bit ISA I/O cycles amended. References to keypad/keyboard removed from sections 1.2, 2.1, 2.18.2 and A.16. Connector J8 changed from 2.54mm to 2mm in Table 1 and section 2.18.2. New paragraph added to section 2.18.2.

REFERENCES

Intel® PXA270 Processor Family Developer's Manual.
 PC/104 specification v2.5.
 Compact Flash specification v4.0.
 USB specification v1.1.
 RoHS Directive 2002/95/EC.
 I²C specification v2.0.
 IEEE 802.3 standard.

1 INTRODUCTION

This manual describes the B00 revision of the Artemis XA270 PC/104 form-factor processor board.

1.1 OVERVIEW

The XA270 is a RoHS compliant board using the Intel Xscale™ PXA270™ high performance RISC, low-power and high-integration systems-on-a-chip (SOC) processor. Low power consumption in normal operation and during sleep, make the XA270 ideal for battery operated systems.

The XA270 operates as a standalone module requiring only a single 5V input, or customers can either interface to the XACONN (a connector board for the XA270) or their own hardware.

1.2 XA270 FEATURES

- The Intel® PXA270™ processor uses the integer instruction set of the ARM* Architecture V5TE, providing high performance at very low power consumption when clocked at a maximum of 520MHz.
- PC/104 form factor, offering expansion using the PC/104 bus.
- 128Mbytes of SDRAM soldered to the board.
- 64Mbytes of Spansion Mirror-Bit Flash containing the operating system and Flash File System.
- On-board Compact Flash socket allowing a range of Compact Flash cards to be used for memory or peripheral expansion.
- 10/100 Base-T Ethernet port.
- 16-bit parallel TTL interface supporting a wide range of TFT LCDs at resolutions up to 800x600.
- Four-wire resistive touch screen controller.
- Two channel 12-bit ADC with 0-7.5V input range.
- Four USB 1.1 host ports.
- One USB 1.1 client port.
- Five serial ports. COM1, COM2 and COM3 are full function RS232, and COM4 and COM5 are limited function RS232.

- AC97 codec providing mono microphone input, stereo line outputs and stereo headphone outputs.
- Two RTCs, one with an input for an external battery.
- One I²C multi-master serial bus providing simple expansion.
- User I/O signals configurable as general purpose I/O.
- Reset input.
- The XA270 consumes very little power from a single 5V power supply even when operating at full speed. The operating system switches off unused circuitry for extremely low power consumption in power managed states.

1.3 PRODUCT HANDLING AND ENVIRONMENTAL COMPLIANCE

1.3.1 Anti-Static Handling

The XA270 and peripherals contain CMOS devices, which can be damaged in the event of static electricity discharging through the device. Please observe anti-static handling precautions when handling the XA270 or when adding or removing connectors.

1.3.2 Electromagnetic Compatibility (EMC)

Although the XA270 and peripherals utilise EMC filtering techniques, it is the user's responsibility to ensure that systems using the XA270 and peripherals are compliant with the appropriate EMC standards.

1.3.3 RoHS Compliance

The XA270 and peripherals are only available as fully RoHS compliant products and do not contain any of the six banned substances above the levels specified in the RoHS Directive 2002/95/EC.

1.4 LAUNCHPAD APPLICATION DEVELOPMENT KIT

DSP Design strongly recommends that you begin your development project by using the LaunchPad Application Development Kit. This is a complete ready to use embedded computer system that is waiting for your application to be placed into the solid-state disk. Figure 1 shows the LaunchPad hardware. Not shown are the complete set of software, manuals and accessories (mouse, keyboard, PSU and cables) that are included in the LaunchPad package. The LaunchPad hardware comprises the following items mounted on a laptop style stand:

- XA270 processor board.
- XACONN connector board.
- LCD and backlight inverter.
- Touchscreen.

The XACONN is a connector board for the XA270 providing standard PC connectors. Please refer to Appendix G for further details.

Using the LaunchPad will greatly reduce your development time, so your product will get to market sooner at a fraction of the engineering costs normally associated with products.

We have two objectives as you begin to use your new LaunchPad Application Development Kit.

Firstly, we expect that within an hour of receiving your LaunchPad you will have set up the hardware, connected it to your LAN and run the demonstration mouse application.

Secondly, we expect that within a day you will have installed the development tools, compiled a sample application, downloaded it to the target hardware, and experimented with debugging this application remotely from the host computer.

So on the second day you can begin developing your real application.

For full details of the LaunchPad Application Development kits see our web site at www.dspdesign.com/launchpad.

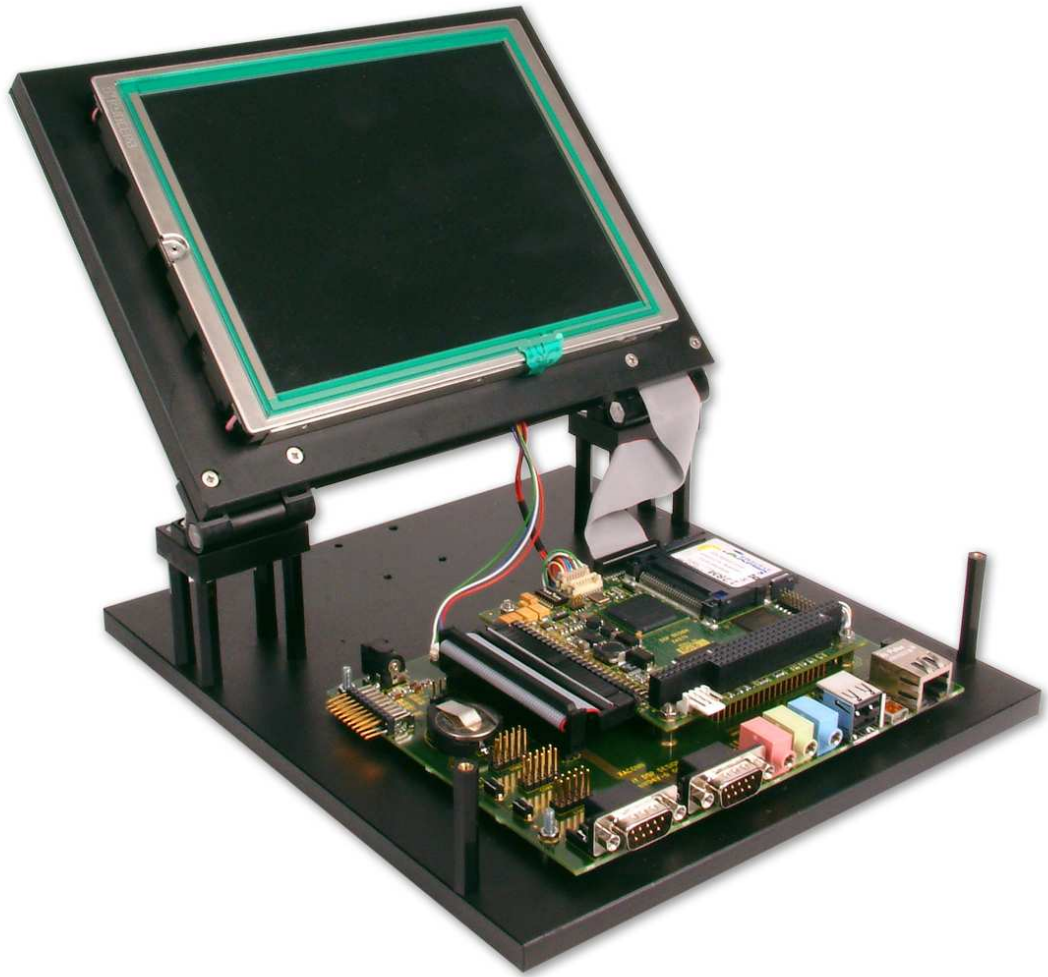


FIGURE 1: THE XA270 LAUNCHPAD

2 HARDWARE

2.1 XA270 CONNECTOR SUMMARY

Table 1 provides a summary of the connectors available on the XA270, along with part numbers where appropriate. The function and pin assignment for each connector is covered in other sections of this manual.

Ref Des	Function	Connector Type or Part Number
J1	PC/104 expansion	104-way PC/104.
J2	LCD	2x20-way 1.27mm pitch header.
J3	USB Host	8-way board to wire, Hirose DF13-8P-1.25V.
J4	USB Host	8-way board to wire, Hirose DF13-8P-1.25V.
J5	Processor JTAG	2x10-way 1.27mm pitch header.
J6	Compact Flash	Type I and II.
J7	General Purpose	2x25-way 2.54mm pitch header.
J8	GPIO	2x10-way 2mm pitch header.
J9	CPLD JTAG	2x10-way 1.27mm pitch header.
J10	Input Power	4-way 2.54mm pitch board to wire with friction lock.
J11	Audio	8-way board to wire, Molex 53261-0871.
J12	Ethernet	8-way board to wire, Hirose DF13-8P-1.25H.
J13	ADC/Touchscreen	9-way board to wire, Molex 53261-0971.
J14	USB Client	8-way board to wire, Hirose DF13-8P-1.25H.

TABLE 1: XA270 CONNECTOR SUMMARY

2.2 XA270 BLOCK DIAGRAM

Figure 2 shows the block diagram of the XA270.

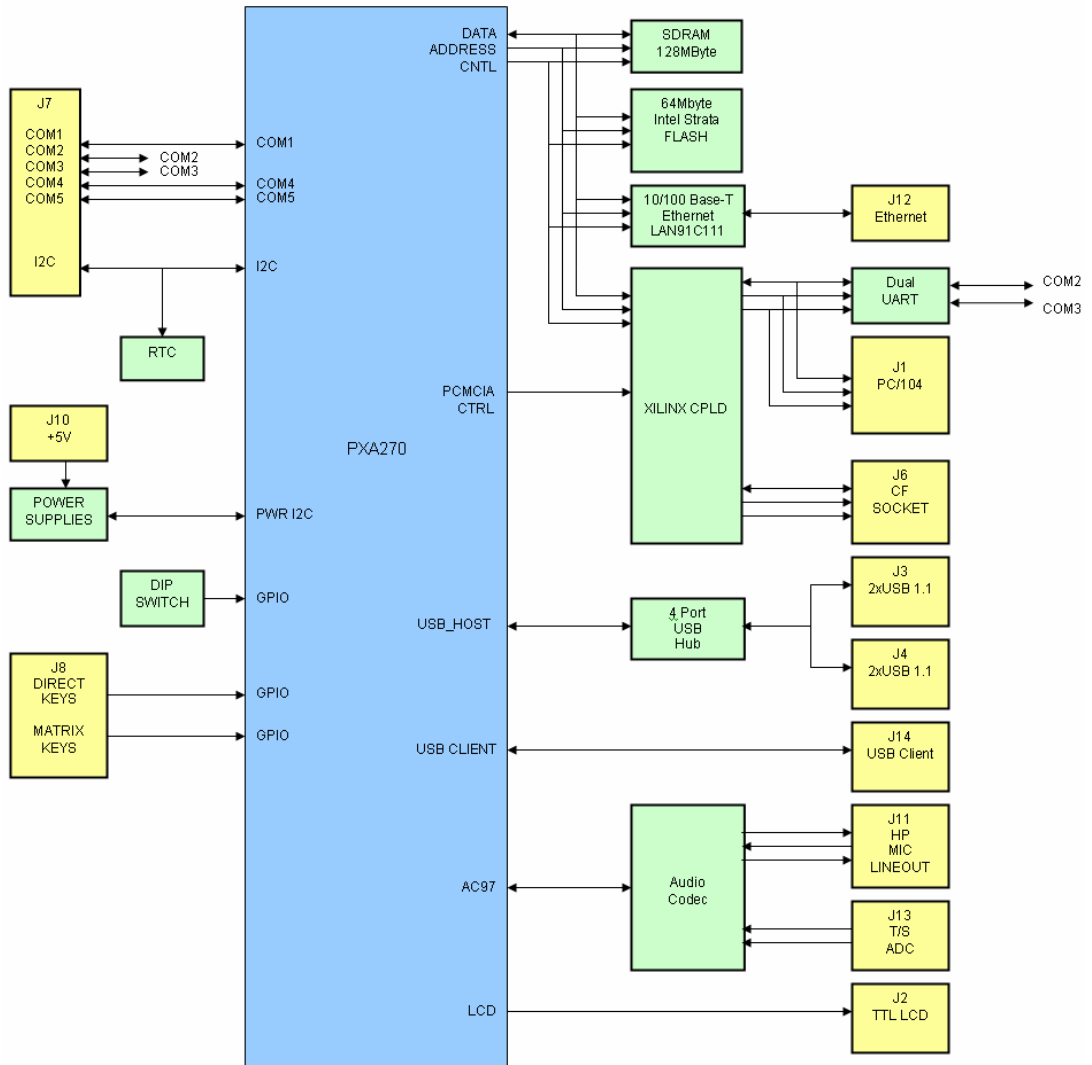


FIGURE 2: XA270 BLOCK DIAGRAM

2.3 PROCESSOR

The Intel® PXA270™ processor is an integrated system-on-a-chip microprocessor for high performance, dynamic, low-power portable handheld and hand-set devices as well as embedded platforms. Figure 3 shows the Intel® PXA270™ processor functional block diagram.

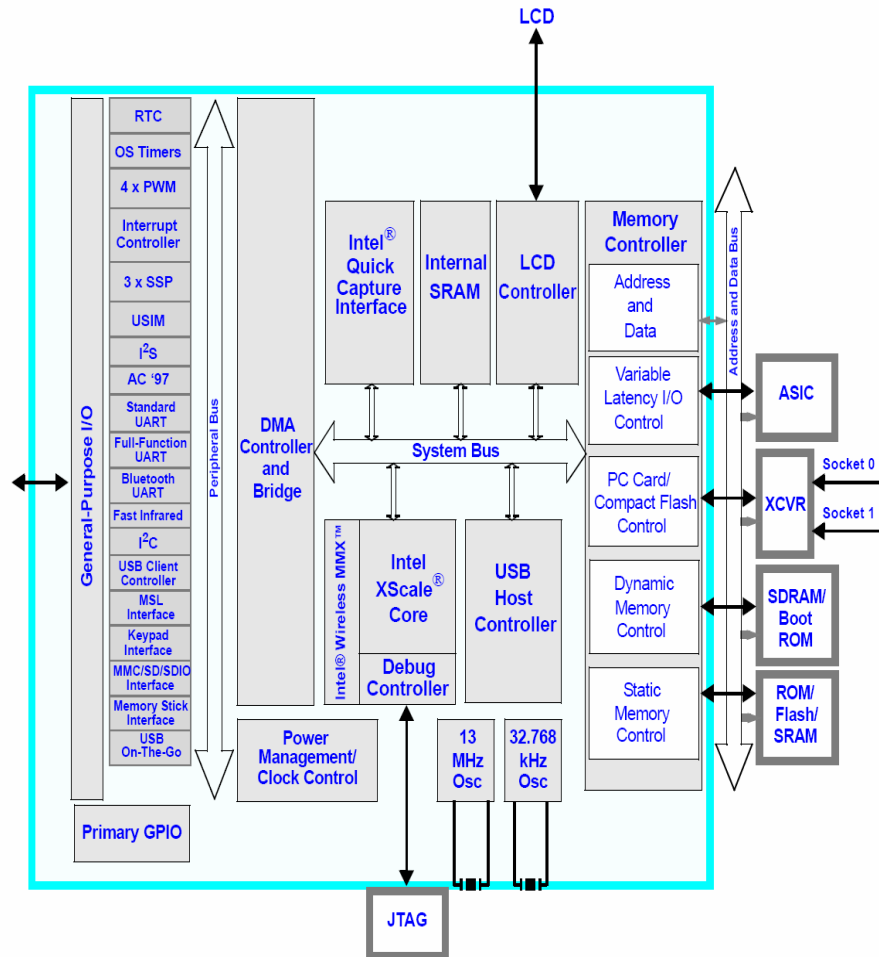


FIGURE 3: INTEL® PXA270™ PROCESSOR BLOCK DIAGRAM

2.4 SDRAM

The XA270 provides 128Mbytes of Synchronous Dynamic RAM (SDRAM) as standard, soldered to the PCB.

The SDRAM is connected to the Intel® PXA270™ processor via a shared 32-bit wide system bus and operates at a maximum frequency of 104MHz.

Some of the SDRAM is allocated to the internal LCD controller, using a technique referred to as unified memory architecture (UMA).

2.5 FLASH MEMORY

The XA270 provides 64Mbytes of Spansion Mirror-Bit Flash as standard, soldered to the PCB.

The 16-bit wide Flash is connected to the Intel® PXA270™ processor via the shared system bus.

The Flash typically contains the operating system and a Flash File System (FFS) for storing user applications and data. Please refer to the Developer's Guide for the specific operating system for further details.

2.6 COMPACT FLASH

The XA270 provides a single on-board Compact Flash (CF) socket suitable for 3.3V memory and I/O cards, providing both memory and peripheral expansion. The CF socket is mapped to the Intel® PXA270™ PC Card Controller socket 0 space.

Power switching circuitry and buffers are provided to isolate the Compact Flash card reducing power consumption and to provide hot swap capability under operating system control.

2.7 SERIAL PORTS

The XA270 provides five RS232 serial ports that are labelled as COM1 through COM5.

Each UART is similar to the industry standard 16550 UART and can be independently configured for 5-8 data bits, 1-2 stop bits, even, odd, mark or no parity and baud rates supported by the operating system. Please refer to the Developer's Guide for the specific operating system for further details.

Each port uses ICL3243E transmitters/receivers, which meet EIA/TIA-232 and V.28/V.24 specifications. Additionally they provide $\pm 15\text{KV}$ ESD protection (IEC61000-4-2 Air Gap and Human Body Model).

All five ports are available on a 50-way dual row 0.1" pitch right angle pin header J7. The pin assignments for J7 are provided in Table 2. J7 also provides other functions, which are described in later sections.

The pin assignments for COM1 to COM4 are arranged to interface with IDC D-type connectors simplifying the assembly of cables.

PIN	NAME	NOTES	PIN	NAME	NOTES
1	DCD1	COM1 RS232 carrier detect input	2	DSR1	COM1 RS232 data set ready input
3	RXD1	COM1 RS232 receive data input	4	RTS1	COM1 RS232 request to send output
5	TXD1	COM1 RS232 transmit data output	6	CTS1	COM1 RS232 clear to send input
7	DTR1	COM1 RS232 data terminal ready output	8	RI1	COM1 RS232 ring indicator input
9	GND	COM1 ground	10	DCD2	COM2 RS232 carrier detect input
11	DSR2	COM2 RS232 data set ready input	12	RXD2	COM2 RS232 receive data input
13	RTS2	COM2 RS232 request to send output	14	TXD2	COM2 RS232 transmit data output
15	CTS2	COM2 RS232 clear to send input	16	DTR2	COM2 RS232 data terminal ready output
17	RI2	COM2 RS232 ring indicator input	18	GND	COM2 ground
19	DCD3	COM3 RS232 carrier detect input	20	DSR3	COM3 RS232 data set ready input
21	RXD3	COM3 RS232 receive data input	22	RTS3	COM3 RS232 request to send output
23	TXD3	COM3 RS232 transmit data output	24	CTS3	COM3 RS232 clear to send input
25	DTR3	COM3 RS232 data terminal ready output	26	RI3	COM3 RS232 ring indicator input
27	GND	COM3 ground	28	GPIO9	General purpose input/output – OS dependant.
29	RES	Do not connect, reserved for DSP Design use.	30	RXD4	COM4 RS232 receive data input
31	RTS4	COM4 RS232 request to send output	32	TXD4	COM4 RS232 transmit data output
33	CTS4	COM4 RS232 clear to send input	34	GND	Ground
35	RESET#	Reset input	36	GND	Ground
37	SDA	I2C Data input/output	38	SCL	I2C Clock output
39	RXD5	COM5 RS232 receive data input	40	TXD5	COM5 RS232 transmit data output
41	RES	Do not connect, reserved for DSP Design use.	42	RES	Do not connect, reserved for DSP Design use.
43	RES	Do not connect, reserved for DSP Design use.	44	RES	Do not connect, reserved for DSP Design use.
45	GND	Ground	46	BATT	Battery Input
47	VCC	+5V Supply	48	VCC	+5V Supply
49	GND	Ground	50	GND	Ground

TABLE 2: XA270 J7 PIN ASSIGNMENTS

2.7.1 COM1, COM2 and COM3

COM1, COM2 and COM3 are standard full function eight-wire RS232 ports.

COM1 is implemented in the Intel® PXA270™ processor. COM2 and COM3 are implemented in a XR16C2550 DUART attached to the PC/104 bus on the XA270.

These ports support, three transmit signals (TXD, RTS and DTR) and five receive signals (RXD, CTS, DCD, DSR and RI).

2.7.2 COM4

COM4 is a four-wire RS232 port implemented in the Intel® PXA270™ processor. The port supports two transmit signals (TXD and RTS) and two receive signals (RXD and CTS).

2.7.3 COM5

COM5 is a two-wire RS232 port implemented in the Intel® PXA270™ processor. The port supports one transmit signal (TXD) and one receive signal (RXD).

2.7.4 Electrical Ratings

All five ports have an absolute maximum input voltage of $\pm 25V$ on any receiver input (RXD, CTS, DCD, DSR and RI) and a minimum output voltage swing of $\pm 5V$ on any transmitter output.

2.8 DISPLAY

The XA270 provides a LCD controller implemented in the Intel® PXA270™ processor, which is capable of driving 16bpp colour LCD panels with resolutions up to 800x600. The parallel TTL interface has been designed to be compatible with a range of interface boards from DSP Design, allowing connection to a variety of common displays. Please refer to Appendix D for a detailed description of each board.

Several TFT panels from different manufacturers have been successfully tested with the XA270. Please refer to the Developer's Guide for the specific operating system for further details.

Due to the unified memory architecture of the Intel® PXA270™ processor, there are bus bandwidth limitations, which will effect display refresh rates at display resolutions above 640x480. Please refer to the Developer's Guide for the specific operating system for further details.

The LCD interface is available on a 40-way dual row 0.05" pitch pin header J2. Table 3 shows the pin assignment for J2.

J2 supports a generic LCD interface used on all DSP Design processor boards, some of which support 24bpp. Bits not used by the XA270 are connected to GND on J2.

PIN	NAME	NOTES	PIN	NAME	NOTES
1	ENBKL	Active high backlight enable signal	2	ENAVDD	Active high LCD power enable signal
3	GND	Ground	4	PCLK	Pixel clock
5	GND	Ground	6	HSYNC	Horizontal sync
7	GND	Ground	8	VSYNC	Vertical sync
9	GND (R0)	Ground	10	GND (R1)	Ground
11	GND (R2)	Ground	12	R3	Data Bit
13	GND	Ground	14	R4	Data Bit
15	R5	Data Bit	16	R6	Data Bit
17	GND	Ground	18	R7	Data Bit
19	-	Reserved. Do not use.	20	-	Reserved. Do not use.
21	GND	Ground	22	G2	Data Bit
23	G3	Data Bit	24	G4	Data Bit
25	VCC3V	3.3V supply	26	G5	Data Bit
27	G6	Data Bit	28	G7	Data Bit
29	VCC3V	3.3V supply	30	GND (B0)	Ground
31	GND (B1)	Ground	32	GND (B2)	Ground
33	VCC/PWM	5V supply or PWM	34	B3	Data Bit
35	B4	Data Bit	36	B5	Data Bit
37	VCC	5V supply	38	B6	Data Bit
39	B7	Data Bit	40	ENAB	Data enable signal

TABLE 3: XA270 J2 PIN ASSIGNMENTS

J2 pin 33 can be configured as either VCC (+5V) or PWM via a two position solder link LK10. In position 1-2, VCC is connected to J2 pin 33. In position 2-3, a GPIO signal PWM is connected to J2 pin 33. The PWM signal is configured as a pulse width modulated output by the operating system providing backlight brightness control. Please refer to the Developer’s Guide for the specific operating system for further details.

2.8.1 Electrical Ratings

The LCD bus has the following characteristics:

- $V_{OH} = 2.7V \text{ min @ } I_{OH} = -3mA.$
- $V_{OL} = 0.3V \text{ max @ } I_{OL} = 3mA.$

2.8.2 LCD Interface Boards

At present DSP Design offers three TFT LCD interface boards, which can be used with the XA270. The TFTIF31, TFTIF41 and TFTIFKYV boards interface to TFT LCDs with conventional parallel interfaces (6 bits of red, green and blue, plus timing signals). Details of the interface boards are provided in Appendix D.

2.9 ETHERNET

The XA270 provides a single IEEE 802.3/802.3u compliant 10/100-Base-T Ethernet port implemented in the LAN91C111 controller with integrated MAC and PHY. The 32-bit controller interfaces to the Intel® PXA270 processor via the shared system bus.

Connection to the Ethernet port is made through a Hirose DF13-8P-1.25H(21) connector J12. The pin assignments for J12 are provided in Table 4.

PIN	NAME	NOTES
1	RX+	Twisted pair receiving data
2	RX-	Twisted pair receiving data
3	VCC/VCC3V	Selects the center tap voltage
4	GND	Ground
5	LINKLED#	Controls LINK status LED in the RJ45 connector
6	LANLED#	Controls LAN activity LED in the RJ45 connector
7	TX-	Twisted pair transmitting data
8	TX+	Twisted pair transmitting data

TABLE 4: XA270 J12 PIN ASSIGNMENTS

The XA270 connects to a network through one of two interface boards available from DSP Design.

- The TP400ET is a small board, which contains the Ethernet RJ45 connector (with integrated magnetics and LEDs), EMC filters and ESD protection. J12 on the XA270 connects to the TP400ET via a short length of CAT-5 twisted pair cable, the TB486ET-CAB. The TP400ET has been designed to be mounted in an enclosure allowing EMC filtering to be optimised. Details of the TP400ET are provided in Appendix E.
- The XACONN is a connector breakout board, which the XA270 plugs into, providing the Ethernet RJ45 connector (with integrated magnetics and LEDs), EMC filters and ESD protection. J12 on the XA270 connects to the XACONN via a short length of CAT-5 twisted pair cable. Details of the XACONN are provided in Appendix G.

ESD protection is not provided on the XA270, but is available on the TP400ET and XACONN.

2.10 USB HOST

The XA270 provides four USB 1.1 compliant host posts available on two Hirose DF13-8P-1.25V connectors J3 and J4. A TUSB2046 USB 1.1 compliant hub expands the single host port available on the Intel® PXA270 processor into four ports.

Each USB port includes a SN75240 transient suppressor, providing ±15KV ESD protection (IEC61000-4-2 Air Gap and Human Body Model).

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Each USB port is powered by a current-limited 5V power supply line. An on-board USB power controller chip limits the current sent to each peripheral at slightly above the 500mA minimum set by the USB specification.

The pin assignments for J3 and J4 are provided in Table 5.

PIN	NAME	NOTES
1	DM1	Port 1 USB negative signal
2	DP1	Port 1 USB positive signal
3	VCC1	Port 1 switched 500mA current limited +5V supply
4	GND1	Port 1 GND
5	VCC2	Port 2 switched 500mA current limited +5V supply
6	GND2	Port 2 GND
7	DM2	Port 2 USB negative signal
8	DP2	Port 2 USB positive signal

TABLE 5: XA270 J3 and J4 PIN ASSIGNMENTS

The XA270 connects to USB peripherals through one of two interface boards available from DSP Design.

- The TP300USB is a small board, which contains two Type-A USB sockets and EMC filters. J3 or J4 on the XA270 connect to the TP300USB via short lengths of CAT-5 twisted pair cable, the TB486ET-CAB. Two TP300USBs will be required to provide a maximum of four ports. The TP300USB has been designed to be mounted in an enclosure allowing EMC filtering to be optimised. Details of the TP300USB are provided in Appendix F.
- The XACONN is a connector breakout board, which the XA270 plugs into, providing two Type-A USB sockets and EMC filters. J3 on the XA270 connects to the XACONN via a short length of CAT-5 twisted pair cable. Details of the XACONN are provided in Appendix G. If two further USB ports are required, a single TP300USB can be connected to J4 on the XA270 as described in the previous section.

2.11 USB CLIENT

The XA270 provides a single USB 1.1 compliant client port implemented in the Intel® PXA270 processor. The pin assignments for the Hirose DF13-8P-1.25H(21) connector J14 are provided in Table 6.

PIN	NAME	NOTES
1	N/C	No connection
2	N/C	No connection
3	N/C	No connection
4	N/C	No connection
5	VBUS	VBUS +5V input
6	GND	GND
7	USBC_N	USB negative signal
8	USBC_P	USB positive signal

TABLE 6: XA270 J14 PIN ASSIGNMENTS

A separate interface board is not available from DSP Design for the USB client port. However, the XACONN connector breakout board, which the XA270 plugs into, provides a single Mini-AB USB socket. J14 on the XA270 connects to the XACONN via a short length of CAT-5 twisted pair cable. Details of the XACONN are provided in Appendix G.

2.12 AUDIO

The XA270 provides a UCB1400 Audio codec connected to the Intel® PXA270 AC97 interface. The UCB1400 provides mono microphone input and stereo line output.

An LM4811 headphone amplifier is connected to the stereo line output to provide a stereo headphone output.

The pin assignments for the 8-way Molex 53261-0871 connector J11 are provided in Table 7.

PIN	NAME	NOTES
1	HPL	Left headphone output
2	HPR	Right headphone output
3	AGND	Analog ground
4	MICGND	Microphone return
5	MIC	Microphone input with bias applied
6	AGND	Analog ground
7	LINEOUTL	Left line output
8	LINEOUTR	Right line output

TABLE 7: XA270 J11 PIN ASSIGNMENTS

The XA270 supports both self-powered and unpowered active microphones. Both types of microphone connect between MIC and MICGND. Unpowered active

microphones require a bias voltage on MIC, which is provided by the XA270 when LK12 is fitted. Self-powered active microphones containing an internal battery do not require a bias voltage and therefore LK12 should not be fitted.

The XACONN provides three colour coded 3.5mm audio jacks for microphone, headphones and line out. J11 on the XA270 connects to the XACONN via a short length of cable. Details of the XACONN are provided in Appendix G.

2.12.1 Electrical Ratings

The UCB1400 provides a typical microphone input voltage of 1V rms and a typical line output of 1V rms into a 10K Ω load.

The LM4811 headphone amplifier provides a typical output power of 40mW into a 16 Ω load and 28mW into a 32 Ω load.

2.13 TOUCH-SCREEN

The XA270 provides a four-wire resistive touch-screen interface implemented in the UCB1400 AC97 codec.

Several touchscreens from different manufacturers have been successfully tested with the XA270. Please refer to the Developer's Guide for the specific operating system for further details.

The pin assignments for the 9-way Molex 53261-0971 connector J13 are provided in Table 8.

PIN	NAME	NOTES
1	AD0	ADC channel 0
2	AD1	ADC channel 1
3	AGND	Analog ground
4	TSPX	Touchscreen top contact
5	TSPY	Touchscreen right contact
6	VCC3V	+3.3V Supply
7	AGND	Analog ground
8	TSMX	Touchscreen bottom contact
9	TSMY	Touchscreen left contact

TABLE 8: XA270 J13 PIN ASSIGNMENTS

The touchscreen sampling rate and calibration are a function of the operating system. Please refer to the Developer's Guide for the specific operating system for further details.

2.14 ANALOG TO DIGITAL CONVERTER

The XA270 provides a two channel, 10-bit successive approximation analog to digital converter (ADC) with internal track-and-hold circuit and analog multiplexer allowing

external analog signals to be monitored. The ADC is implemented in the UCB1400 AC97 codec.

The signals are available on a 9-way Molex connector shared with the touch-screen. Please refer to Table 7 for the pin assignments.

The ADC sampling rate is a function of the operating system. Please refer to the Developer's Guide for the specific operating system for further details.

2.14.1 Electrical Ratings

The ADC inputs provide a typical full-scale range of 7.5V and a typical input impedance of 77K Ω .

2.15 I²C EXPANSION

The XA270 provides a two pin serial Inter-Integrated Circuit (I²C) expansion bus available on the 50-way pin header J7. The I²C bus controller is implemented in the Intel® PXA270 processor and is compliant with the I²C Bus Specification Version 2.0, supporting both standard-speed and fast-mode operation. The I²C bus interfaces to a large range of simple data acquisition/control devices available from a number of manufacturers.

A circuit is provided on the XACONN to demonstrate expansion capabilities using the I²C bus and is mainly intended for use as part of the LaunchPad. Example code is provided as part of the LaunchPad. Please refer to Appendix G and the Developer's Guide for the specific operating system for further details.

The pin assignments for J7 are provided in Table2. SDA and SCL are both pulled high on the XA270 by 1K5 resistors.

2.15.1 Electrical Ratings

The I²C bus has an absolute maximum input voltage of +4V (ie they are not 5V tolerant), beyond which damage to the XA270 may result.

The I²C bus has the following characteristics:

- $V_{IH} = 2.4V$ min.
- $V_{IL} = 0.6V$ max.
- $V_{OH} = 2.7V$ min @ $I_{OH} = -3mA$.
- $V_{OL} = 0.3V$ max @ $I_{OL} = 3mA$.

2.16 PC/104 EXPANSION

2.16.1 Overview

The XA270 provides a 16-bit PC/104 interface on connector J1. Refer to Table 9 for the pin definition of this connector, which is compliant with the PC/104 Specification.

The PC/104 bus is the same from an electrical and timing point of view as the ISA bus found in PC computers. However, it is mechanically different, using a stacking connector instead of the gold-plated edge connector used in PCs. Add-on PC/104 boards may be stacked with the XA270 to provide additional functionality.

The XA270 PC/104 interface drives signals at 3.3V levels. The interface is however 5V tolerant, and can therefore be used with PC/104 add-on cards that use either 3.3V or 5V signal levels.

The XA270 PC/104 bus is derived from the Intel® PXA270 PC Card Interface. The PC/104 memory space is mapped onto the PC Card socket 1 common memory space, and the PC/104 I/O space is mapped onto the PC Card socket 1 I/O space. As a result, some PC/104 signals and features can't be supported. These limitations are detailed in Section 2.13.8.

The register set of the Intel® PXA270 Memory Controller allows the PC Card interface signals to be configured to provide an ISA compatible interface. The I/O and memory cycles for the XA270 PC/104 bus are provided in the following sections.

2.16.2 PC/104 Bus I/O Cycles

Figures 4 and 5 show 8-bit and 16-bit I/O cycles respectively.

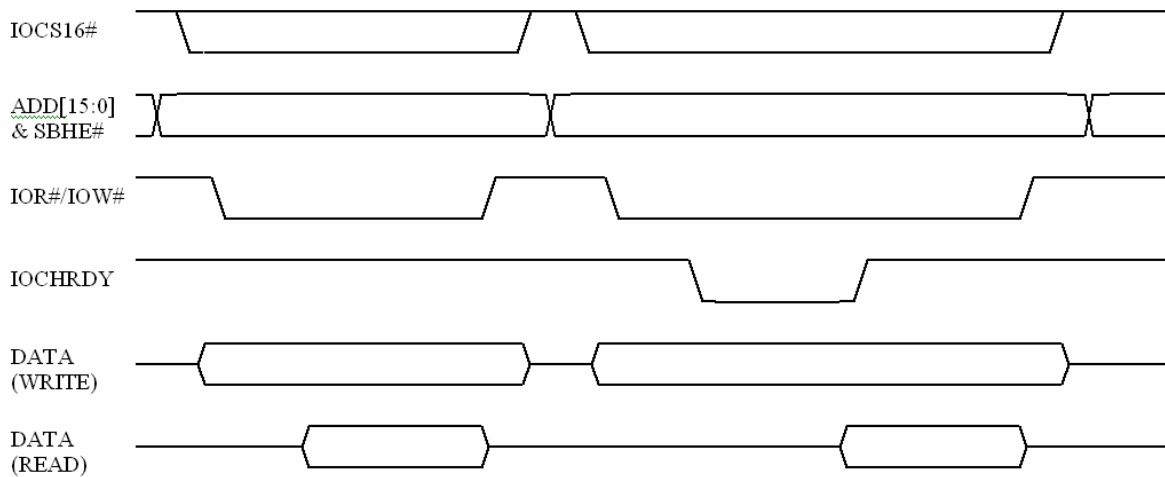


FIGURE 4: PC/104 8-BIT I/O CYCLE

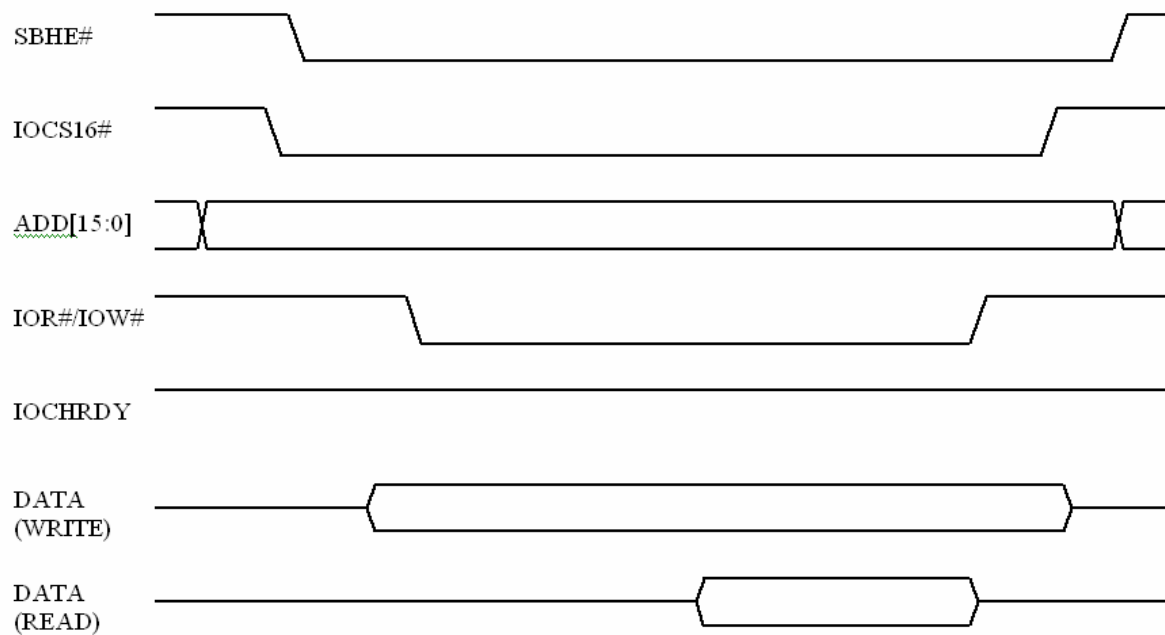


FIGURE 5: PC/104 16-BIT I/O CYCLE

2.16.3 PC/104 Bus Memory Cycles

Figure 6 shows memory cycles on the PC/104 bus. The cycles are the same for both 8-bit and 16-bit accesses as the MEMCS16# signal is not supported by the XA270. Users must be aware of the data width of any memory device accessed on the ISA bus, and must issue 8-bit or 16-bit memory accesses as appropriate to avoid invalid data.

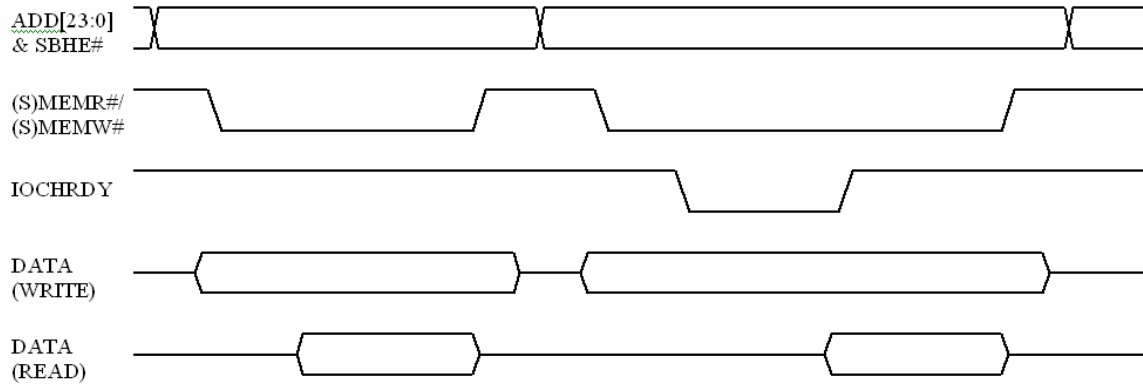


FIGURE 6: PC/104 8/16-BIT MEMORY ACCESS TIMING

2.16.4 PC/104 Expansion Connector

PIN	J1 ROW D	J1 ROW C
0	GND	GND
1	MEMCS16# ⁽²⁾	SBHE#
2	IOCS16#	LA23
3	IRQ10	LA22
4	IRQ11	LA21
5	IRQ12	LA20
6	IRQ15 ⁽¹⁾	LA19
7	IRQ14	LA18
8	DACK0# ⁽⁴⁾	LA17
9	DRQ0 ⁽¹⁾	MEMR#
10	DACK5# ⁽⁴⁾	MEMW#
11	DRQ5 ⁽¹⁾	SD8
12	DACK6# ⁽⁴⁾	SD9
13	DRQ6 ⁽¹⁾	SD10
14	DACK7# ⁽⁴⁾	SD11
15	DRQ7 ⁽¹⁾	SD12
16	+5V	SD13
17	MASTER# ⁽²⁾	SD14
18	GND	SD15
19	GND	KEY ⁽⁶⁾

PIN	J1 ROW A	J1 ROW B
1	IOCHK# ⁽²⁾	GND
2	SD7	RESET
3	SD6	+5V
4	SD5	IRQ9 ⁽¹⁾
5	SD4	-5V ⁽³⁾
6	SD3	DRQ2 ⁽¹⁾
7	SD2	-12V ⁽³⁾
8	SD1	SRDY# ⁽²⁾
9	SD0	+12V ⁽³⁾
10	IOCHRDY	KEY ⁽⁶⁾
11	AEN ⁽⁵⁾	SMEMW#
12	SA19	SMEMR#
13	SA18	IOW#
14	SA17	IOR#
15	SA16	DACK3# ⁽⁴⁾
16	SA15	DRQ3 ⁽¹⁾
17	SA14	DACK1# ⁽⁴⁾
18	SA13	DRQ1 ⁽¹⁾
19	SA12	REFRESH# ⁽²⁾
20	SA11	BCLK ⁽⁵⁾
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5 ⁽¹⁾
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2# ⁽⁴⁾
27	SA4	TC ⁽⁵⁾
28	SA3	BALE ⁽⁴⁾
29	SA2	+5V
30	SA1	OSC ⁽⁵⁾
31	SA0	GND
32	GND	GND

Notes:

- (1) These inputs are not supported and are n/c on the XA270.
- (2) These signals are not supported but are pulled up to 3.3V on the XA270.
- (3) These power supply pins are not used and are n/c on the XA270.
- (4) These outputs are not supported and are tied to 3.3V on the XA270.
- (5) These outputs are not supported and are tied to GND on the XA270.
- (6) These pins are plugged to prevent incorrect insertion of peripheral cards.

TABLE 9: XA270 J1 PIN ASSIGNMENTS

2.16.5 PC/104 Interrupts

Eight of the PC/104 interrupts are supported by the XA270 for use by PC/104 expansion cards. The interrupt lines are buffered with 5V tolerant non-inverting buffers before being connected to Intel® PXA270 GPIO lines. The eight supported interrupt lines along with the GPIO allocation are provided in Table 9.

PC/104 Interrupt	PXA270 GPIO Allocation
IRQ3	GPIO 22
IRQ4	GPIO 23
IRQ6	GPIO 25
IRQ7	GPIO 26
IRQ10	GPIO 32
IRQ11	GPIO 52
IRQ12	GPIO 84
IRQ14	GPIO 114

TABLE 10: SUPPORTED PC/104 INTERRUPTS AND GPIO ALLOCATION

Note that IRQ5 and IRQ9 are not available for use by PC/104 expansion cards, as these are allocated to the onboard DUART on the PC/104 bus, which provides COM2 and COM3.

The Intel® PXA270 GPIO controller can be configured to generate an interrupt on either a rising or falling edge (or both) of each of these GPIO lines. The actual implementation of the active edge for each GPIO line is operating system dependent. Please refer to the Developer’s Guide for the specific operating system for further details.

2.16.6 PC/104 Pull Up Resistors

Table 11 details the value of the pull-up resistors included on the XA270. All pull-ups are to 3.3V.

PC/104 Signal	Pull-Up Value (Ohms)
All IRQ Interrupt Lines	2K2
All SD Data Lines	10K
IOCHRDY	1K
IOCS16#	330R
IOCHK# ⁽¹⁾	4K7
MASTER# ⁽¹⁾	300R
MEMCS16# ⁽¹⁾	300R
SRDY# ⁽¹⁾	300R
REFRESH# ⁽¹⁾	4K7

Notes: (1) These signals are pulled up but not functionally used by the XA270.

TABLE 11: PC/104 PULL UP RESISTORS

2.16.7 PC/104 Expansion Bus Power and Reset

The XA270 provides power (+5V) to the PC/104 bus, but cannot be powered from the PC/104 bus. **Powering the XA270 from the PC/104 bus may result in damage to the XA270.**

Add-on cards must power down when the +5V supply is removed from the bus by the XA270. This is to prevent damage to onboard components which are only 5V tolerant when powered up by the onboard 3.3V supply. The XA270 implements power sequencing to ensure that the onboard 3.3V supply comes up before the +5V supply is applied to the PC/104 bus.

Some of the PC/104 signals are pulled up to the 3.3V supply and are driven before the +5V supply is applied to the PC/104 bus. This will result in the PC/104 signals self-powering a PC/104 card until the +5V supply is applied to the PC/104 bus.

The XA270 drives the PC/104 RESET signal to reset the PC/104 bus, but cannot be driven by the PC/104 RESET signal. The XA270 is therefore a reset master only. The PC/104 RESET signal is inverted from the main board reset signal driven by the processor to reset the onboard peripherals.

2.16.8 Unsupported PC/104 Features and Signals

The following features and associated signals are not supported by the XA270 PC/104 bus:

- (1) DMA is not supported. Hence the AEN# and TC# outputs are tied to GND, all DACK# outputs are tied to 3.3V and all DRQ inputs are not connected on the XA270.
- (2) Bus arbitration is not supported. The XA270 is always the bus master and does not support add-on bus owner cards. The MASTER# signal is pulled up to 3.3V via a 300R resistor on the XA270, but is not functionally used.
- (3) BALE address latching is not supported. BALE is tied to 3.3V on the XA270 and the address remains valid throughout the entire bus cycle.
- (4) Interrupts IRQ5 and IRQ9 are not available for use by PC/104 expansion cards. These interrupts are already allocated to the DUART on the PC/104 bus, which provides COM2 and COM3.
- (5) Interrupt IRQ15 is not supported. This signal is a no-connect on the XA270.
- (6) I/O Channel Check is not supported. IOCHK# is a no-connect on the XA270.
- (7) Zero wait state transfers are not supported. The SRDY# (NOWS#) signal is a no-connect on the XA270.
- (8) Only asynchronous bus cycles are supported. The BCLK and OSC clock signals are tied to GND on XA270.
- (9) Refresh cycles are not supported. The REFRESH# signal is pulled up to 3.3V via a 4K7 resistor on the XA270, but is not functionally used.

- (10) MEMCS16# functionality is not supported. Hence any 16-bit transfers to or from memory devices will not be automatically split up into two 8-bit accesses by the Intel® PXA270 PC Card Controller. Users must be aware of the data width of any memory device accessed on the ISA bus, and must issue 8 or 16 bit memory accesses as appropriate to avoid invalid data.

2.16.9 Electrical Ratings

All PC/104 inputs have an absolute maximum input voltage of 5.5V (ie they are 5V tolerant), although PC/104 inputs must not be driven when power is removed from the PC/104 bus, otherwise damage to the XA270 may result.

The PC/104 bus has the following characteristics:

- $V_{IH} = 2.0V$ min.
- $V_{IL} = 0.8V$ max.
- $V_{OH} = 2.4V$ min @ $I_{OH} = -8mA$.
- $V_{OL} = 0.4V$ max @ $I_{OL} = 8mA$.

2.17 REAL TIME CLOCK

The XA270 provides two real time clocks, one inside the Intel® PXA270 and another in a Dallas device connected to the I²C bus. Both RTCs have an accuracy better than 2 seconds a day.

The Intel® PXA270 RTC maintains time and date during normal operation and sleep, but is not battery backed and will therefore lose its contents when +5V is removed from the XA270.

The Dallas DS1338U RTC can be connected to an external Lithium battery via the 50-way pin header J7 to maintain time and date under all power conditions. The battery voltage should be maintained between 1.3V to 3.7V. Exceeding the maximum voltage may cause damage to the RTC and result in unpredictable behavior.

The Dallas DS1338U has a slave address of 68h.

The operation of the RTCs is operating system dependant. Please refer to the Developer's Guide for the specific operating system for further details.

2.18 USER IO

2.18.1 System GPIO

The Intel® PXA270 processor GPIO block provides 120 general purpose IO signals, the majority of which are reserved for controlling dedicated functions internal to the XA270. A number of signals are available for interfacing to external customer circuits.

User GPIO

Sixteen General Purpose I/O signals are available on a 20-way 2mm pitch pin header J8. The pin assignments for J8 are provided in Table 12. Please refer to the Developer's Guide for the specific operating system for further details.

Pin Number	Name	Pull-up/down	Pin Number	Name	Pull-up/down
1	GND	-	2	+3V3	-
3	GPIO93	100K P.D	4	GPIO94	100K P.D
5	GPIO95	100K P.D	6	GPIO99	100K P.D
7	GPIO98	100K P.D	8	GPIO97	100K P.D
9	GPIO102	100K P.D	10	GPIO101	100K P.D
11	GPIO100	100K P.D	12	GPIO96	-
13	GPIO108	-	14	GPIO107	-
15	GPIO106	-	16	GPIO105	-
17	GPIO104	-	18	GPIO103	-
19	+3V3		20	GND	-

TABLE 12: XA270 J8 PIN ASSIGNMENTS

The Intel PXA270 processor sometimes generates a high glitch of less than 20ns on these GPIO signals when coming out of reset. This means that any GPIO configured by the operating system as an output with a default low state may glitch to the 'active' high state following a reset, potentially causing the connected device to register a false transition on its input. The glitch occurs approximately 80ns after a power on reset, and is documented in errata E82 of the PXA27x Processor Family Specification Update dated July 2006. If external logic is sensitive to a glitch on a GPIO signal configured as an output, an external filter circuit must be implemented.

2.18.2 Power Management GPIO

The XA270 provides a single input signal GPIO9 on the 50-way general-purpose connector J7. The signal is typically used as an active low wake from sleep interrupt, although this is operating system dependent. Please refer to the Developer's Guide for the specific operating system for further details.

2.18.3 DIP Switches

The XA270 provides an 8-way DIP switch connected to the Intel® PXA270 processor GPIO block. The switch positions are read during power up to configure the operating system. Please refer to the Developer's Guide for the specific operating system for further details.

2.18.4 Electrical Ratings

The GPIO signals have an absolute maximum input voltage of +4V (ie they are not 5V tolerant), beyond which damage to the XA270 may result.

The GPIO signals have the following characteristics:

- $V_{IH} = 2.4V$ min.
- $V_{IL} = 0.6V$ max.
- $V_{OH} = 2.7V$ min @ $I_{OH} = -3mA$.
- $V_{OL} = 0.3V$ max @ $I_{OL} = 3mA$.

2.19 POWER

The XA270 operates from a single +5V input, generating all other supplies internally. Power can be applied to the XA270 by either a 4-way power connector J10 or a 50-way general purpose pin header J7. Table 13 provides the pin assignments for J10.

Pin Number	Name
1	GND
2	GND
3	+5V
4	+5V

TABLE 13: XA270 J10 PIN ASSIGNMENTS

2.19.1 Electrical Ratings

The XA270 operates over an input range of +4.75V to +5.25V. Voltages above +5.25V may result in damage to the XA270. Voltages below +4.75V may result in unpredictable behavior.

The XA270 provides power to PC/104 bus under operating system control. **Powering the XA270 from the PC/104 bus may result in damage to the XA270.**

2.20 RESET

The XA270 can be reset by applying a low going pulse to the RESET# input on connector J7. In this way a system reset can be generated by an external IC or switch.

RESET# is an input to the power management IC. The power management IC generates power-on reset to the processor, which in turn asserts the main board reset to all other peripherals during the power-up sequence and hardware reset events under operating system control.

2.21 SOLDER LINKS

Unless otherwise described in previous sections, solder links are configured by DSP Design for test purposes and must remain unchanged. Failure to do so may result in unpredictable behavior.

2.22 MISCELLANEOUS CONNECTORS

Two 8-way pin headers J5 and J9 are provided for JTAG support for the Intel® PXA270 and Xilinx CPLD, and are therefore reserved for manufacturing use by DSP Design only.

APPENDIX A: SPECIFICATION

This is the specification for the XA270 highly integrated low power single board computer in a PC/104 form factor.

A.1 PROCESSOR

The XA270 uses the Intel® PXA270 Xscale processor clocked at up to 520MHz.

A.2 DRAM

The XA270 provides 128Mbytes SDRAM soldered directly to the PCB.

A.3 SRAM

The XA270 provides 256 Kilobytes SRAM internal to the Intel® PXA270 processor.

A.4 FLASH

The XA270 provides 64Mbytes Spansion Mirror-Bit Flash soldered directly to the PCB.

A.5 LCD

The LCD controller is integral to the Intel® PXA270, driving TFT LCDs up to 800x600 and 16-bit colour. LCDs can be connected through a 40-way ribbon cable. The interface includes control signals to turn on and off power to the LCD and backlight inverter.

A.6 TOUCHSCREEN

The XA270 provides a 4 wire resistive touchscreen interface.

A.7 USB HOST

The XA270 provides four USB v1.1 host ports available on two DF13 board to wire connectors on the board edge. On-board power switches provide 500mA continuous current per port and short circuit protection. USB peripherals can be connected via the TP300USB or XACONN.

A.8 USB CLIENT

The XA270 provides a single USB client port which is available on a DF13 board to wire connector on the board edge.

A.9 SERIAL PORTS

The XA270 provides five serial ports on a 50-way general purpose pin header. COM1, COM2 and COM3 are full function RS232 ports with 3 output signals and 5 input signals. COM4 is RS232 RX/TX/RTS/CTS only and COM5 is RS232 RX/TX only.

A.10 COMPACT FLASH

The XA270 provides a single 3.3V Compact Flash socket on the board edge which can accept Compact Flash memory and I/O cards.

A.11 ETHERNET

A 10/100Base-T Ethernet port is provided on a DF13 board to wire connector on the board edge. The port can connect to a local area network via the TP400ET or XACONN.

A.12 AUDIO

The XA270 provides an AC97 audio subsystem supporting microphone in, stereo line out and stereo headphone out.

A.13 ADC

The XA270 provides two 10-bit ADC inputs with 0V to +7.5V input range.

A.14 PC/104 EXPANSION

The XA270 provides a 16-bit PC/104 (ISA) interface on a standard PC/104 connector.

A.15 I²C EXPANSION

The XA270 provides a single I²C interface for connecting to data acquisition/control devices.

A.16 USER I/O

The XA270 provides sixteen signals, which are configured as either general-purpose I/O.

A.17 DIP SWITCHES

The XA270 provides eight switches for configuring the operating system during power on.

A.18 REAL TIME CLOCK

The XA270 provides two RTC's, one of which supports an input for an external backup battery to maintain time and date during power off and low power modes. Accuracy is better than 2 sec/day.

A.19 RESET CIRCUIT

The Power Management IC (PMIC) provides power-on reset and an input to allow an external switch or signal to reset the XA270.

A.20 DIMENSIONS

PCB dimensions 90.2mm x 95.9mm (3.55 inches x 3.775 inches).

PCB thickness 1.6mm (1/16 inch).

Maximum component height above the PCB 7.5mm.

Maximum component height below the PCB 3.7mm (except for the PC/104 connector which is 10.5mm).

A.21 WEIGHT

73g.

A.22 POWER SUPPLY

Single +5V +/- 5%. Typical power consumption figures without power management for the XA270 are between 2W and 4W under Windows CE 5.0, and vary depending on activity. These do not include figures for a LCD or other peripherals.

A.23 OPERATING TEMPERATURE RANGE

0 – 70 degrees Celsius.

A.24 HUMIDITY

10% - 90% non-condensing.

APPENDIX B: XA270 DRAWINGS

This appendix provides component placement diagrams and mechanical drawings for the XA270.

B.1 COMPONENT PLACEMENT

Figures B1 and B2 show the component placement for the top and bottom sides of the XA270 respectively. A high resolution PDF is available on the DSP Design website.

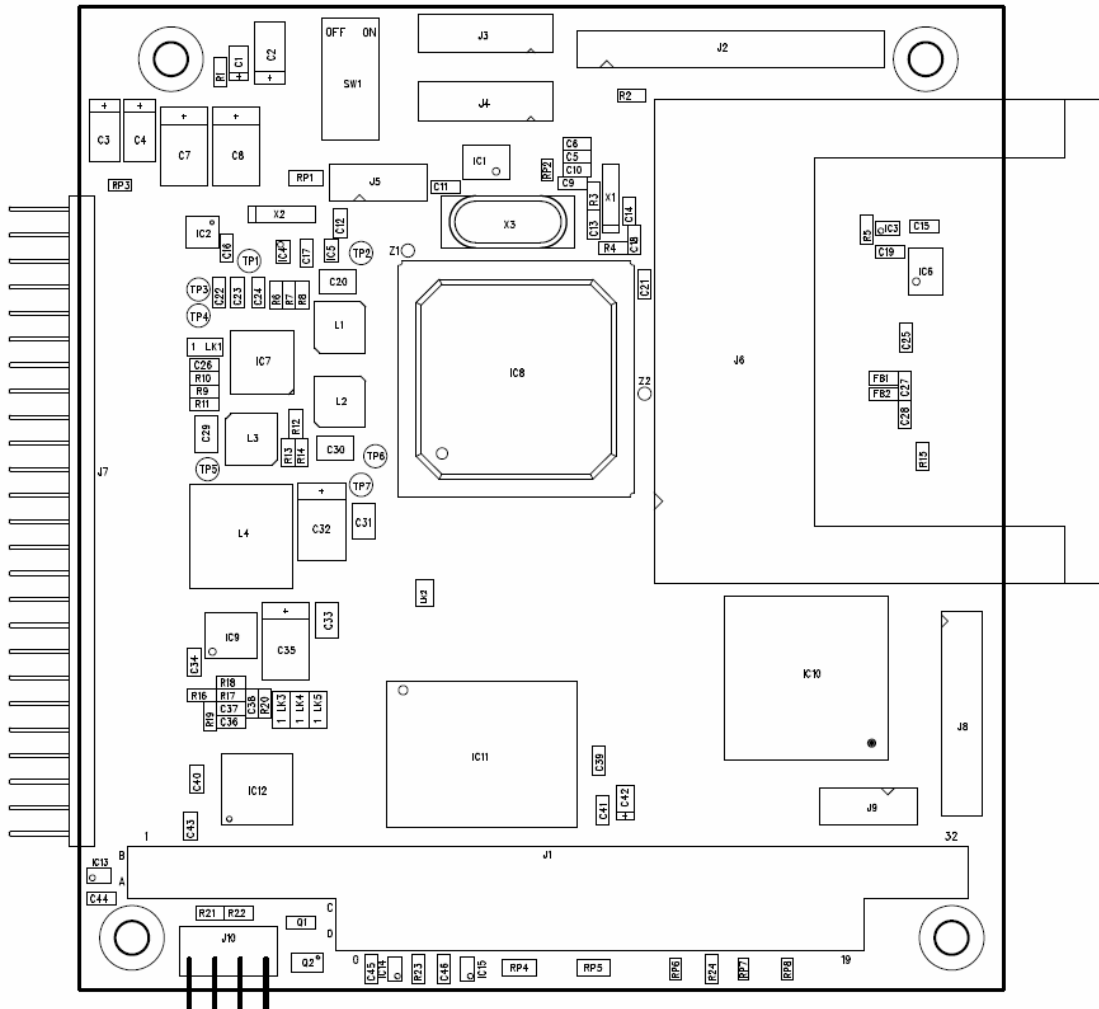


FIGURE B1: XA270 COMPONENT PLACEMENT DIAGRAM – TOP SIDE

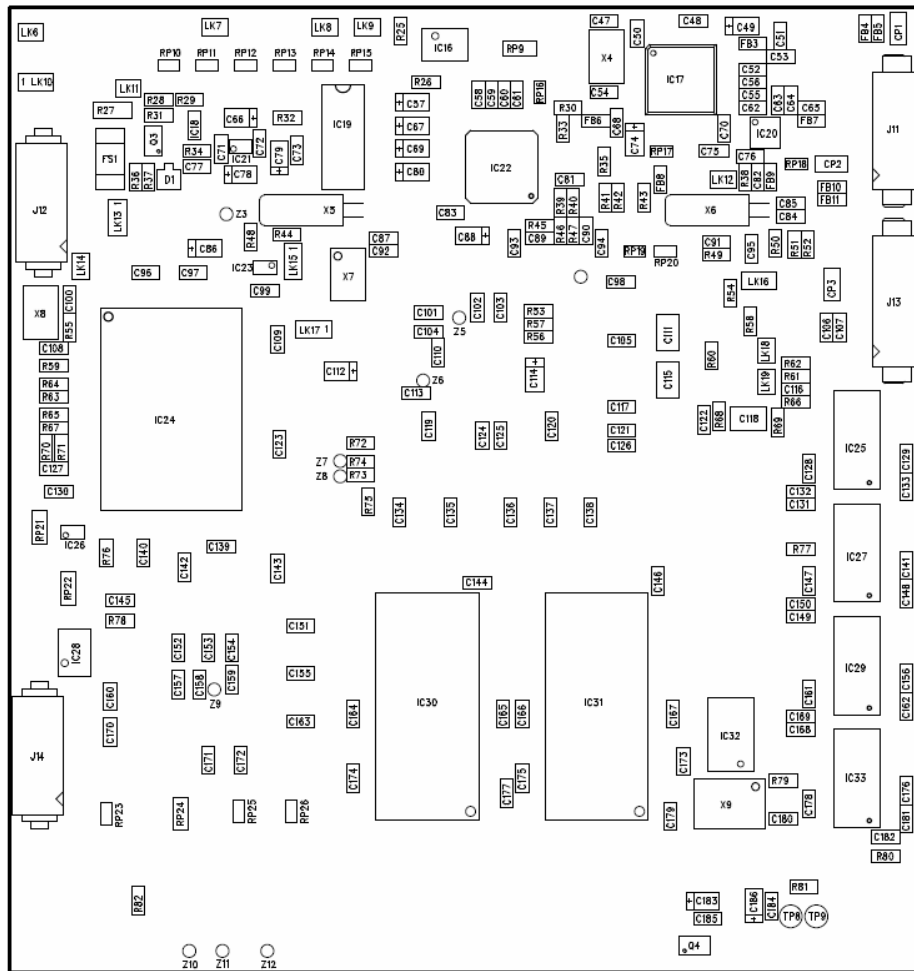
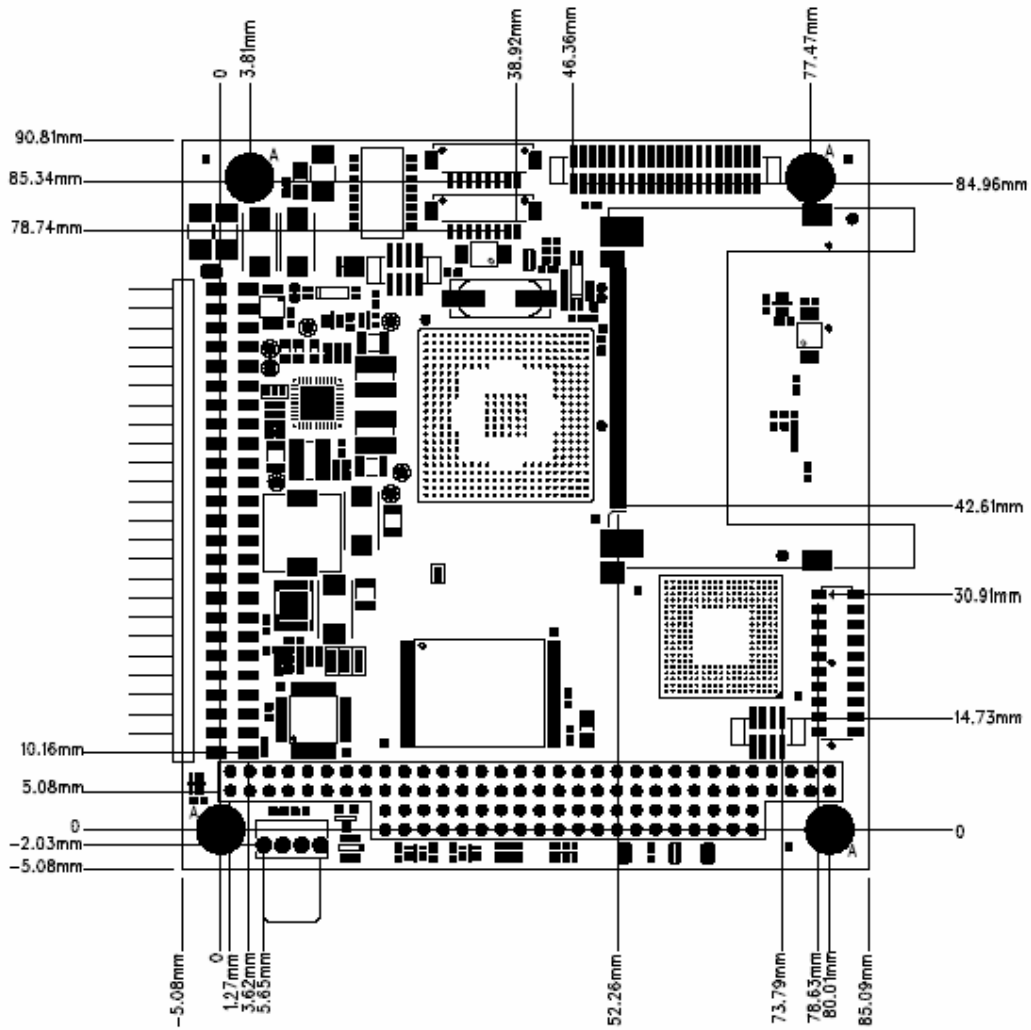


FIGURE B2: XA270 COMPONENT PLACEMENT DIAGRAM – BOTTOM SIDE

B.2 MECHANICAL DIMENSIONS

Figures B3 and B4 show the position and size of mounting holes, and the position of pin 1 for each connector on the XA270. A high resolution PDF is available on the DSP Design website.



NOTES:-

- 1) 4 OFF "A" HOLES - 3.2mm DIAMETER

FIGURE B3: XA270 MECHANICAL DIMENSIONS – TOP SIDE

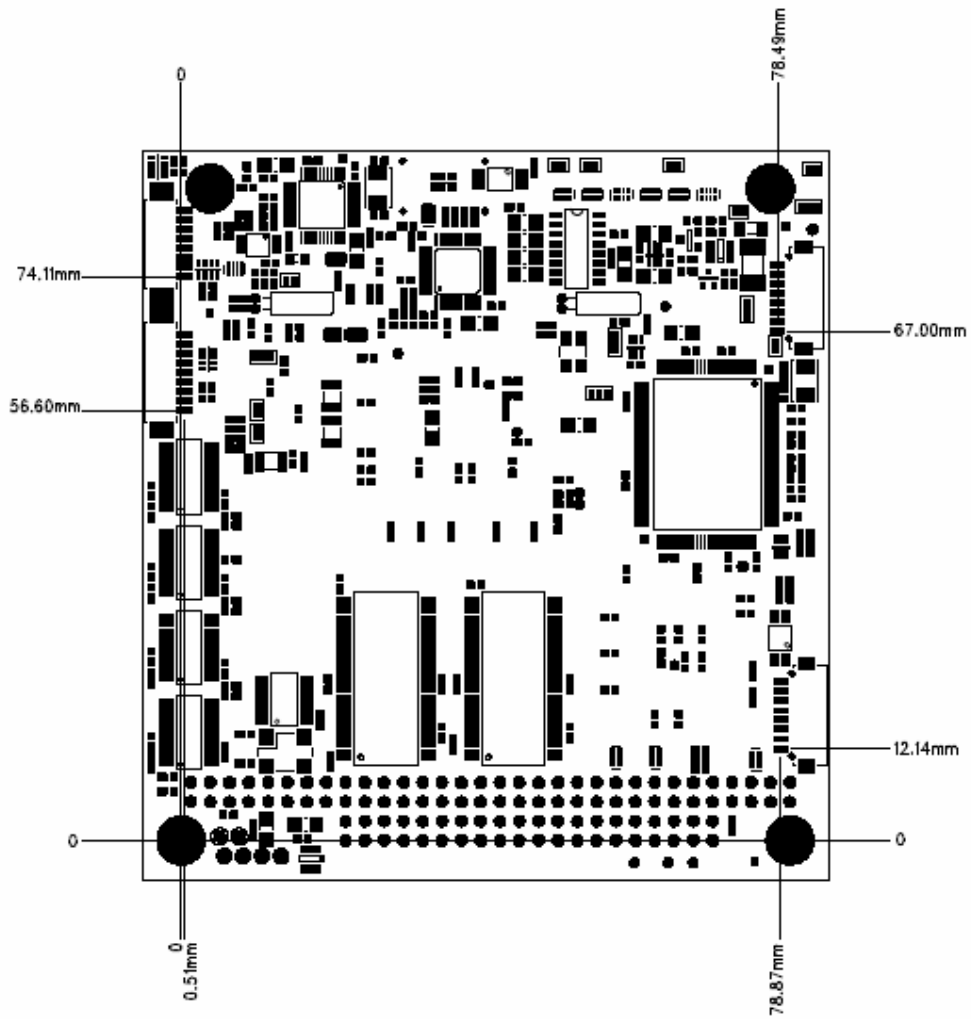


FIGURE B4: XA270 MECHANICAL DIMENSIONS

APPENDIX C: OPTIONS AND ORDERING INFORMATION

This appendix lists the range of products available from DSP Design related to the XA270. Order codes prefixed with **DSP-** indicate the items are RoHS compliant.

C.1 PROCESSOR MODULES

Table C1 contains the order codes for the XA270 processor.

ITEM	DESCRIPTION
DSP-XA270CE	XA270 processor module with Windows CE 5.0

TABLE C1: PROCESSOR MODULES

C.2 LAUNCHPAD APPLICATION DEVELOPMENT KITS

Table C2 contains the order codes for the LaunchPad Application Development Kits for the XA270.

ITEM	DESCRIPTION
DSP-LP270CE	Windows CE 5.0 LaunchPad Application Development Kit.

TABLE C2: LAUNCHPAD APPLICATION DEVELOPMENT KITS

C.3 DISPLAY ACCESSORIES

Table C3 contains the order codes for the cables and display interface boards for the XA270.

ITEM	DESCRIPTION
DSP-TFTIF-CAB7	40 way cable assembly for DSP-TFTIF31, DSP-TFTIF41 and DSP-TFTIFKYV boards, connectors at both ends, length 7 inches
DSP-TFTIF-CAB11	40 way cable assembly for DSP-TFTIF31, DSP-TFTIF41 and DSP-TFTIFKYV boards, connectors at both ends, length 11 inches
DSP-TFTIF31	Display interface adapter. Connects 40-way ribbon cable to LCDs which use the 31-pin Hirose DF9 connector.
DSP-TFTIF41	Display interface adapter. Connects 40-way ribbon cable to LCDs which use the 41-pin Hirose DF9 connector.
DSP-TFTIFKYV	Display interface adapter. Connects 40-way ribbon cable to Kyocera LCDs.
TRM-TFTIFKYV	Printed and bound Technical Reference Manual for the TFTIFKYV.
DSP-TFTKYV75	A Kyocera V-series 640 X 480 7.5" TFT display.
DSP-TFTKYV75-KIT	A display kit, comprising the TFTKYV75, TFTIFKYV, backlight inverter and cables.
DSP-AAVGA	Display interface adapter for VGA CRTs. Connects 40-way ribbon cable to a video D/A converter and 15-pin D-type connector.

TABLE C3: DISPLAY ACCESSORIES

C.4 OTHER ACCESSORIES

Table C4 contains the order codes for miscellaneous accessories for the XA270.

ITEM	DESCRIPTION
DSP-TCONN-PSU	PSU for the XACONN.
DSP-XACONN	Connector breakout board for the XA270. Includes all the cables to interface with the XA270.
TRM-XA270	Printed and bound Technical Reference Manual (this manual).
DSP-TP300USB	Adapter board containing two Type A USB connectors
DSP-TP400ET	Adapter board containing an RJ45 Ethernet connector.
DSP-TB486ET-CAB	Cable assembly for TP300USB and TP400ET.
DSP-CFSSxx	Compact Flash cards. These are available in a number of sizes. Contact DSP Design for details.

TABLE C4: OTHER ACCESSORIES

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APPENDIX D: TFTIF LCD INTERFACE BOARDS

D.1 TFTIF31

The TFTIF31 is designed to interface with a number of TFT LCDs, from Sharp and other manufacturers that use a 31-way Hirose DF9 connector. This section describes the TFTIF31, listing the display pin assignments and the solder link settings.

D.1.1 31-pin Connector Pin Assignments

Table D1 shows the pin assignments for the TFTIF31 display connector.

PIN	LCD SIGNAL	PIN	LCD SIGNAL
1	GND	2	PCLK
3	HSYNC	4	VSYNC
5	GND	6	GND (R2)
7	R3	8	R4
9	R5	10	R6
11	R7	12	GND
13	G2	14	G3
15	G4	16	G5
17	G6	18	G7
19	GND	20	GND (B2)
21	B3	22	B4
23	B5	24	B6
25	B7	26	GND
27	ENAB	28	LCDVCC
29	LCDVCC	30	LEFT/RIGHT
31	UP/DOWN	-	-

TABLE D1: TFTIF31 DISPLAY PIN ASSIGNMENTS

D.1.2 Power Supply Selection: LK1

The TFTIF31 accepts +3.3V and +5V from the XA270 and passes it on to the LCD, to power its electronics (though not the backlight inverter). The power supply voltage is selected by solder link LK1. The selected voltage is then routed to a transistor switch, which turns on the power to the LCD (LCDVCC) under control of the XA270 ENAVDD signal. LK1 can be set to one of two positions. The position marked "5" is for 5V LCDs. The position marked "3.3" is for 3.3V LCDs. You may need to change the solder link to match your display.

D.1.3 Pin 30 and 31 Configuration: LK2 and LK3

LK2 and LK3 are connected to the 31-way connector pins 30 and 31 respectively. The links can be used to change the display orientation, at least on some Sharp displays. For a normal image both should be left open, or linked in the 2-3 position. For an upside-down image both should be linked in the 1-2 position. Some other

LCDs use pins 30 and 31 for other purposes, such as additional power supply pins. LK2 and LK3 should therefore be linked to match the requirement of each display.

Table D2 shows the connections of the LK2 and LK3 pins, thus allowing suitable connections to be made.

LK2 PIN	LK2 CONNECTION	LK3 PIN	LK3 CONNECTION
1	GND	1	GND
2	PIN 30	2	PIN 31
3	LCDVCC	3	LCDVCC

TABLE D2: TFTIF31 PIN 30 AND PIN 31 CONNECTIONS

LCDVCC is the LCD display voltage selected by LK1, as described in the previous section.

D.1.4 Backlight Enable Signal

The XA270 generates a logic-level signal intended to turn on and off the backlight inverter. This signal is called ENBKL, and is 0V for “off” and +3.3V for “on”. The ENBKL signal can be taken to a backlight inverter from the TFTIF31 connector J3. J3 is a Molex 53261-0390 connector. Pin assignments are given in Table D3. Note that some backlight inverters specify a 5V signal to turn on the backlight, so ENBKL may not work with all inverters.

J3 PIN	SIGNAL
1	VCC (+5V)
2	ENBKL
3	GND

TABLE D3: TFTIF31 J3 PIN ASSIGNMENTS

D.2 TFTIF41

The TFTIF41 is designed to interface with a small number of TFT LCDs, principally from Sharp, that use a 41-way Hirose DF9 connector. This section describes the TFTIF41, listing the display pin assignments and the solder link settings.

D.2.1 41-pin Connector Pin Assignments

Table D4 shows the pin assignments for the TFTIF41 display connector.

PIN	LCD SIGNAL	PIN	LCD SIGNAL
1	GND	2	SHFCLK
3	GND	4	HSYNC
5	VSYNC	6	GND
7	GND	8	GND
9	GND (R2)	10	R3
11	R4	12	GND
13	R5	14	R6
15	R7	16	GND
17	GND	18	GND
19	G2	20	G3
21	G4	22	GND
23	G5	24	G6
25	G7	26	GND
27	GND	28	GND
29	GND (B2)	30	B3
31	B4	32	GND
33	B5	34	B6
35	B7	36	GND
37	ENABLE	38	LEFT/RIGHT
39	LCDVCC	40	LCDVCC
41	UP/DOWN	-	-

TABLE D4: TFTIF41 DISPLAY PIN ASSIGNMENTS

D.2.2 Power Supply Selection: LK1

The TFTIF41 accepts +3.3V and +5V from the XA270 and passes it on to the LCD, to power its electronics (though not the backlight inverter). The power supply voltage is selected by solder link LK1. The selected voltage is then routed to a transistor switch, which turns on the power to the LCD (LCDVCC) under control of the XA270 ENAVDD signal. LK1 can be set to one of two positions. The position marked "5" is for 5V LCDs. The position marked "3.3" is for 3.3V LCDs. You may need to change the solder link to match your display.

D.2.3 Pin 41 and 38 Configuration: LK2 and LK3

LK2 and LK3 are connected to the 41-way connector pins 41 and 38 respectively. The links can be used to change the display orientation, at least on some Sharp displays. For a normal image both should be left open, or linked in the 2-3 position.

For an upside-down image both should be linked in the 1-2 position. Some other LCDs may use pins 41 and 38 for other purposes, such as additional power supply pins. LK2 and LK3 should therefore be linked to match the requirement of each display. Table D5 lists the connections of the LK2 and LK3 pins, thus allowing suitable connections to be made.

LK2 PIN	LK2 CONNECTION	LK3 PIN	LK3 CONNECTION
1	GND	1	GND
2	PIN 41	2	PIN 38
3	LCDVCC	3	LCDVCC

TABLE D5: TFTIF41 PIN 41 AND PIN 38 CONNECTIONS

LCDVCC is the LCD display voltage selected by LK1, as described in the previous section.

D.2.4 Backlight Enable Signal

The XA270 generates a logic-level signal intended to turn on and off the backlight inverter. This signal is called ENBKL, and is 0V for “off” and +3.3V for “on”. The ENBKL signal can be taken to a backlight inverter from the TFTIF41 connector J3. J3 is a Molex 53261-0390 connector. Pin assignments are given in Table D6. Note that some backlight inverters specify a 5V signal to turn on the backlight, so ENBKL may not work with all inverters. ENBKL is also available on connector J17.

J3 PIN	SIGNAL
1	VCC (+5V)
2	ENBKL
3	GND

TABLE D6: TFTIF41 J3 PIN ASSIGNMENTS

D.3 TFTIFKYV

The TFTIFKYV is designed to interface with a small number of LCDs, principally from Kyocera, that use a 33-way Molex connector. The TFTIFKYV has its own Technical Reference Manual, which provides more information on this product.

D.4 AAVGA CRT / VGA Interface Board

A VGA CRT or LCD monitor can be driven with the addition of the AAVGA adapter board, which plugs into the 40-way parallel TTL interface J2 on the XA270 and provides a standard 15-way D-type VGA connector. The AAVGA converts the parallel data from the XA270 to RGB signals displaying up to 64K colours.

APPENDIX E: TP400ET ETHERNET ADAPTER BOARD

The Ethernet port on the XA270 connects to a network through a small printed circuit board called the TP400ET. This is joined to the XA270 with a short length of unshielded twisted pair cable, the TB486ET-CAB. The TP400ET contains the Ethernet isolation transformer, EMC filters and an RJ45 connector with status LEDs. The TP400ET has been designed, so that EMC filtering is optimised when mounted in an enclosure. The TP400ET has two status LEDs indicating link and activity status.

Figure E1 shows the mechanical drawing for the TP400ET including dimensions and mounting positions and sizes.

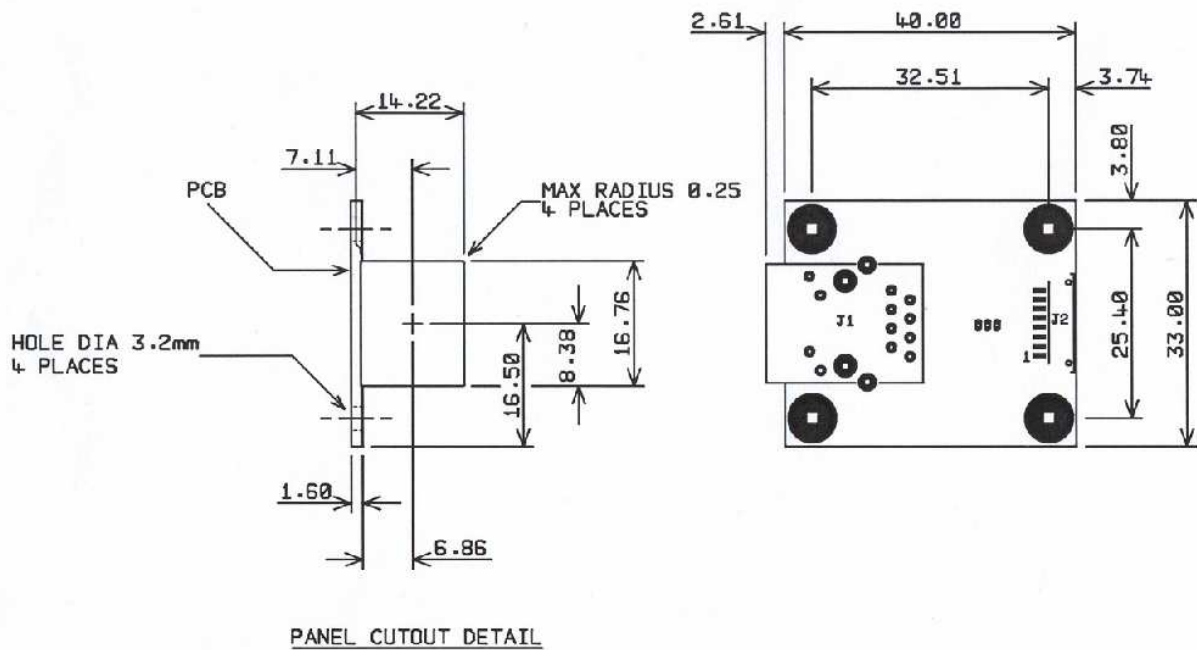


FIGURE E1: TP400ET MECHANICAL DRAWING

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APPENDIX F: TP300USB USB ADAPTER BOARD

The USB host ports on the XA270 connect to USB peripherals through a small printed circuit board called the TP300USB. This joins to the XA270 with a short length of unshielded twisted pair cable, the TB486ET-CAB. The TP300USB contains two Type-A USB sockets and EMC filters. The TP300USB has been designed, so that EMC filtering is optimised when mounted in an enclosure.

Two TP300USB's are required to implement all four host ports on the XA270.

Figure F1 shows the mechanical drawing for the TP300USB including dimensions and mounting positions and sizes.

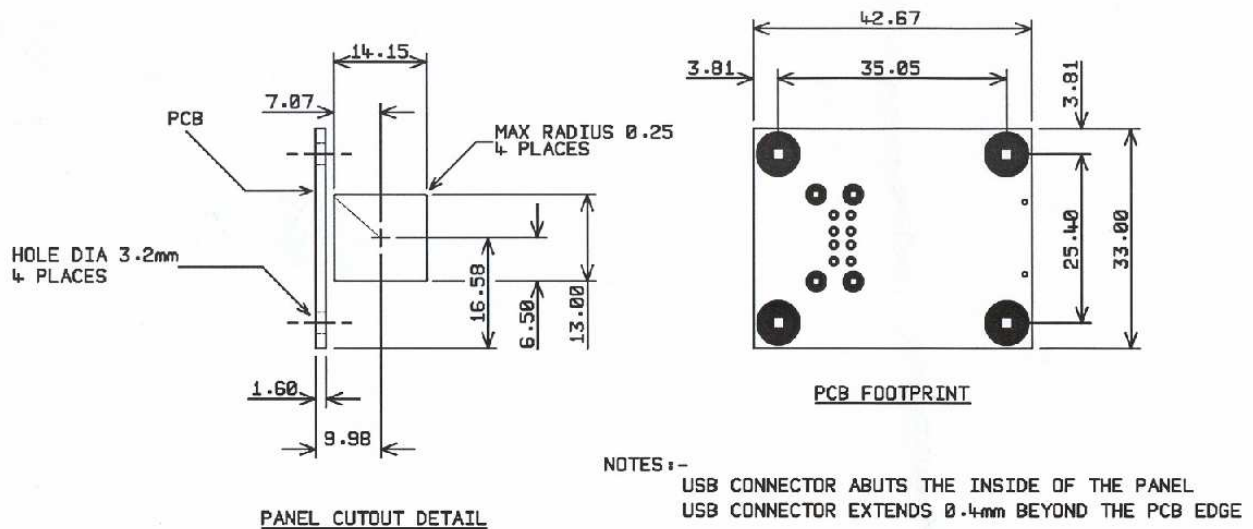


FIGURE F1: TP300USB MECHANICAL DRAWING

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APPENDIX G: XACONN CONNECTOR BOARD FOR THE XA270

G.1 INTRODUCTION

The XACONN is a connector breakout board for the XA270 PC/104 processor board. The XA270 mounts onto four pillars on the XACONN and then interfaces to the XACONN via a number of short cable assemblies, which are provided as part of the XACONN assembly.

The XACONN provides the following standard PC connectors mounted along one edge of the board for easy mounting in an enclosure:

- One RJ45 Ethernet socket.
- Two USB host Type-A connectors in a single stacked package.
- One USB client Mini-AB connector.
- Two 9-way male D-type connectors.
- Three 3.5mm audio jacks.

The XACONN also provides a number of board-to-wire connectors for interfacing to peripherals within an enclosure.

Unless otherwise described in the following sections, solder links are configured by DSP Design for test purposes and must remain unchanged. Failure to do so may result in unpredictable behavior.

G.2 ASSEMBLY DRAWINGS

A high resolution PDF of the XACONN assembly drawing is available on the DSP Design website.

G.3 MECHANICAL DRAWINGS

A high resolution PDF of the mechanical drawing is available on the DSP Design website.

G.4 ETHERNET

The XACONN provides a single RJ45 socket J9 (with built-in magnetics and link/activity LEDs) and EMC filters. The port also provides ESD protection. Socket J9 connects to a board to wire connector J7 on the XACONN, which in turn connects to J12 on the XA270 via a short length of CAT-5 twisted pair cable. Pin assignments for J7 are provided in Table G1.

Pin No	SIGNAL
1	RXD+
2	RXD-
3	VCC/VCC3V
4	GND
5	LINKLED#
6	LANLED#
7	TX-
8	TX+

TABLE G1: J7 PIN ASSIGNMENTS

G.5 USB HOST

The XACONN provides two EMC filtered Type-A USB host ports in a single socket J11. The socket connects to a board to wire connector J5 on the XACONN, which in turn connects to J3 on the XA270 via a short length of CAT-5 twisted pair cable. Pin assignments for J5 are provided in Table G2.

Pin No	SIGNAL
1	DM1
2	DP1
3	VCC1
4	GND1
5	VCC2
6	GND2
7	DM2
8	DP2

TABLE G2: J5 PIN ASSIGNMENTS

G.6 USB CLIENT

The XACONN provides a single EMC filtered Mini-AB USB client socket J10. The socket connects to a board to wire connector J8 on the XACONN, which in turn connects to J14 on the XA270 via a short length of CAT-5 twisted pair cable. Pin assignments for J8 are provided in Table G3.

Pin No	SIGNAL
1	NC
2	NC
3	NC
4	NC
5	VBUS
6	GND
7	USBC_N
8	USBC_P

TABLE G3: J8 PIN ASSIGNMENTS

G.7 AUDIO

The XACONN provides three EMC filtered, colour coded 3.5mm audio jacks. The sockets connect to a board to wire connector J4 on the XACONN, which in turn connects to J11 on the XA270 via a short length cable. The sockets are colour coded as shown in Table G4. Pin assignments for J4 are provided in Table G5.

IDENT	COLOUR	FUNCTION
J12	BLUE	HEADPHONE
J14	PINK	MICROPHONE
J13	GREEN	LINE OUT

TABLE G4: AUDIO SOCKETS

Pin No	SIGNAL
1	HPL
2	HPR
3	AGND
4	MICGND
5	MIC
6	AGND
7	LINEOUTL
8	LINEOUTR

TABLE G5: J4 PIN ASSIGNMENTS

G.8 COM1 AND COM2

The XACONN provides two full function 9-pin D-type sockets J15 and J16 for COM1 and COM 2 respectively. The sockets connect to a board to wire connector J20 (shared with other functions) on the XACONN, which in turn connects to J7 on the XA270 via a short ribbon cable. The pin assignments for J20 are provided in Table G6.

PIN	NAME	NOTES	PIN	NAME	NOTES
1	DCD1	COM1 RS232 carrier detect input	2	DSR1	COM1 RS232 data set ready input
3	RXD1	COM1 RS232 receive data input	4	RTS1	COM1 RS232 request to send output
5	TXD1	COM1 RS232 transmit data output	6	CTS1	COM1 RS232 clear to send input
7	DTR1	COM1 RS232 data terminal ready output	8	RI1	COM1 RS232 ring indicator input
9	GND	COM1 ground	10	DCD2	COM2 RS232 carrier detect input
11	DSR2	COM2 RS232 data set ready input	12	RXD2	COM2 RS232 receive data input
13	RTS2	COM2 RS232 request to send output	14	TXD2	COM2 RS232 transmit data output
15	CTS2	COM2 RS232 clear to send input	16	DTR2	COM2 RS232 data terminal ready output
17	RI2	COM2 RS232 ring indicator input	18	GND	COM2 ground
19	DCD3	COM3 RS232 carrier detect input	20	DSR3	COM3 RS232 data set ready input
21	RXD3	COM3 RS232 receive data input	22	RTS3	COM3 RS232 request to send output
23	TXD3	COM3 RS232 transmit data output	24	CTS3	COM3 RS232 clear to send input
25	DTR3	COM3 RS232 data terminal ready output	26	RI3	COM3 RS232 ring indicator input
27	GND	COM3 ground	28	GPIO9	General purpose input/output – OS dependant.
29	PB_IN	Reserved (Do not use)	30	RXD4	COM4 RS232 receive data input
31	RTS4	COM4 RS232 request to send output	32	TXD4	COM4 RS232 transmit data output
33	CTS4	COM4 RS232 clear to send input	34	GND	Ground
35	RESET#	Reset input	36	GND	Ground
37	SDA	I2C Data input/output	38	SCL	I2C Clock output
39	RXD5	COM5 RS232 receive data input	40	TXD5	COM5 RS232 transmit data output
41	AGND	Analog ground for LINE_IN_L	42	LINE_IN_L	Left audio line input
43	AGND	Analog ground for LINE_IN_R	44	LINE_IN_R	Right audio line input
45	GND	Ground	46	BATT	Battery Input
47	VCC	+5V Supply	48	VCC	+5V Supply
49	GND	Ground	50	GND	Ground

TABLE G6: J20 PIN ASSIGNMENTS

G.9 COM3, COM4 AND COM5

The XACONN provides three 2x5 way 0.1” pin headers J17, J18 and J19, for COM3, COM4 and COM5 respectively. The headers connect to a board to wire connector J20 (shared with other functions) on the XACONN. The pin assignments for J20 are provided in Table G6, and J17, J18 and J19 are provided in Table G7.

Pin No	J17 (COM3)	J18 (COM4)	J19 (COM5)
1	DCD3	NC	NC
2	DSR3	NC	NC
3	RXD3	RXD4	RXD5
4	RTS3	RTS4	NC
5	TXD3	TXD4	TXD5
6	CTS3	CTS4	NC
7	DTR3	NC	NC
8	RI3	NC	NC
9	GND	GND	GND
10	NC	NC	NC

TABLE G7: J17, J18 AND J19 PIN ASSIGNMENTS

The pin assignment of J17, J18 and J19 have been arranged so that IDC D-type cable assemblies can be easily interfaced. These cable assemblies are not available from DSP Design.

G.10 ADC

The XACONN provides a single 2x10 way 0.1” pin header J21 for the ADC inputs. The header connects to a board to wire connector J3 (shared with other functions), on the XACONN, which in turn connects to J13 on the XA270. The pin assignments for J21 and J3 are provided in Table G8 and G9 respectively.

Pin No	SIGNAL	Pin No	SIGNAL
1	NC	2	NC
3	NC	4	GND
5	NC	6	NC
7	+5V	8	TXD2
9	GND	10	NC
11	NC	12	NC
13	NC	14	ADCGND
15	ADC2	16	ADCGND
17	ADC1	18	ADCGND
19	ADC0	20	+3.3V

TABLE G8: J21 PIN ASSIGNMENTS

Pin No	SIGNAL
1	AD0
2	AD1
3	ADCGND
4	TSPX
5	TSPY
6	+3.3V
7	ADCGND
8	TSMX
9	TSMY

TABLE G9: J3 PIN ASSIGNMENTS

The pin assignment of J21 has been arranged to interface with the SP100EXP experiment board available from DSP Design. The function of the SP100EXP is to provide a set of analog voltages that can be measured by the A/D converter on the XA270. Sample application software can read these voltages and use these measurements as appropriate. Please refer to the SP100EXP TRM for further details.

The XA270 provides two ADC inputs, whereas the SP100EXP provides three ADC outputs. Solder links on the XACONN allow the three ADC outputs from the SP100EXP to be connected to either ADC input on the XA270.

ADC0 on the XA270 will connect to ADC0, ADC1 or ADC2 on the SP100EXP by linking LK2, LK4 or LK6 on the XACONN respectively. Do not fit more than one link at any time.

ADC1 on the XA270 will connect to ADC0, ADC1 or ADC2 on the SP100EXP by linking LK1, LK3 or LK5 on the XACONN respectively. Do not fit more than one link at any time.

Signal TXD2 connects to connector J21 via a solder link LK7. TXD2 connects to an LED on the SP100EXP which flashes with transmit activity on COM2. LK7 can be omitted disabling the LED.

G.11 POWER

The XACONN can be powered from a +5V +/-0.25V power supply through either a 2mm power jack J1, a board to wire connector J6 or via the XA270 through connector J20.

- J1 is a standard power jack with a positive center post. The TCONN-PSU is a suitable power supply, and is available separately from DSP Design or as part of the LaunchPad.
- J6 is a 6-way board to wire Molex connector, 53261-0671 with the pin assignments shown in Table G10.

Pin No	SIGNAL
1	GND
2	GND
3	GND
4	+5V
5	+5V
6	+5V

TABLE G10: J6 PIN ASSIGNMENTS

- The XA270 can be powered via a 4-way connector J10, which in turn can power the XACONN via the 50-way connector J20 on the XACONN.

G.12 SWITCHES

The XACONN provides three push button switches which connect directly to connector J20 (shared with other functions).

- Switch SW1 when pressed, will assert RESET# on J2 pin 35, which in turn will reset the XA270.
- Switch SW2 when pressed, will assert GPIO9 on J20 pin 28. The operation of GPIO9 is operating system dependant, so please refer to the Developer's Guide for further details.
- Switch SW3 is reserved for DSP Design use and will not effect the function of the XACONN or XA270.

G.13 I2C DIGITAL I/O

The XACONN provides an 8-bit LED driver, the PCA9551, connected to the I2C bus on connector J20 (shared with other functions). The PCA9551 drives four LEDs mounted along one edge of the board. Table G11 shows how the LEDs are connected to the PCA9551. Please note that two PCA9551 signals are connected to each LED, one of which must be configured as an output to drive the LED and the other as an input to read the LED status.

The circuit is provided to demonstrate expansion capabilities using the I2C bus and is mainly intended for use as part of the LaunchPad. Example code is provided as part of the LaunchPad. Please refer to the Developer's Guide for further details on interfacing with the PCA9551.

The PCA9551 has a slave address of 60h.

PCA9551 Pin Name	LED
LED0	LED1
LED1	LED2
LED2	LED3
LED3	LED4
LED4	LED1
LED5	LED2
LED6	LED3
LED7	LED4

TABLE G11: I2C LED CONFIGURATION

G.14 BATTERY

The XACONN provides a CR2032 battery holder for backing up the Dallas RTC on the XA270. The battery can be isolated from the XA270 via a three pin header J22. A jumper is fitted across pins 1 and 2 by default, connecting the battery to the XA270. If the battery is not required or needs to be isolated, fit the jumper across pins 2 and 3. This ensures the battery is isolated and the battery input to the XA270 on pin 46 of connector J20 is connected to GND. Removing the jumper completely may result in unpredictable behavior.

G.15 Touchscreen

The XACONN provides a single 9-way board to wire connector J2 for interfacing to touchscreens. J2 connects to a board to wire connector J3 (shared with other functions) on the XACONN, which in turn connects to J13 on the XA270. The pin assignments for J2 provided in Table G12.

Pin No	SIGNAL
1	NC
2	NC
3	NC
4	TSPX
5	TSPY
6	NC
7	NC
8	TSMX
9	TSMY

TABLE G12: J2 PIN ASSIGNMENTS

APPENDIX H: XA270 LINK SETTINGS

Table H1 shows the default solder link settings for the XA270. These are factory set and unless stated otherwise in this document, they must remain unchanged otherwise unpredictable behaviour may result.

LINK	SETTINGS
LK1	Fit 2-3
LK2	Not Fitted
LK3	Fit 1-2
LK4	Fit 1-2
LK5	Fit 1-2
LK6	Fit
LK7	Fit
LK8	Fit
LK9	Fit
LK10	Fit 1-2
LK11	Fit
LK12	Not Fitted
LK13	Fit 1-2
LK14	Not Fitted
LK15	Fit 1-2
LK16	Fit 2-3
LK17	Fit 2-3
LK18	Not Fitted
LK19	Not Fitted

TABLE H1: XA270 SOLDER LINK SETTINGS

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APPENDIX I: FAULT REPORTING

DSP Design makes every effort to ship products and documentation that are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a "Product Fault Report" form. If you ever have cause to return a module for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to your supplier.

Prior to returning a faulty product, please check the following:

1. The module has been correctly configured for the intended.
2. The power supplies are providing correct voltage levels.
3. Cabling to the module is sound and connected correctly.
4. Other cards in the system are known to be correctly configured and functioning.
5. **PLEASE RETURN THE MODULE TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT

CUSTOMER INFORMATION

PRODUCT INFORMATION

COMPANY NAME:

PRODUCT/DOCUMENT:

INDIVIDUAL CONTACT:

SERIAL NO:

PHONE NO:

DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE MODULE USUALLY USED? (WHAT OTHER MODULES, WHAT SOFTWARE ETC.)?

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT:

REPAIRED BY:

CHARGES TO BE INVOICED: £

DATE OF RETURN:

RETURNED BY:

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