DSP DESIGN
dspdesign.com

TP600

PC/104-Plus

PC Compatible Computer

Technical Reference Manual

Revision A01 | 23rd May 2012 | 158904.A02

(This page is the inside of the front cover, and is intentionally blank)

All information in this manual is believed to be accurate and reliable. However, no responsibility is assumed by DSP Design Limited for its use. Since conditions of product use are outside our control, we make no warranties express or implied in relation thereto. We therefore cannot accept any liability in connection with any use of this information. Nothing herein is to be taken as a license to operate under or a recommendation to infringe any patents.

Whilst every effort has been made to ensure that this document is correct, errors can occur. If you find any errors or omissions please let us know, so that we can put this right.

DSP Design Limited
Tapton Park Innovation Centre
Brimington Road
Chesterfield S41 0TZ
United Kingdom

Tel +44 (0) 1246 545 910
Fax +44 (0) 1246 540 576
Email sales@dspdesign.com
Web: www.dspdesign.com

(This page is intentionally blank)

TABLE OF CONTENTS

TABLES

FIGURES

REVISION INFORMATION

REV	BY	DATE	CR	DESCRIPTION
A02	ELR	23/05/12	7968	Updated to document USB floppy support under DOS and FFS drive letters following new BIOS release 158910.A02.
A01	IKD	15/02/12	7812 7813	Changed document number from 159804 to 158904. BIOS chip changed from 49LF004 512K byte to 49LF008A 1M byte.
A00	ELR	18/11/11	7737	This is the first version of this manual. It reflects the Rev A and Rev B versions of the PCB.

(This page is intentionally blank)

1 INTRODUCTION

This Technical Reference Manual describes the TP600 PC-compatible embedded computer.

1.1 OVERVIEW

To maintain our lead in advanced and highly integrated PC compatible computers, DSP Design have released a very highly integrated, high performance PC/104-Plus processor board. The board has been specially designed to allow low power operation.

The TP600 uses the AMD Geode LX800@0.9W processor and the CS5536 companion chip. This chipset provides a PC-compatible x86 processor with many integrated peripherals, including a flexible graphics engine.

DSP Design have added further peripherals around the AMD chipset to deliver a fully-featured embedded PC.

The TP600 can operate as a stand-alone module or can be used in a system consisting of a number of PC/104 and PC/104-Plus modules.

The TP600 has been designed to be a replacement for the TP500 and TP400B, and is almost identical in terms of functionality, connector position and pin assignments and so forth. Appendix I summarises the minor differences between these products and provides guidance on migrating to the TP600.

1.2 TP600 FEATURES

- High integration processor: a Geode processor is fitted, running at 400MHz.
- PC/104 16-bit bus interface for wide compatibility.
- PC/104-Plus connector is fitted to allow PCI expansion cards to be used.
- Floppy and IDE disk controllers.
- Four serial ports - three are RS-232 compatible and one provides TTL level signals only. COM2 is user-configurable as RS-485.
- Bi-directional Centronics parallel port. EPP and ECP compatible.
- Up to 1G bytes of SDRAM. SDRAM is implemented with a user-installable 200-pin DDR SODIMM module (dual in line memory module). 128M , 256M, 512M and 1G byte modules are available.
- BIOS installed in a 1M byte Flash memory chip.
- A separate 2M-byte flash chip implements a solid-state disk. A Flash File System license is provided with every TP600 to allow use as a read-write logical disk drive.

- Keyboard, PS/2 mouse and speaker ports.
- Two full-speed USB ports. Filter components and a dual USB socket are provided on a small PCB (the TP300USB, an optional extra) which connects via twisted pair cable to the TP600.
- The Geode integrates graphics circuitry, providing VGA graphics on CRT monitors at resolutions of up to 1280 x 1024 and TFT displays at resolutions of up to 1024 x 768. The graphics accelerator uses part of the system memory for high performance and low system cost.
- The Geode integrates a PC compatible sound system. The TP600 can record and play back high-quality audio.
- 10/100Base-T Ethernet chip. The Ethernet magnetics and RJ45 socket are provided on a small PCB (the TP400ET, an optional extra) that connects via twisted pair cable to the TP600.
- Powered by a single 5V supply. A switched mode power supply is provided to efficiently produce 1.25V, 2.6V and 3.3V for the processor and memory that require these voltages.
- Calendar/clock chip uses external battery.
- A 512-byte serial EEPROM is provided to retain set-up parameters in the absence of an external battery. Space is also available for user data.
- Reset, power supply monitor and watchdog timer circuitry.
- Expansion is by way of the ISA-compatible PC/104 bus connector. High performance expansion is by way of the PCI-compatible PC/104-Plus connector.

1.3 THE TP600 ARCHITECTURE

Figure 1 gives a block diagram of the TP600. As can be seen, the Geode processor connects to the DDR DRAM memory, the display and to the PCI expansion bus. The display shares the DRAM with the processor.

The CS5536 connects to the Geode processor through the PCI interface and provides a number of interfaces, including an interface to an AC97 audio codec, two USB ports and an IDE interface. The CS5536 also provides the core set of PC-compatible functions such as interrupt controllers, timers and the real-time clock.

The BIOS and a Super I/O chip are attached through the LPC bus. The Super I/O chip provides a number of interfaces including two full-function serial ports and a parallel port.

The PCI expansion bus hosts the 10/100Base-T Ethernet chip, and goes to the PCI-104 connector, where other PCI peripherals may be attached. An ISA bus bridge chip converts PCI signals to ISA bus signals. The ISA bus is sent to the PC/104 bus and to an extra UART chip, which implements COM3 and COM4.

A 16-bit PC/104 interface allows the TP600 to perform memory and I/O accesses to the PC/104 bus, and a PC104/Plus interface allows PCI bus transfers.

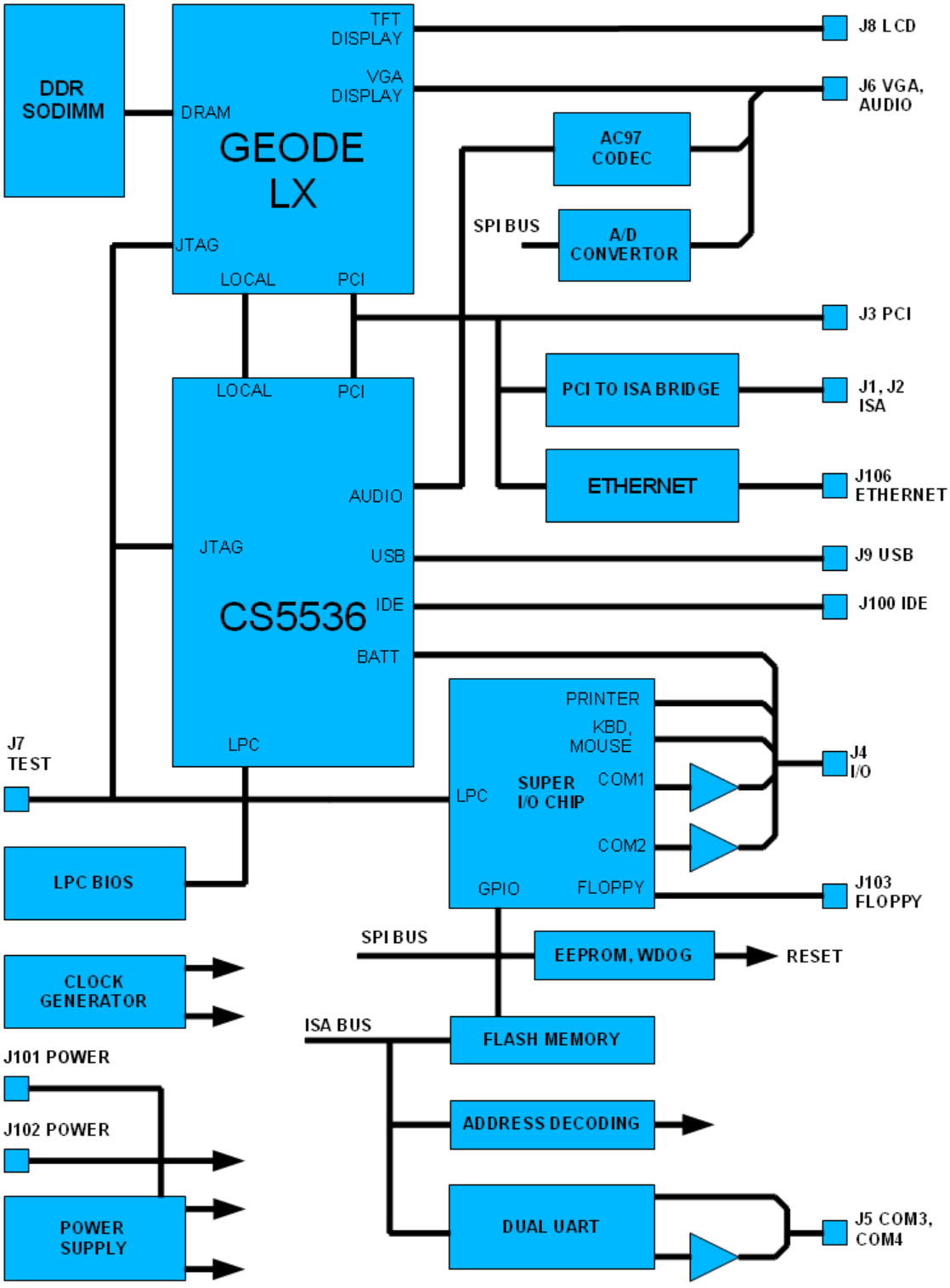


FIGURE 1 - TP600 BLOCK DIAGRAM

1.4 TCONN CONNECTOR BREAKOUT BOARD

The TCONN is a breakout board that provides an easy method of connecting to DSP Design's PC/104 processor boards. It mates with the I/O connectors of the PC/104 board, and provides standard PC compatible connectors for most of the peripherals.

All connectors are filtered, which greatly simplifies compliance with EMC standards. Features include:

- PC/104 board plugs directly into the TCONN.
- All connectors filtered for good EMC performance.
- Two 6-pin mini-DIN connectors for keyboard and mouse.
- Keyboard and mouse power rails have thermal fuse protection.
- Three 9-way D-type connectors for serial ports.
- 25-way D-type connector for printer.
- 15-way high density D-type connector for VGA.
- Circular power inlet connector.
- Pin header carrying miscellaneous signals.
- Lithium battery for CMOS SRAM and RTC.
- Small speaker.
- Reset switch.
- Power LED.

See Appendix D for ordering information.

1.5 LAUNCHPAD INTEGRATED HARDWARE/SOFTWARE DEVELOPMENT KITS

The LaunchPad products are a family of integrated hardware/software development kits for DSP Design computers and embedded operating systems. We've taken care of the tools so you can focus on your applications development.

The LaunchPad products will save significant amounts of development time for most users.

We have two objectives as you begin to use your new LaunchPad Development Kit.

Firstly, we expect that within an hour of receiving your LaunchPad you will have set up the hardware, connected it to your LAN and run the demonstration data acquisition application from a web browser.

Secondly, we expect that within a day you will have installed the development tools,

compiled a sample application, downloaded it to the target hardware, and debugged this application remotely from the host computer.

So on the second day you can begin developing your real application.

For full details of the LaunchPad Development kits see our web site at www.dspdesign.com/launchpad. Ordering information is given in Appendix D.

1.6 AVOIDING COMMON PROBLEMS

This section draws your attention to a number of issues that can cause problems, but that can be avoided if you are aware of them.

The battery pin must not be connected to +5V and must not be left floating. See section 3.6 for further details.

Some old disk drives and some Compact Flash cards do not report their parameters and so the parameters will need to be set manually for these devices. See section 3.9 for further details.

Some form of cooling may be needed for the Geode processor. This is discussed in section 2.2.

If you find that a USB peripheral does not operate correctly when directly plugged into the TP600, then you should consider using a powered hub. This is discussed in section 3.12.

There are some limitations in using PC/104-Plus boards which operate as bus masters.. See section 4.3.3 for details. Similarly, PC/104-Plus boards that operate with 5V signalling voltages cannot be used. This is discussed in section 4.3.2.

The TP600 display controller signals are 3.3V voltage levels. Some 5V displays may not work reliably with 3.3V displays. This is discussed in section 3.10.

1.7 FURTHER RESOURCES

Many people will have questions which are related to PC technology in general, rather than the TP600 specifically. We would recommend these two resources to answer these questions:

A book:

The Indispensable PC Hardware Book
By: Hans-Peter Messmer
Published: Addison-Wesley
ISBN: 978-0201596168

A web site: The PC Guide http://www.pcguide.com/

2 PROCESSOR AND MEMORY

The TP600 processor board is based around the AMD Geode LX family of processors. The BIOS is resident in a Flash memory chip. There is one SODIMM SDRAM socket. The standard TP600 is supplied without SDRAM memory, allowing you to choose memory to suit your application. SDRAM options are detailed in Appendix D, Options and Ordering Information.

2.1 PROCESSOR

The TP600 board uses the AMD Geode LX800@0.9W processor clocked at 400MHz. This chip has the following key features:

- An x86 processor with floating point processor and cache.
- A DRAM memory controller for DDR SDRAM.
- A PCI bus interface.
- A display controller with various graphics acceleration hardware.

The processor is available in a number of speed grades. DSP Design installs the mid-performance chip, known as the Geode LX800@0.9W, as standard. The maximum core clock frequency of this chip is actually 500MHz, but AMD claims equivalent performance to a VIA processor running at 800MHz. This chip can be configured to run at slower speed, which allows some saving in power consumption. DSP Design configure the processor to run at 400MHz as standard.

There are slower and faster parts available from AMD, including the LX600 @ 0.7W (maximum real clock speed is 366MHz), the LX700 @ 0.8W (maximum real clock speed is 433MHz) and the LX 900 @ 1.5W (maximum real clock speed is 600MHz). Boards fitted with slower or faster parts are available for customers placing volume orders. Please contact DSP Design if you require a slower or faster part.

Solder links on the PCB can be set to configure the processor clock speed and the memory bus clock speed, independently. The processor clock speed can be set between 166MHz and 600MHz with 33MHz increments. The memory speed can be set from one quarter to one half of the processor speed (though because the data transfer rate of DDR memory is twice this clock speed, the DDR data transfer rate is thus between half the processor clock speed and the same as the processor clock speed). Altogether there are 31 different combinations of processor and memory clock speeds.

Reducing the clock speeds has the effect of reducing power consumption. This effect is magnified by the fact that at slower clock speeds the processor core supply voltage can also be reduced.

Table 1 gives a few of the CPU, GeodeLink Interface Unit (GLIU) and memory clock speeds, the corresponding DDR transfer rates and power consumption when running ROM-DOS. See Appendix B for information on changing the clock speed.

CPU FREQUENCY (MHz)	GLIU FREQUENCY (MHz)	DDR CLOCK FREQUENCY (MHz)	DDR TRANSFER RATE (MHz)	POWER CONSUMPTION (W)
266	266	133	266	6.3
333	333	166	333	6.6
400	266	133	266	6.7
400	400	200	400	6.7
500	400	200	400	7.1

TABLE 1 - CPU AND MEMORY SPEED

The above measurements were made with an 8-chip 256M-byte SODIMM module installed. The power consumption figures were taken after DOS had booted and the processor was sitting idle at the DOS prompt.

2.2 PROCESSOR COOLING

Typical power consumption figures for the TP600 are between 6W and 7W under Windows XP Embedded and vary depending upon activity. These do not include the display or other peripherals.

A substantial proportion of this power is dissipated as heat by the processor. In most circumstances some cooling should be provided, or the processor may overheat. DSP Design can provide a passive heatsink which may be useful in ambient temperatures up to 55ºC – see Appendix D for ordering information. In some systems fans may be required. Ultimately cooling is a system design issue, and must remain the responsibility of the system design engineer.

Heatsinks should be mounted with a thermal bonding material to ensure good thermal contact. The heatsink listed in Appendix D comes with a square of double-sided adhesive material, with an aluminium substrate. This both provides good thermal contact and also mechanically secures the heatsink.

2.3 CS5536 COMPANION CHIP

The CS5536 is the second part of the Geode chip set. It attaches to the Geode processor mainly through the PCI bus. It provides these extra features:

- A PCI bus interface to the Geode processor
- Four USB ports (only two used by the TP600).
- IDE disk controller.
- AC97 audio sub-system
- Battery-backed Real Time Clock with CMOS SRAM
- Two UARTs (not used by the TP600)

- Power management logic
- Legacy PC hardware (interrupt controllers, timers etc.).

These peripheral functions are described elsewhere in this manual.

2.4 FLASH MEMORY

The TP600 is fitted with one 1M byte Flash memory chip residing on the LPC bus and one 2M byte Flash chip residing on the PC/104 bus.

2.4.1 BIOS

The BIOS is located in the 1M byte Flash memory chip residing on the LPC bus. The chip is an SST49LF008A. This Flash memory chip contains the BIOS: machine-dependent software that is used to configure the hardware, and to boot and support the operating systems.

Flash memory is non-volatile memory that can be programmed while it is installed on the TP600 or during manufacture. Data written to the Flash memory is retained after power is removed.

The BIOS makes use of "shadow RAM" in place of the Flash chip for greater speed. In this scheme the BIOS contained within the Flash chip is copied by the BIOS to SDRAM at the same addresses. The Flash chip is then disabled and the BIOS is executed from the 64-bit wide SDRAM, much faster than it would be from the Flash chip.

2.4.2 Flash File System

The 2M byte Flash chip is for a Flash File System. This chip is a 29F016 chip, connected to the ISA bus. This is used for storing programs and data for DOS-based programs.

The Flash File System memory chip occupies a relatively small memory footprint, and a paging mechanism allows the whole chip to be accessed.

The Flash File System is described in detail in section 6.6.

2.5 DDR SDRAM

The main memory of the TP600 consists of double-data-rate (DDR) SDRAM chips. The chips are mounted on a small 200-pin printed circuit board called a SODIMM module (small outline dual-in-line memory module). There is an SODIMM socket on the TP600. The memory is 64-bits wide. Four options are available:

- 128M bytes
- 256M bytes
- 512M bytes
- 1G Byte

The standard configuration of the TP600 is to have no SDRAM fitted. SODIMM modules must be ordered separately and fitted into the SODIMM socket on the TP600. Thus users can select the correct memory capacity for their application. See Appendix D - Ordering Information.

The use of SODIMM modules for SDRAM memory means that the SDRAM configuration can be altered at a later stage. DSP Design carry stock of the SODIMM modules described above, or customers may provide their own. DDR SODIMM modules should be used. The speed grade of the SODIMM modules are given in Table 2. The memory clock speed is selectable using solder links – see Appendix B for details.

MEMORY CLOCK (MHZ)	DDR DATA TRANSFER RATE (MHZ)	SODIMM SPEED
100	200	PC2100
133	266	PC2100
166	333	PC2700
200	400	PC3200

TABLE 2 - SODIMM MEMORY SPEEDS

Care must be taken when handling the TP600 and associated components. Ensure that all anti-static handling precautions are taken. See Appendix B – Configuration Information for instructions on installing SODIMM modules.

The BIOS automatically determines the amount of SDRAM present and configures the internal Geode registers accordingly.

Some of the SDRAM is taken from the processor and allocated to the graphics controller, using a technique referred to as UMA (unified memory architecture). Up to 16M bytes may be allocated to graphics. The BIOS default is for 8M bytes to be used.

Note that only the first 640k bytes of SDRAM are usually directly accessible by DOS. Some of the remaining SDRAM is used to shadow the BIOS (see section 6.1) and the remainder is re-mapped above the 1M byte boundary, where it can be used by DOS extenders and by Windows and other operating systems.

Memory between C0000H and FFFFFH (the top of the 1M-byte block) can be used to shadow BIOS code. This allows the BIOS to run at the fast SDRAM speed rather than the slow Flash speed. Typically the system BIOS (from E0000H – FFFFFH) and the VGA BIOS (from C0000H – C7FFFH) are shadowed. Memory beyond the 1M byte limit is available for Windows and other protected mode operating systems.

2.6 MEMORY ADDRESS MAP

Table 3 shows the memory map as configured by the standard BIOS of the TP600. This table shows the bottom 1M byte address space. Extra SDRAM is located immediately above the 1M byte boundary. Memory accesses beyond the top of the SDRAM are performed on the PCI bus.

The ISA bridge chip is programmed to claim certain memory address ranges and map these onto the ISA bus, where they are performed as ISA bus cycles.

The ISA bus bridge chip has four sets of memory address registers, allowing four blocks of memory address space to be mapped onto the ISA bus. These address ranges have been selected by DSP Design to provide a flexible set of addresses that should be suitable for most users. These are listed in Table 3.

ADDRESS	MEMORY DEVICE DECODED	MEMORY SIZE
FFFFF E0000	BIOS in Flash Chip – copied to shadow SDRAM memory during the boot sequence.	128K
DFFFF D0000	Available for PC/104 and PC/104-Plus memory mapped boards. BIOS Extension code can be located here.	64K
CFFFF C8000	Available for PC/104 and PC/104-Plus memory mapped boards. BIOS Extension code can be located here.	32K
C7FFF C0000	Usually VGA BIOS, which is copied from Flash chip to shadow SDRAM at this address. Alternatively used by VGA BIOS on PC/104 or PC/104-Plus bus that can also be shadowed.	32K
BFFFF A0000	Allocated to VGA memory.	128K
9FFFF 00000	SDRAM	640K

TABLE 3 - TP600 ADDRESS MAP – FIRST 1M BYTE

3 PERIPHERALS

This section describes the I/O address map and the on-board peripherals.

3.1 I/O ADDRESS MAP

The TP600 features a number of on-board I/O mapped resources, and supports access to the PC/104 bus I/O space as well.

All I/O mapped functions that are present on desktop PCs are present at the same I/O addresses on the TP600. The TP600 is therefore compatible at the machine code or register level with desktop PCs.

On-board I/O devices include registers within the Geode chip set, the Super I/O chip, Ethernet chip, the ISA bridge chip and the extra UART chip. The Super I/O chip contains the floppy disk controller, Utility Register, keyboard controller and the serial and parallel I/O ports. The on-board I/O addresses are listed in Table 4.

I/O accesses are routed as follows. I/O accesses within the Geode processor remain internal to this chip. I/O addresses that are within PCI bus devices (which includes the registers internal to the CS5536 chip) are performed on the PCI bus. PCI bus peripherals (implemented as PC/104-bus boards) can claim I/O accesses directed at them; the addresses occupied by the PCI peripherals are allocated by the BIOS during a power-on configuration process. The Super I/O chip includes certain I/O addresses. The ISA bridge chip is programmed to claim certain I/O address ranges and map these onto the ISA bus, where they are performed as ISA bus cycles.

The ISA bus bridge chip has six sets of I/O address registers, allowing six blocks of I/O address space to be mapped onto the ISA bus. These address ranges have been selected by DSP Design to provide a flexible set of addresses that should be suitable for most users. These are listed in Table 4.

Note that, in common with early ISA bus I/O boards, address decoding logic on PC/104 boards sometimes decodes only address lines A0 - A9, which can result in “aliasing” - whereby a PC/104 board can respond to more than one address. For example, a PC/104 bus board set for I/O address 200h may also respond at I/O addresses 600h, A00h, E00h and so on.

I/O addressing of PC/104-Plus (PCI bus) peripherals is to a large extent programmable, via each peripheral's PCI Configuration registers. These registers are programmed by the BIOS following reset, in a process that should normally ensure that no conflicts occur. PCI I/O addressing uses all 32 bits of the PCI address space, so aliasing cannot occur.

ADDRESS	I/O FUNCTION
00 - 0F	DMA Controller in Geode
20 - 21	Interrupt controller in Geode
2E - 2F	Super I/O Chip Configuration Registers
40 - 43	Timer Unit in Geode
60 and 64	Keyboard controller in Super I/O chip.
61	Port B Control/Status Port in Geode
70 - 71	Real-Time Clock in Super I/O chip and NMI enable in Geode.
72 - 73	Second bank of CMOS SRAM
80 - 8F	DMA Page Registers in Geode
92	Port A System Control Port in Geode
A0 - A1	Interrupt Control/Status Reg. in Geode
C0 - DE (Even addresses only)	DMA Controller in Geode
F0 - F1	Coprocessor Error Registers in Geode
1F0 - 1F7	IDE disk controller
200 – 2BF	Mapped onto ISA bus
2E0 – 2E7	Mapped onto ISA bus
2E8 - 2EF	COM4: in extra UART chip.
2F8 - 2FF	COM2: Serial Port in Super I/O chip.
300 – 34F	Mapped onto ISA bus.
378 - 37A	Parallel Port in Super I/O chip.
3B4 - 3B5	VGA Register in Geode (monochrome modes).
3BA	VGA Register in Geode (monochrome modes).
3C0 - 3CF	VGA registers in Geode.
3D4 - 3D5	VGA Register in Geode (colour modes).
3DA	VGA Register in Geode (colour modes).
3E0 – 3E7	Mapped onto ISA bus
3E8 - 3EF	COM3: Serial Port in extra UART chip.
3F0 - 3F7	Floppy Disk Controller
3F8 - 3FF	COM1: Serial Port in Super I/O chip.
481 - 48F	DMA high page registers.
4D0 - 4D1	IRQ edge/level select registers.
CF8 - CFF	PCI Configuration Registers

TABLE 4 - TP600 I/O ADDRESS MAP

3.2 SUPER I/O CHIP

Many of the peripheral functions are implemented in a single chip, the "Super I/O" chip. This is the W83627 from Winbond. The following functions are included in the W83627:

- Two serial ports (operating as COM1 and COM2).
- A printer port.
- A keyboard controller (providing a PS/2 mouse as well as the keyboard)
- A floppy disk controller.
- Several general-purpose I/O bits, used on the TP600 as the "Utility Register".

Each of these functions (except the general purpose I/O) have their own I/O addresses, allocated at the same locations as in every PC. In addition, the W83627 has its own set of configuration registers, which can be used by the BIOS to enable or disable each function, assign I/O addresses, place the functions in low power modes etc.

3.3 EXTRA UART

The Super I/O chip contains two serial ports; two further serial ports are provided by an additional dual UART chip, located on the ISA bus. This chip provides the COM3 and COM4 serial ports. The chip selects for these two ports are in turn generated by two of the programmable chip select registers within the Super I/O chip.

Further details of all four serial ports are given in section 3.4.

3.4 SERIAL PORTS

The TP600 features four serial ports that are accessed as COM1, COM2, COM3 and COM4. The first three are RS-232 ports. COM4 provides TTL level transmit and receive data signals only. Additionally the COM2 port can be configured for RS-485 operation.

3.4.1 Signals, Addressing and Interrupts

Table 5 lists the default physical locations, addresses and IRQ allocations for the four serial ports.

There is some control over serial port addresses and interrupt assignments of the two UARTs in the Super I/O chip (normally configured as COM1 and COM2). Control over these parameters is found in the SIO menu in the BIOS System Configuration Utility. Note that the BIOS is unaware of the two extra serial ports, COM3 and COM4, and it allows you to configure the Super I/O UARTs to occupy the same addresses and interrupts as COM3 and COM4 in the extra UART chip. If you do this conflicts will occur.

The UARTs in the Super I/O chip may also be disabled, which can be of use if you are using an external serial port – within a PCMCIA card for example.

NAME	I/O ADDRESS	INTERRUPT	HARDWARE LOCATION
COM1:	3F8h – 3FFh	IRQ4	Super I/O Serial port 1
COM2:	2F8h – 2FFh	IRQ3	Super I/O Serial port 2
COM3:	3E8h – 3EFh	IRQ5	Extra UART A
COM4:	2E8h – 2EFh	IRQ9	Extra UART B

TABLE 5 - SERIAL PORT RESOURCES

3.4.2 COM1 and COM2 RS232 Ports

COM1 and COM2 are standard, full function PC RS232 serial ports. They are implemented in a Super I/O chip on the LPC bus.

COM1 and COM2 are configured in the BIOS, normally to the standard PC I/O addresses and interrupts. However they can also be disabled by the BIOS Setup program.

These ports have RS232 transceiver chips that support three transmit signals (TxD, RTS and DTR) and five receive signals (RxD, CTS, DCD, DSR and RI).

Connection is made to the COM1 and COM2 serial ports via the 50-way J4 connector. See Appendix E for pin assignments of this connector.

3.4.3 COM2 Configured for RS485

COM2 can be configured as an RS-485 serial port by changing solder links on the board. This is described in Appendix B.

The COM2 RS-485 port configuration provides either half-duplex or full duplex interfaces. In full duplex mode one twisted pair is used for transmission and another twisted pair is used for reception. Full duplex mode would normally be used in point-to-point communication between two computers.

In half duplex mode the transmit and receive twisted pairs must be connected together at the TP600. In this mode several boards can be connected to the single twisted pair, with no more than one board driving the cable at once. A suitable protocol needs to be agreed by all nodes on the twisted pair to ensure that only one computer transmits at any one time.

On the TP600 the RS-485 driver is controlled by the RTS bit of the on-board UART. When RTS is off (inactive) the RS-485 transceiver chip does not drive the transmit twisted pair cable. This is the default state after a TP600 reset. When RTS is set active the RS-485 transceiver does drive the transmit twisted pair cable and the TP600 can transmit. Note that the receiver part of the transceiver is always enabled. Thus in half duplex mode COM2 will receive the characters that it transmits itself.

In RS-485 mode the DTR control output has no effect, and the CTS, DCD, DSR and RI status inputs are seen as asserted by software.

No RS-485 termination resistors are provided on the TP600. These must be provided externally if required.

When operating as an RS-485 port the COM2 RS-232 signals on connector J4 are re-assigned. Appendix E provides information on RS-485 pin assignments.

3.4.4 COM3 and COM4

COM3 and COM4 are implemented within the extra UART chip.

COM3 provides the full complement of RS-232 signals. Transmit Data, Request To Send (RTS) and Data Terminal Ready (DTR) are outputs from the TP600. Receive Data, Data Carrier Detect (DCD), Data Set Ready (DSR), Clear to Send (CTS) and Ring Indicator (RI) are inputs to the TP600.

COM4 provides only Transmit Data and Receive Data as 3.3V CMOS-level signals. The control inputs of COM4 are all connected so as to appear permanently asserted. COM4 provides output signals at 0V or 3.3V, and will expect signals of the same levels. Do not exceed 3.3V on the RxD4 input pin. Note that RS232 transceiver chips both provide level shifting and signal inversion, so the polarity of the signals of the COM4 port is opposite of that of the RS232 ports.

The COM3 and COM4 addresses are permanently set to the standard PC I/O addresses and cannot be changed. DSP Design allocate all four serial ports their own interrupt level, which is beyond the conventional PC standard.

Connection is made to the COM3 and COM4 serial ports via the 14-way J5 connector. The pin assignments of J5 is such that COM3 easily connects to 9-pin D-type connectors. See Appendix E for pin assignments of this connector.

Following a reset of the TP600 the serial ports are initialized as 9600 baud, one stop bit, eight data bits and no parity. These parameters can be changed by the MS-DOS MODE command.

3.4.5 Infra-Red Operation Modes

The COM2 port in the Super I/O chip can be programmed to support a number of Infra-red modes, including IrDA. At the time of writing the TP600 BIOS does not support the IrDA mode of the Super I/O chip.

3.5 PRINTER PORT

The TP600 implements a full-function Centronics compatible printer port. This port is the MS-DOS PRN device. The printer port is contained within the W83627 Super I/O chip.

The parallel port is allocated standard PC I/O addresses and interrupt which can be changed in the BIOS System Configuration Utility, in the SIO menu. By default the parallel port is enabled. The standard I/O address range is 378h – 37Ah and standard interrupt is IRQ7.

The BIOS configures the parallel port mode to Standard and Bi-directional (SPP) mode when the parallel port is enabled.

The parallel port can often be used to provide a small number of general-purpose I/O signals. As well as the eight-bit data port there are 5 input signals and four output signals.

The printer port control output signals (/STROBE, /AUTOFD, /INIT and /SLCTIN) are open drain with 10k pull-up resistors fitted. The printer port status inputs (BUSY, PE, SLCT, /ACK and /ERROR) have 10k pull-up resistors fitted. The printer port data lines (PD0-7) are driven to TTL levels when outputs. They have 10k pull-up resistors fitted.

The printer port signals are brought out on the 50-way J4 I/O connector on the TP600. See Appendix E for pin assignments of this connector.

3.6 REAL TIME CLOCK

As with all PCs, the TP600 computer includes a real-time clock circuit, closely associated with CMOS SRAM for storage of system settings. Calendar/Clock facilities are provided in all PC computers. The calendar/clock module is often known as the Real Time Clock, or RTC. These RTC functions emulate those found in the Motorola MC146818 chip, and include time of day functions, calendar functions and CMOS RAM for storing setup parameters. Calendar/clock functions are implemented within the CS5536 chip, which requires a battery to maintain the time and date when the TP600 is powered off.

The calendar/clock hardware is read by the BIOS, which maintains time and date on behalf of the operating system. The calendar/clock logic may be accessed through the MS-DOS calls (interrupt 1AH) or with MS-DOS TIME and DATE commands.

As well as the calendar clock functions there are 242 bytes of static RAM (usually called “CMOS SRAM”) that are backed up by the battery. Much of this is used to store configuration parameters used by the BIOS, but some may be available for use by third party applications. The clock registers and the first bank of SRAM are accessed at I/O address 70h – 71h. The second bank of SRAM is accessed at I/O addresses 72h - 73h.

A battery can be used to provide power to maintain the clock and CMOS RAM when the main +5V power supply is not present. This external battery should be connected between the BATT input and GND of J4. The battery voltage should be between 2.4V and 3.6V and can be either be a rechargeable battery (e.g. NiMH) or a non-rechargeable battery (e.g. Lithium).

When the battery is not provided, the BATT pin on the J4 connector should be connected to GND (0V). It must not be left floating, and it must not be connected to +5V.

The battery pin is called BATT and is pin 28. A ground pin exists on the adjacent pin, pin 27.

The calendar/clock circuitry draws approximately 1uA (maximum of 2uA at 25 degrees C and 6uA at 85degrees C) from the battery when the TP600 is powered down and draws no current when operating normally (i.e. powered up).

Figure 2 gives a suitable circuit for a rechargeable battery back-up circuit. Note that care must be taken with this circuit that the voltage at the BATT pin does not exceed 3.9V. This can happen if the trickle-charge resistor allows an excessive trickle-charge – in this case the battery voltage may rise over 4V. The 2k2 value seems suitable for a 150mAhr NiMH battery.

Note also that this circuit is suitable only when using a NiMH or Nicad battery. The circuit shown in Figure 2 is **not** suitable for Lithium or other non-rechargeable battery types. The diode, resistor and connection to VCC must be omitted if a lithium battery is used.

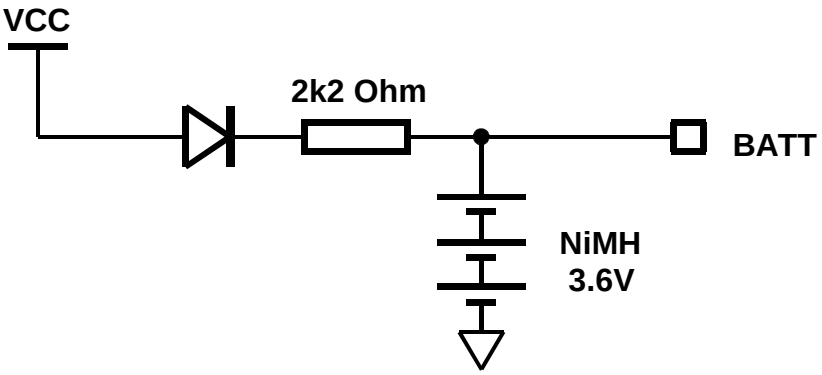


FIGURE 2 - RECOMMENDED BATTERY BACK-UP CIRCUIT

3.7 KEYBOARD AND MOUSE

The TP600 uses an AT or PS/2 type keyboard. Your supplier can provide a suitable keyboard. Alternatively, USB keyboards can be used - see section 3.12 for details of the USB ports.

In many applications the familiar desktop keyboard is inappropriate. A variety of industrial keyboards and keypads are available - contact DSP Design for details. The TP600 will work without a keyboard if required.

Users should avoid plugging in the keyboard or mouse when the TP600 is powered on.

The keyboard controller circuitry on the TP600 is contained within the Super I/O chip, and also includes a PS/2 style mouse port. The keyboard uses the IRQ1 interrupt line and the mouse uses IRQ12. Connections to the keyboard and mouse are made through the 50-way J4 connector.

Users should note that some DOS mouse drivers may not work with the TP600.

3.8 LEGACY FLOPPY DISK INTERFACE

The TP600 includes an on-board floppy disk controller. The floppy disk controller electronics are included within the Super I/O chip. To distinguish between this floppy disk interface and a floppy disk on the USB bus, this floppy disk interface is referred to as the legacy floppy disk interface.

Due to a limitation on PCB space the floppy disk controller is accessed through a 26-way flat flexible cable connector, J105, rather than the 34-way IDC connector used on older drives. The 26-way connector is used on floppy disk drives used in laptop PCs. The cable carries power as well as control and data signals. The laptop floppy drives tend to be much smaller than the drives used in desktop PCs. The signals used on the flat flexible cable are the same as used on the 34-way connector, so if necessary the older floppy drives could be driven.

DSP Design is able to supply suitable floppy disk drives and the 26-way cable. We are also able to supply an adapter board called the DIS35-26 that allows the 26-way cable to connect to drives with the older 34-way connector.

The floppy disk circuit uses an interrupt (IRQ6) and a DMA channel (DREQ2 and /DACK2).

With the default CMOS settings, the legacy floppy disk drive is normally accessed as A:, unless there is also a USB floppy drive installed, in which case the USB floppy drive is A: and the legacy floppy drive is B:.

The priority of USB and legacy floppy drives can be changed by swapping their order in the Boot menu of the BIOS System Configuration Utility. Placing Floppy 0, which corresponds to the legacy floppy drive, higher up the list than the USB floppy will ensure that the legacy floppy is always drive A:.

It is possible to boot from the A: floppy (legacy or USB) but not the B: floppy. The Boot menu in the BIOS System Configuration Utility allows you to select the boot device order and put either floppy above IDE if required.

3.9 COMPACT FLASH AND IDE DISK DRIVES

The Geode chip set includes an IDE disk controller. On the TP600 this is connected to a 44-way connector J100, which can connect to one or two external IDE disk drives, or to CF100 Compact Flash adapter boards.

The IDE drives occupy standard PC I/O addresses and use the standard IRQ14 interrupt. A number of data transfer modes can be set by the BIOS System Configuration Utility, or the transfer mode can be left in the default ”UDMA Mode (40 conductor cable)” setting.

3.9.1 IDE Drive

A mechanical hard disk drive or CD-ROM can be connected to the TP600 through the 44-way 2mm connector J100. This connector will connect directly to 2.5-inch IDE drives. CD-ROM drives and 5.25-inch disk drives typically use 40-way 0.1-inch connectors, and require an external power supply, so require appropriate cable assemblies to make the necessary transitions.

Mechanical drives are usually configured as the master or slave with a jumper on the drive. In systems with one drive, this drive must be configured as the master. In systems with two drives one must be configured as the master and one as the slave.

3.9.2 Compact Flash Drive

Compact Flash cards provide solid-state disk storage. Cards are available in a variety of capacities, ranging from a few megabytes to hundreds of megabytes or even gigabytes. In addition, mechanical disk drives are available in the Compact Flash form factor. These are referred to as Microdrives and are available in capacities of several gigabytes.

The TP600 supports Compact Flash cards through the use of the CF100 Compact Flash adapter board. This is a small printed circuit board which plugs onto the IDE connector J100 and which contains a connector for a Compact Flash memory module.

The CF100 PCB can be fixed to the TP600, mating directly on the J100 IDE connector. Alternatively it can be connected to J100 through a length of ribbon cable, and thus mounted elsewhere on the TP600 or elsewhere within the TP600's enclosure.

The Compact Flash cards can be removed from the CF100 and data transferred to other PC computers. DSP Design sells Compact Flash cards.

Some Compact Flash cards do not conform to the Compact Flash Specification, and we have found therefore that not all Compact Flash cards will operate with the TP600. Users who are considering buying their own Compact Flash cards should take care and if necessary seek advice. DSP Design supply Compact Flash cards which work. See Appendix D for ordering information.

Compact Flash cards may not be inserted or removed from the TP600 while the power is supplied.

The Compact Flash socket is configured as a master or slave by a solder link on the CF100. In systems with one drive, this drive must be configured as the master. In systems with two drives one must be configured as the master and one as the slave. When LK1 on the CF100 is fitted, the Compact Flash socket is configured as a master.

3.10 DISPLAY CONTROLLER

The Geode chip has a powerful in-built display controller. The controller is VGA-compatible and includes 2D and video acceleration hardware.

The display controller can support LCD displays of 640 x 480, 800 x 600 and 1024 x 768.

Display depth is up to 24 bits per pixel. The BIOS setup program allows the LCD display resolution to be set. The default resolution is 640 x 480.

The display controller uses a Unified Memory Architecture (UMA). This sets aside a portion of the main memory as a display frame buffer and other purposes. Up to 60M bytes can be allocated to the display controller. The amount of memory allocated is set by the BIOS Setup program (Chipset menu). For a 1024 x 768 x 24 bpp then 8M bytes is ample.

For a more complete view of the display memory requirements and other aspects of the Geode's display system please refer to AMD's document entitled “AMD Geode LX Processor Graphics Software Specification”.

Hardware frame buffer compression improves the memory bandwidth efficiency.

The display controller is VGA compatible and supports a number of VGA and VESA display modes. Native display drivers exist for Windows XP and other operating systems.

The display controller drives VGA monitors, and can drive TFT LCD panels as well. Simultaneous operation is possible. Users should note that the horizontal and vertical sync signals (HSYNC and VSYNC) are shared between both display interfaces. Table 6 specifies the DC characteristics of the display signals. The system designer should ensure that the selected displays do not require more than the available drive current, particularly for the HSYNC and VSYNC outputs which must drive both displays in parallel.

INTERFACE	SIGNALS	PARAMETER	MIN	TYP	MAX	UNITS
VGA	RED	Output Current	-	18.67	21	mA
	GREEN	Output Load	-	37.5	-	Ohms
	BLUE			Note 1		
TFT	R[7:0]	V_{OH}	2.4	-	VCC3V	V
	G[7:0]	V_{OL}	0	-	0.4	V
	B[7:0]	I_{OH}	-24	-	-	mA
	ENAB	I_{OL}	-	-	24	mA
	SHFCLK					
	ENABKL					
	ENAVDD					
Both	HSYNC	V_{OH}	2.4	-	VCC3V	V
	VSYNC	V_{OL}	0	-	0.4	V
		I_{OH}	-16	-	-	mA
		I_{OL}	-	-	16	mA

NOTE 1: There is a 75Ω resistor to GND on TP600. Connecting a VGA monitor with 75Ω termination will provide the specified output load of 37.5Ω.

TABLE 6 - DISPLAY SIGNAL DC CHARACTERISTICS

3.10.1 VGA Operation

Connection to a VGA monitor from the TP600 is made via the 16-way connector J6.

A variety of display resolutions and refresh rates can be set using the BIOS setup program and by operating system drivers.

Note that the TP600 display controller signals are 3.3V voltage levels. Some 5V displays may not work reliably with 3.3V signals. In this event, pull-up resistors (to 5V) on some timing or sync signals may be useful, although users must make their own decisions about this.

3.10.2 TFT Operation

Connection to flat panel displays is made through the 40-way 0.05” pitch connector J8.

Both 18-bit (6 bits each of R, G and B) and 24-bit displays (8 bits each of R,G and B) are supported. The 18-bit displays are driven by the 6 most significant bits of each of the R, G and B colour buses. The signals on the 40-way connector are summarised in Table 7.

Note that the TP600 display controller signals are 3.3V voltage levels. Some older 5V displays may not work reliably with 3.3V signals. In this event, pull-up resistors (to 5V) on some timing or sync signals may be useful, although users must make their own decisions about this.

The 40-way ribbon cable carries both 5V and 3.3V power supplies to the flat panel display.

DSP Design provide a number of interface boards for connecting to common displays, and can also supply the displays and backlight inverters. The display interface boards are documented in Appendix F. See Appendix D for ordering information.

SIGNAL	DESCRIPTION
R0-7	Red data. On 18-bit displays use R2-7
G0-7	Green data. On 18-bit displays use G2-7
B0-7	Blue data. On 18-bit displays use B2-7
SHFCLK	Pixel clock. This may be given different names by different display manufacturers.
HSYNC	Horizontal timing signal. This may be given different names by different display manufacturers.
VSYNC	Vertical timing signal. This may be given different names by different display manufacturers.
ENAB	Display Enable signal. This signal is active at times when valid data is being output. This may be given different names by different display manufacturers.
ENABKL	Backlight enable signal. High to turn on an LCD backlight.
ENAVDD	LCD power enable signal. High to turn on power to display.
VCC	+5V power supply. J3 carries VCC through two pins. It can provide 5V at a few hundred milliamps, but care should be taken not to draw too much power from the TP600, as the thin wires and small connectors will result in a voltage drop across the cable.
VCC3V	+3.3V power supply. J3 carries VCC3V through two pins. It can provide 3.3V at a few hundred milliamps, typically to power the electronics of an LCD, but care should be taken not to draw too much power from the TP600, as the thin wires and small connectors will result in a voltage drop across the cable.

TABLE 7 - LCD SIGNAL DESCRIPTIONS

3.11 SOUND

The TP600 includes a PC-compatible sound system. This is implemented in two parts – a simple beeper circuit, and a high-quality stereo system.

3.11.1 Beeper

A speaker interface circuit is present, and can be used to generate tones and clicks. A small speaker of around 8 ohms should be connected between the SPKR pin of connector J4 and VCC (+5V) or VCC3V (+3.3V). The speaker circuitry on the TP600 consists of a MOSFET with its source connected to GND. The drain is connected in series with a 33-ohm resistor, which in turn connects to the SPKR pin.

3.11.2 AC97 Codec

The Geode chip includes an AC97-compatible audio circuit. This is paired with an AC97 audio codec chip.

A subset of the available audio input and output signals are available to users. The features available are a mono microphone input, with phantom power, a stereo line out channel and a stereo line in.

The TP600 provides power for the microphone. A voltage of about 2.2V is applied to the microphone through a 2k2 resistor.

Due to a lack of connectors the analog to digital converter chip shares pins on connector J6 with the audio circuitry. Appendix B describes how pins on this connector can be assigned to one function or the other. See Appendix E for pin assignments of this connector.

Windows driver software is available for the audio sub-system. This is available as part of the LaunchPad Application Development Kits.

3.12 USB PORTS

The CS5536 chip implements two PCI-based USB controllers, providing four USB ports. Only two of the USB ports are available on the TP600. The USB ports can operate as USB v1.1 or USB v2.0, but only USB v1.1 is supported by DSP Design. The USB ports utilise the Open Host Controller Interface (OHCI) standard.

The USB ports may be used for keyboard and mouse and a wide range of other peripherals, such as memory sticks, floppy and CD-ROM disk drives, Bluetooth interfaces, cameras and biometric sensors.

The BIOS also provides support for USB floppy disk drives and USB CD-ROM drives under DOS.

A USB floppy drive requires no special set-up. Simply insert a floppy drive into a USB socket and use it as you would any floppy drive. The legacy floppy disk drive is normally accessed as A: unless there is also a USB floppy drive installed, in which case the USB floppy drive is A: and the legacy floppy drive is B:.

A USB CD-ROM requires a little configuration. To boot an operating system from a USB CD-ROM the BIOS setup must be configured so that boot from CD-ROM is enabled, and the CD-ROM device appears appropriately early in the list of boot devices. To use the CD-ROM drive as a DOS drive a driver will be required. This is likely to be specific to each CD-ROM drive.

Access to the USB ports on the TP600 is through the eight-way connector J9. Appendix E gives the pin assignments for the USB connector.

DSP Design manufacture a small printed circuit board, carrying a dual USB connector and EMC filtering components, which can be connected to the J9 connector by a short cable assembly. The USB printed circuit board is called the TP300USB and the cable assembly is the TB486ET-CAB. The TP300USB is designed to be mounted on an enclosure; this

location allows EMC filtering to be optimised.

The TP300USB and TP400ET-CAB are sold as optional extras. See Appendix D for ordering information. A circuit diagram and mechanical drawing of the TP300USB are given in Appendix H.

Each of the USB ports is powered by a current-limited 5V power supply line. An on-board USB power controller chip will limit the current sent to each peripheral at slightly above the 500mA limit set by the USB specification. Some users have reported that some USB devices do not operate correctly when directly plugged into the TP600, but that they do when plugged in via a powered hub. This leads us to believe that these USB peripherals may be exceeding the power output of the TP600.

The USB controller is implemented as a PCI device. It is allocated an interrupt, usually IRQ10, by the BIOS's Plug and Play software (see section 4.5 for details).

3.13 ETHERNET

A 10/100-Base-T Ethernet controller chip is provided on the TP600.

The chip used is the National Semiconductor DP83816, and it is connected to the on-board PCI bus (see section 4.3). The chip is configured by the BIOS during the POST process following reset. It is both I/O and memory mapped and uses one interrupt and bus mastering. The memory and I/O addresses are allocated by the BIOS so as to avoid clashes with other resources. The chip uses 256 bytes of I/O address space and 4K bytes of memory address space. The chip acts as a PCI bus master, for fast and efficient transfer of data across the PCI bus.

Device drivers are available for Windows XP. These are provided as part of DSP Design's LaunchPad Application Development Kit.

The Ethernet chip is connected to the network's twisted pair cable through a small printed circuit board called the TP400ET. This is joined to the TP600 with a short length of unshielded twisted pair cable. The TP400ET contains the Ethernet isolation transformer, EMC filters and an RJ45 connector with status LEDs. The cable assembly is the TB486ET-CAB. The TP400ET is designed to be mounted on the enclosure; this location allows EMC filtering to be optimised.

The TP400ET and TB486ET-CAB are sold as optional extras. A circuit diagram and mechanical drawing of the TP400ET are given in Appendix G.

The TP400ET has two status LEDs. The green LED connects to the LED10 and LED100 pins of the DP83816 and glows whenever the DP83816 receives valid 10Base-T or 100Base-T link pulses. The yellow LED connects to the LEDACT pin of the DP83816 and glows when the DP83816 transmits or receives a frame.

A serial EEPROM is connected to the DP83816. The EEPROM is programmed during the manufacturing process. It contains the 6-byte Ethernet address (IA, or Individual Address), as well as defining other parameters.

3.14 ANALOG TO DIGITAL CONVERTER

The TP600 includes a four channel 12-bit analog to digital converter chip. The converter allows analog signals to be monitored.

The analog to digital converter is a Maxim MAX1247 device. Communication with the A/D chip is through a serial link that is implemented in the Utility Register. Using this communications link the processor may configure the A/D converter or make conversions.

The A/D converter has four inputs, called ADC0, ADC1, ADC2 and ADC3. These inputs can be between 0V and +5V. The input voltages must not extend beyond this range, or else internal protection diodes will begin conducting. If there is a chance of the supply voltages exceeding the supply rails then current limiting resistors must be added external to the TP600, to limit this current to 4mA. This same restriction applies when the power is switched off - if the analog voltage is still applied to the A/D chip when the TP600 is powered off then the internal protection diodes will conduct, and so the current limiting resistors must be used.

The voltages are measured as a proportion of a reference voltage, VREF. VREF defines the input voltage that provides the full-scale digital reading. The VREF pin on the A/D chip can be driven from an external voltage source, or from the on-board VCC supply voltage (which is the default). A solder link allows this selection to be made. The accuracy of the measurement of course will be limited by the accuracy of the VREF voltage.

Measurements can be made as “single-ended” or “differential” measurements, as programmable options. In single-ended mode each of the four inputs are measured with respect to the AGND (0V) pin. (AGND is connected to the digital GND at a single point on the TP600). In differential mode the difference between two inputs is measured. The difference between ADC0 and ADC1 can be measured, as can the difference between ADC2 and ADC3.

Measurements can also be made as unipolar or bipolar, as programmable options. In Unipolar mode an input voltage of AGND will give a digital output of 0000h, and an input voltage of VREF will give a digital output of 0FFFh. In bipolar mode an input voltage of VREF/2 will give a digital output of 0000h, an input voltage of VREF will give a digital output of 07FFh, and an input voltage of 0V will give a digital output of 800h. Voltages between 0V and VREF/2 are treated as negative voltages, and converted into twos complement negative numbers. It is probably only sensible to use bipolar mode in conjunction with differential mode, where the difference between two inputs can be negative as well as positive.

Sample software for the A/D converter is provided in the TP600 Support Material. This software makes measurements using the A/D converter. The software may be used as a guide to users who wish to write their own A/D code.

A temperature sensor is provided on the TP600. This is mounted close to the Geode processor chip, and thus measures a temperature that will be related to that of the Geode package. Thus the temperature of the Geode can be estimated. This feature was added to allow the power management software to slow the processor down if it got too hot. At the time of writing this power management feature has not been implemented.

The temperature sensor is connected via a solder link to ADC3. If ADC3 is required to measure an off-board voltage then the solder link can be removed.

The temperature sensor is the National Semiconductor LM60C. It has a voltage output given by:

V = (T x 0.00625) + 0.424

where T is temperature in degrees C.

Expressed differently, the output is 6.25mV per degree C, with an offset such that 0 degrees C gives 424mV.

Alternatively:

T = (V - 0.424) x 160

The data sheets for the MAX1247 and the LM60C are in the TP600 Support Material.

Due to a lack of connectors the analog to digital converter chip shares pins on connector J6 with the audio circuitry. Four three-way solder links route the J6 pin to either the MAX1247 or to the audio circuitry. Appendix B describes how pins on this connector can be assigned to one function or the other.

In addition, there are four sites for capacitors, which can be added between the A/D input pins and analog GND, to reduce noise. Alternatively, these sites can be used to short unused inputs to GND. By default these sites are unpopulated. Contact DSP Design if you need to make use of these capacitor sites.

3.15 SERIAL EEPROM

The TP600 has a serial EEPROM chip fitted. This is used primarily to store set-up parameters in systems that lack a battery to retain configuration data in the CMOS SRAM. There is some space available in the serial EEPROM for users' data. The serial EEPROM chip also contains the watchdog timer, which is also accessed through the EEPROM's serial interface.

See sections 6.7 and 6.8 for information on using the serial EEPROM utility programs. See sections 5.2 and 6.9 for details of the watchdog timer.

3.16 UTILITY REGISTER

The TP600 has a Utility Register that controls a number of peripheral functions including the serial EEPROM, analog to digital converter interface and Flash memory programming. The Utility Register is formed by a number of the GPIO pins within the W83627 Super I/O chip. The Utility Register is accessed through the PnP configuration registers at I/O addresses 2Eh - 2Fh.

The Utility Register is used extensively by the Flash File System DOS driver software and the serial EEPROM and analog to digital converter software, and will not normally be accessed by the user. Table 8 gives the function of each bit in the Utility Register. Following reset all bits are set to logic 1. They have internal pull-up resistors fitted.

PORT	BIT	FUNCTION
1	0	BA14 (For Flash memory bank switching)
1	1	BA15 (For Flash memory bank switching)
1	2	BA16 (For Flash memory bank switching)
1	3	BA17 (For Flash memory bank switching)
1	4	BA18 (For Flash memory bank switching)
1	5	BA19 (For Flash memory bank switching)
1	6	BA20 (For Flash memory bank switching)
1	7	BA21 (For Flash memory bank switching)
2	0	/ENFLASH (Enables access to the Flash memory chips when 0)
2	1	Not used
2	2	Not used
2	3	Not used
2	4	Not used
2	5	Not used
2	6	Not used
2	7	Not used
3	0	/CSADC (To CS pin of the A/D converter. Active low.)
3	1	/CSEEPROM (To serial EEPROM. Active low.)
3	2	SK (Clock to serial EEPROM and A/D Converter.)
3	3	SI (Data to serial EEPROM and A/D Converter.)
3	4	SO (Data from serial EEPROM and A/D Converter.)
3	5	Not used
3	6	Not used
3	7	Not used

TABLE 8 - UTILITY REGISTER

(This page is intentionally blank)

4 STAND-ALONE OPERATION AND EXPANSION BUSES

The TP600 will operate as a stand-alone single board computer, or it can use the PC/104 bus interface to expand its capabilities with the wide range of PC/104 bus I/O cards currently available. The PC/104-Plus bus allows for expansion using high speed PCI chips. This section of the manual describes first the stand alone operation and then operation on the PC/104 and PC/104-Plus buses.

4.1 STAND-ALONE OPERATION

The TP600 will operate as a single board computer with the addition of the appropriate peripherals and a single +5V power supply. In stand-alone operation the TP600 need not be plugged into a bus.

The TP600 requires a +5V power supply. Power can be supplied in one of three ways.

The best option is to use the power connector J101. This is a four pin right-angle AMP HE14 shrouded header located near the Geode processor chip. Appendix E includes pin assignments of this connector and part numbers of suitable mating connector.

The second option is to use the PC/104 or PC/104-Plus buses. The PC/104 bus connectors include a number of +5V and GND pins. Some or all of these pins can be connected in parallel and the resulting +5V and GND connected to the power supply. This is the way the TP600 would be powered if it was inserted into a motherboard of the user's own design.

The third option is to provide power to the board through the 50-way I/O connector J4. This also includes a number of +5V and GND pins.

Users should take care to provide power to the TP600 through cables that are as short and thick as possible, and to make use of as many of the power and ground pins as possible, connecting them in parallel. This is to minimise the voltage drop that will occur through the resistance of the power cables and connector pins.

The battery pin must not be connected to +5V and must not be left floating. See section 3.6 for further details.

4.2 PC/104 BUS

The PC/104 bus is the same from an electrical and timing point of view as the ISA bus found in PC computers. However it is mechanically different, using a stacking connector instead of the gold-plated edge connector used in the PC.

The PC/104 interface is via the J1 and J2 connectors along the bottom edge of the TP600. The 64-way J1 connector provides the 8-bit data bus and the 40-way J2 connector provides the 16-bit signals. The TP600 is able to interface with both the 8-bit and 16-bit modules that meet the PC/104 specification.

The ISA bus is connected to the PCI bus by a bridge chip. This chip generates the ISA bus address, data and control signals, and decodes memory and I/O address spaces which are

to be routed to the ISA bus. See section 3.1 for a discussion of the ISA bus address decoding.

Pull up resistors, internal to the ISA bus bridge chip, of approximately 50k ohms are present on the SD0 - SD15 data bus signals, the interrupt input signals and most of the control signals. The IOCHRDY, /IOCS16, /MEMCS16 and /ZEROWS signals have 1k ohm pull up resistors.

The TP600 does not support ISA bus DMA transfers. The active low DACK- and TC output pins are connected to a pull-up resistor and the DREQ input pins are not connected.

The BUSCLK signal runs at 8.25MHz.

The TP600 has male PC/104 pins only, and so must be positioned at the top of a PC/104 stack. This is because the provision for cooling the Geode chip prevents a board being stacked on top of it.

The TP600 uses polarizing pins on the J1 and J2 connectors. Some early versions of the PC/104 specification did not use polarizing pins and it was seen that this could result in possible misalignment and subsequent product failure if power was applied before the error was discovered. “Key” positions have been assigned to the J1 and J2 connectors. These can be seen on the J1 and J2 pin assignment diagrams detailed in Appendix E. The key positions have had their pin removed to prevent entry by any adjacent pin.

The PC/104 specification is available on DSP Design's web site (www.dspdesign.com).

4.3 PC/104-Plus BUS

The TP600 features a PC/104Plus bus interface.

4.3.1 Overview

The PC/104-Plus specification extended the earlier PC/104 specification by adding a PCI bus interface. This is electrically the same as the PCI bus used in desk-top PCs, but it uses a high-density 120-pin connector along the opposite edge of the PCB to the PC/104 (ISA bus) connectors.

The PC/104-Plus bus standard allows existing PC/104 expansion boards to be used, but also allows for high-performance expansion boards using PCI bus logic chips.

For a full description of the PCI bus, see the PCI bus specification (www.pcisig.com). The PC/104-Plus specification (version 2.0) is available on DSP Design's web site (www.dspdesign.com).

4.3.2 PCI Slots

Functional blocks attached to the PCI bus are each allocated a "PCI Device" logical device number. These PCI Devices include on-board functions, such as the USB controller and Ethernet controller chip, and external PC/104-Plus boards.

The PC/104-Plus specification allows for the addition of up to four expansion boards using the PCI bus. PC/104 boards can be included in the system as well. The boards can be configured by a switch or similar to occupy one of four "slots", slot 1 to slot 4. Each of the four slots is allocated a different logical device number.

The Geode processor used on the TP600 has 3.3V PCI bus signals which are not 5V tolerant. The TP600's VI/O power supply pins are configured to be at 3.3V. This means that the TP600 cannot be used with PC/104-Plus or PCI boards which have 5V signal levels. It will operate with 3.3V boards and with boards which support either 3.3V or 5V operation.

Most of the PCI bus signals are bussed to all PCI boards in the system. Some signals however are unique to each board. These are the IDSEL, clock, bus request and grant pins. The interrupt pins also receive special treatment. A switch or solder links on PC/104-Plus boards configure the boards as occupying slots 1, 2, 3 or 4, and thus route these signals appropriately.

Each board receives a different address routed to its IDSEL pin. This allows each PCI board to be allocated an individual "PCI Device" number. The IDSEL pin is used during the configuration of each PCI Device.

There is a separate 33MHz clock for each board. Due to differences in clock track lengths on the TP600, a slot 1 board must be adjacent to the TP600, then the slot 2, slot 3 and slot 4 boards are added each further from the TP600 in turn.

The bus request/bus grant signals are also routed to each board separately. Note however that the TP600 only supports bus request/bus grant signals to one or two PCI expansion boards. See section 4.3.3 and for a full discussion of operation with bus master boards.

The interrupt pins are "rotated" one position with every board. The means that if four PCI boards are each asserting a single interrupt request (on their INTA# pin), the PCI bridge (in the CS5536 chip) receives four different interrupt requests, one on each of its four INTx# pins.

Please note that at the time of writing, the INTC# interrupt input to the CS5536 is not supported by the BIOS. Therefore boards configured for slot 3 will not be able to use interrupts, and boards configured for other slots that drive multiple interrupts may not work if one of those interrupts is rotated to the CS5536 INTC# position.

Table 9 describes the allocation of these point-to-point signals within a TP600 system. This table also notes the allocation of the IDSEL signals to the PCI devices within the CS5536 chip.

The CS5536 incorporates two internal PCI devices, both featuring multiple functions. These include the PCI host bridge, the graphics controller, two USB controllers, the PCI to ISA bus bridge, audio controller and an IDE device. There is also an on-board Ethernet chip. These devices are also listed in Table 9.

PCI DEVICE	DESCRIPTION	IDSEL ADDR.	PCI-104 CLK PIN	REQ/ GNT PAIR	5536 INTA#	5536 INTB#	5536 INTC# NOTE	5536 INTD#	SW. POS.
Device 1 Function 0	Host PCI Bridge	AD11	-	-	-	-	-	-	-
Device 1 Function 1	Video Device	AD11	-	-	INTA#	-	-	-	-
Device 1 Function 2	Encryption	AD11	-	-	INTA#	-	-	-	-
Device 9	ISA bridge chip	AD19	-	-	-	-	-	-	-
Device A	PCI-104 slot 1	AD20	CLK0	0	INTA#	INTB#	INTC#	INTD#	0 or 4
Device B	PCI-104 slot 2	AD21	CLK1	1	INTB#	INTC#	INTD#	INTA#	1 or 5
Device C	PCI-104 slot 3	AD22	CLK2	0	INTC#	INTD#	INTA#	INTB#	2 or 6
Device D	PCI-104 slot 4	AD23	CLK3	-	INTD#	INTA#	INTB#	INTC#	3 or 7
Device E	DP83816 Ethernet Controller	AD24	-	0	INTA#	-	-	-	-
Device F Function 0	ISA Bridge	AD25	-	-	-	-	-	-	-
Device F Function 2	IDE Controller	AD25	-	-	-	-	-	-	-
Device F Function 3	Audio Controller	AD25	-	-	-	INTA#	-	-	-
Device F Function 4	USB OHCI Controller	AD25	-	-	-	-	-	INTA#	-
Device F Function 5	USB EHCI Controller	AD25	-	-	-	-	-	INTA#	-

NOTE: At the time of writing, the CS5536 INTC# interrupt is not supported by the BIOS.

TABLE 9 - PCI BUS RESOURCE ALLOCATIONS

4.3.3 Operating the TP600 with Bus Master Boards

The PCI specification calls for a bus request (REQn#) and bus grant (GNTn#) signal for each slot. A PCI card that requires control of the PCI bus asserts REQn# and waits for a central bus arbiter to reply with (GNTn#). The PCI card can then initiate data transfers across the PCI bus. This mechanism is typically used to stream large blocks of data across the PCI bus between a card (such as an Ethernet or frame grabber card) and the memory of the processor.

The Geode chip set has only two spare request/grant pairs. Yet there is a potential requirement for four pairs on the PCI bus and a further pair for the on-board DP83816 Ethernet chip. To make the best possible use of the limited resources we have done the following.

One pair connects to the PC/104-Plus slot 2, as REQ1#/GNT1#.

The other pair connects to PC/104-Plus connector slot 1, and slot 3, and to the DP83816 Ethernet chip, as REQ0#/GNT0#.

Slot 4 does not have a REQ/GNT pair.

This means that one request/grant pair is always available to a PC/104-Plus card configured as slot 2 – this is the pair named REQ1#/GNT1#. A further request/grant pair is available to a PC/104-Plus card configured as slot 1, or as slot 3, or to the DP83816 Ethernet chip – this is the pair named REQ0#/GNT0#. Only one PCI peripheral may use the REQ0#/GNT0# pair. Normally this will be the Ethernet chip. But if the Ethernet chip is not being used (or its bus master function is not required) then two solder links on the TP600 can be removed, and REQ0#/GNT0# used by a second PC/104-Plus card requiring bus mastering – either in slot 1 or slot 3.

The reason for this routing is historical – this is the routing used on the TP400B and TP500, and it has been replicated on the TP600 to maintain compatibility.

The TPPCIC PCI adapter board can be configured as any slot, and so connected to either the REQ0#/GNT0# pair or the REQ1#/GNT1# pair.

It is worth noting that the TCVIDEO video frame grabber board can be configured as any PC/104-Plus slot and still have a choice of whether to connect to REQ0#/GNT0# or REQ1#/GNT1#. This is because on the TCVIDEO the request/grant pair can be selected independently of the PC/104-Plus slot number.

4.4 PC/104 AND PC/104-Plus CLOCK AND RESET SIGNALS

4.4.1 PC/104 Clock and Reset Signals

Two PC/104 clocks are provided: the bus clock (BUSCLK) and an oscillator (OSC). The BUSCLK runs at 8.25MHz. The OSC signal is a clock running at 14.31818MHz.

The TP600 can reset the PC/104 bus. See section 5 for details. The TP600 drives the PC bus RESETDRV signal but cannot be reset by the RESETDRV signal.

The TP600 can be reset by issuing a low going pulse on the /RESET pin of the J4 connector. In this way a system reset can be generated by an external signal or switch. The TP600 will then force the RESETDRV signal of the PC/104 bus to be driven.

4.4.2 PC/104-Plus Clock and Reset Signals

The PC/104-Plus bus provides four 33MHz clocks, one for each of the possible expansion boards.

The TP600 can reset the PC/104-Plus bus. See section 5 for details. The PC/104-Plus bus provides an active low reset signal, PCIRST#, which is asserted whenever the on-board hardware reset signal is asserted. The TP600 cannot be reset by asserting the PCIRST# signal.

The TP600 can be reset by issuing a low going pulse on the /RESET line of the J4 connector. In this way a system reset can be generated by an external signal or switch. The TP600 will then force the PCIRST# signal on the PCI bus to be driven. PCIRST# can also be asserted by system software, and in fact this happens when ctrl-alt-del is pressed when running ROM-DOS or MS-DOS.

4.5 INTERRUPTS

The Geode chip set contains the same interrupt controller circuit as is present on all PC computers. This consists of two 8259 type interrupt circuits, each with eight interrupt inputs. One 8259 is connected in cascade with the other, leaving 15 interrupts available.

Some of these 15 interrupts are used internally by the Geode chip set. Other interrupts are connected to on-board peripherals (serial ports and disk controllers for example). Further interrupts can come from the PCI bus or the PC/104 bus..

Table 10 shows how the interrupts are assigned.

4.5.1 On-Board and PC/104 Bus Interrupts

For IRQs 3, 4, 5, 6, 7 and 9, if the associated on-board peripheral is not programmed to generate interrupts then the interrupt may be used on the PC/104 (ISA) bus. Interrupts from the ISA bus (and this includes the interrupts from the COM3 and COM4 serial ports) are routed through the ISA bridge chip.

The allocation of interrupts to PCI bus devices, which includes the audio, video, USB and Ethernet controllers, is discussed in section 4.5.2.

All the PC/104 bus interrupts are programmed to generate an interrupt on a positive-going edge.

The Geode does not have a dedicated NMI pin, so non-maskable interrupts are not available on the TP600's PC/104 bus.

PC IRQ	ALLOCATION	DEFAULT
0	Timer	Timer
1	Keyboard	Keyboard
2	Cascades IRQ8-15 from second 8259 controller.	Cascade
3	COM2 or PC/104 bus board	COM2
4	COM1 or PC/104 bus board	COM1
5	COM3 or PC/104 bus board	COM3
6	Floppy or PC/104 bus board	Floppy
7	Printer or PC/104 bus board	Printer
8	Periodic interrupt from RTC.	RTC
9	COM4 or PC/104 bus board	COM4
10	PCI INTA#, INTB# or INTD#	INTD# (USB)
11	PCI INTA#, INTB# or INTD#	INTB# (Audio)
12	Mouse	Mouse
13	Floating point processor	Floating point
14	Compact Flash (IDE controller)	IDE
15	PCI INTA#, INTB# or INTD#	INTA# (Video, Ethernet)

TABLE 10 - INTERRUPT ALLOCATION

4.5.2 PC/104-Plus Bus Interrupts

The PCI-104-Plus bus (PCI bus) has three supported interrupt pins: INTA#, INTB# and INTD# (the INTC# interrupt is not implemented on TP600). These are routed to the CS5536 chip. The Plug and Play BIOS automatically allocates PCI interrupts to IRQs on boot. Only IRQs 10, 11 and 15 can be used for interrupts from the PCI bus. The default mapping with no PCI/104 boards plugged in is shown in Table 10. Note that the Geode chip set includes a number of internal PCI devices with interrupt sources which are also mapped to the INTx# signals, internal to the chip.

The PCI bus interrupts are active-low level-sensitive interrupts. In principle, several PCI devices can drive the same INTx# pin low, and one PCI board may drive more than one interrupt line (a PCMCIA controller board sold by DSP Design does this – one interrupt for each PCMCIA slot). In practice, few boards drive more than one INTx# line, and a rotation of the INTx# pins from one slot to the next ensures that if each of three boards drive their INTA# pin, the TP600 will see one interrupt on each of INTA#, INTB# and INTD#. However, the limited number of unassigned interrupts in the TP600 mean that PCI cards may need to share an IRQ level. Further details on interrupt 'rotation' can be found in Section 4.3.2 and Table 9.

The on-board Ethernet chip is connected to the INTA# signal, as is the video device internal to the Geode chipset. There is a PCI audio controller within the Geode chip set. This is connected (internally) to the INTB# signal. There are two PCI USB controllers within

the Geode chip set. These are both connected (internally) to the INTD# signal.

When a PCI device (which includes the on-board audio controller, video device, USB controllers and Ethernet chip) is detected by the BIOS during the power-on self test (POST) process, the BIOS automatically allocates an IRQ level to it (either 10, 11 or 15).

The Geode chipset does not support the PCI bus SERR# and PERR# pins.

4.5.3 Plug and Play Control of Interrupts

The PnP BIOS is aware of most of the interrupt requirements of the on-board peripherals. It uses this information to try to eliminate conflicts between different devices requiring the same IRQ. This is most evident with PCI bus devices, which normally have their IRQ level allocated to them by the PnP BIOS during power-on self test (POST). The PnP BIOS allocates an IRQ level that is believes is unused.

This gives rise to an anomaly. The PnP BIOS is not aware of the existence of COM3 or COM4. It is therefore possible for their interrupts (IRQ5 or IRQ9) to be allocated to other PnP devices without the PnP BIOS being aware of a conflict.

4.6 DMA

The Geode processor contains the same DMA controller circuit as is present on all PC computers. This consists of two 8237 type interrupt circuits, each with four DMA Request (DREQ) inputs and four DMA acknowledge (DACK) outputs. One 8237 is connected in cascade with the other, leaving seven DMA channels available.

However, due to incompatibility between the Geode chip set and the ISA bridge chip, the ISA bus DMA signals are not implemented on the TP600. The floppy disk controller makes use of a DMA channel, but this is not routed through the ISA bus.

The PC/104-Plus bus (PCI bus) has no DMA signals.

5 HARDWARE RESET OPTIONS

A full set of hardware reset options exist for the TP600. The reset circuit is built around the X5043 serial EEPROM chip, which provides reset functions as well as memory. This chip includes a power supply monitor and a watchdog timer. To avoid glitches on the reset signal, the X5043 will always hold the reset signal asserted for approximately 200ms. This ensures all circuitry is properly reset, and conforms to the PC/104 bus specification.

The X5043 resets the CS5536 chip, on-board circuitry and the PC/104 bus. The CS5536 chip responds to its reset by resetting the Geode processor and the PCI bus.

5.1 POWER SUPPLY MONITOR

The X5043 monitors the +5V supply voltage. When the supply drops below about 4.5V the X5043 will assert the TP600 reset signal. Once the power supply returns to within specification, the reset signal will be released after further 200ms. This circuit prevents power "brown-out" causing unpredictable behaviour.

Users should note that if the voltage drop across the cables that link the power supply to the TP600 is excessive then the power supply monitor may reset the TP600. This may also happen if there are noise spikes on the power supply. It is recommended that all power supply cables be as thick and short as possible to minimize the voltage drop across them.

5.2 ONBOARD WATCHDOG TIMER

A watchdog timer exists on the X5043. The function of a watchdog timer is to reset a computer if the software has crashed. The correct operation of the timer relies on software to access the watchdog timer hardware on a regular basis. If the software crashes, the watchdog timer will not be "kicked" and so eventually it will time-out and reset the computer. The watchdog timer function is accessed via the Utility Register.

The Utility Register is a multi-function register that among other things gives access to the four control signals on the X5043 serial EEPROM. The Utility Register is described in section 3.12. The watchdog is enabled by writing an enable command to the X5043 via the Utility Register. Once this has been initiated, an internal clock to the X5043 starts counting and will continue to count until it times out, until the watchdog timer is “kicked” by the user’s application software, or until the watchdog timer is disabled by a disable command sent to the X5043.

The watchdog timer period can be set to approximately 1.4s, 600ms or 200ms, or it can be disabled, by writing different command words to the serial EEPROM command register. Once it has been enabled the watchdog timer must be accessed repeatedly by the user’s software. If the watchdog timer is allowed to time out the X5043 chip will issue a hardware reset to the TP600 (and to the PC/104 and PC/104 buses).

The watchdog timer is “kicked” by taking its chip select (/CS) pin low then high. The /CS pin is driven by Port 3 Bit 1 of the Utility Register. The TP600 Support Material has documented sample code illustrating the use of the watchdog function, and also includes the data sheet of the X5043. Note that it is the responsibility of the user to design code that will reliably kick the watchdog timer.

The BIOS includes code that disables the watchdog timer immediately after a reset, and thus if a watchdog time-out occurs the watchdog timer is disabled until after the operating system is loaded and the application software re-enables it. See sections 5.2 and 6.9 for further information on the watchdog timer.

5.3 RESET SWITCH

The TP600 can be reset by issuing a low going pulse on the /RESET line of the J4 connector. In this way a system reset can be generated by an external signal or switch. The reset switch connects between J4 pins 23 and 24. (Pin 24 is the /RESET input, and pin 23 is a GND pin). The TP600 will then force the RESETDRV signal on the PC/104 bus and the PCIRST# signal on the PC/104-Plus bus to be asserted.

5.4 RESETTING THE PC/104 AND PC/104-Plus BUSES

The TP600 always resets the PC/104 and PC/104-Plus buses whenever the X5043 is driving the TP600 on-board reset signal - that is, in response to a power failure, watchdog timer time-out, or a low going pulse on the /RESET line of the J4 I/O connector.

It is not possible to reset the TP600 by driving the RESETDRV signal on the PC/104 bus or the PCIRST# signal on the PC/104-Plus bus.

PCIRST# and RESETDRV can also be asserted by system software, and in fact this happens when ctrl-alt-del is pressed when running ROM-DOS or MS-DOS.

6 SOFTWARE

The TP600 offers a very high degree of PC compatibility. The vast majority of software (both operating systems and applications software) that will run on a conventional PC will also run satisfactorily on the TP600.

Most users will wish to use the ROM-DOS (or MS-DOS) or Windows operating systems (booting from a hard disk or floppy disk) and then run off-the-shelf software, or their own application. Other users will want to use Linux or one of the real-time operating systems.

The LaunchPad products are a family of integrated hardware/software development kits for PC/104 computers and embedded operating systems. We've taken care of the tools so you can focus on your applications development.

DSP Design offers a number of software utilities to ease software development. These are described here.

6.1 SYSTEM BIOS

The system BIOS is a program that interfaces between the TP600 hardware, the operating system and application code. It is responsible for controlling the TP600 hardware and providing a standard interface to the higher levels of software. The BIOS also deals with functions such as initialisation and testing of the TP600 hardware following power-on.

The TP600 uses a system BIOS supplied by General Software. General Software has since been acquired by Phoenix Technologies. Users should note that the BIOS is the copyright of General Software / Phoenix.

The BIOS has an in-built System Configuration Utility, which can be invoked by typing the DEL key at the keyboard during the boot sequence. Section 6.2 contains more information on the System Configuration Utility.

The BIOS is programmed into the Flash memory chip as part of the manufacturing process. The system BIOS and display BIOS extension are combined in a single 512k byte file, which is programmed into the 1M byte 49LF008A Flash memory chip. This is the chip in the 32-pin PLCC socket, and is henceforth referred to as the LPC Flash chip, as it is attached to the the Geode processor through the LPC bus. The contents of the Flash memory chip can be changed by the user if necessary, as described in section 6.5.

6.2 BIOS SETUP PROGRAM

The BIOS has an in-built System Configuration Utility, which can be invoked by typing the DEL key at the keyboard during the boot sequence. The configuration utility allows many system parameters to be changed and then stored in CMOS memory. Amongst the parameters that can be changed are the current time and date, display resolution, drive boot sequence, enabling and disabling of peripheral devices and interrupt allocation.

6.2.1 Operation of the System Configuration Utility

The System Configuration Utility is menu driven, and its operation should be self-explanatory. Users are advised not to change parameters that they do not understand.

Configuration parameters are stored in the on-board CMOS memory, and it is backed-up if an external battery is provided. If no external battery is present then the Configuration parameters can be stored in an on-board serial EEPROM, as described in section 6.7. If neither the CMOS SRAM nor the serial EEPROM contain valid data then default settings will be loaded from the BIOS.

The default values can also be restored by an option in the Exit menu of the System Configuration Utility.

The LCD display resolution can be set in the Chipset menu.

The COM1 and COM2 serial ports can be configured in the SIO menu. The ports can be disabled and their interrupts re-assigned. This could be required, for example, to allow the TP600 to co-exist with other PC/104 boards that are already using the standard COM1 and COM2 addresses. If the serial ports are not required then their interrupts can be made available for other uses.

The COM3 and COM4 cannot be explicitly disabled.

The parallel address and interrupt can also be changed in the SIO menu. If the printer port is not required then its interrupt can be made available for other uses.

The System Configuration Utility allows the splash screen to be enabled and disabled. The splash screen is disabled by default.

The disk drive boot order can be changed in the Boot menu.

6.3 VGA BIOS AND OTHER BIOS EXTENSIONS

As well as the system BIOS, the Flash memory chips contain other BIOS extensions. These include the VGA BIOS.

6.3.1 Principles of Operation

The system BIOS and the VGA BIOS extension are combined into a single 512k byte file, which is programmed into the LPC Flash memory chip using a Flash programming utility, as described in section 6.5.

As well as executing BIOS extensions contained within the Flash chips, the BIOS also searches the PC/104 and PC/104-Plus buses for BIOS extension EPROMs that might be present elsewhere in the system. The BIOS searches on every 2k byte boundary from C0000h to just below the system BIOS at E0000h. If valid BIOS extension EPROMs are found on the PC/104 or PC/104-Plus buses then they are executed.

The system BIOS is shadowed, and BIOS extension code in the Flash chip, such as the VGA BIOS is also shadowed. BIOS extensions that may reside on other PC/104 modules (such as VGA boards or LAN boards) are not shadowed by default.

6.3.2 The VGA BIOS Extension

The VGA BIOS extension is 32k bytes in size, and is located at address C0000h.

Before the TP600 BIOS installs a VGA BIOS for the on-board graphics logic from within the Flash chip it first examines the PC/104 and PC/104-Plus buses, looking for any other VGA BIOS that may be present. If another VGA BIOS exists (because the user is using another graphics controller) then this other VGA BIOS and its associated VGA controller hardware are used.

6.4 OPERATING SYSTEMS

6.4.1 ROM-DOS

DSP Design have licensed the ROM-DOS operating system from Datalight. ROM-DOS is an MS-DOS compatible operating system.

Each TP600 shipped includes a license for ROM-DOS, although ROM-DOS is not pre-loaded on the TP600. See information in the TP600 Support Material for instructions on how to obtain ROM-DOS v7.1.

As modern C and C++ development software no longer produce code for DOS operating systems, Datalight have a licence agreement with Borland to offer Borland's C++ 5.2 Development Kit for use with ROM-DOS. This Integrated Development Environment (IDE) includes a compiler and debugging tools. These Borland tools are only available as part of the ROM-DOS Software Developer’s Tool Kit, available from Datalight.

6.4.2 Other Operating Systems

As well as ROM-DOS, the TP600 will run any version of MS-DOS, and should run any other operating system which will run on a PC. For example Windows CE, Windows XP, QNX and Linux run successfully on the TP600.

There are LaunchPad integrated hardware/software development kits available for some of these operating systems. See section 6.10 and our web site at www.dspdesign.com/launchpad for details.

6.5 FLASH MEMORY PROGRAMMING

Flash programming utility programs provide facilities for programming data into the Flash memory chips on the TP600. The programs can erase some or all of the Flash chips, and can write a file from disk to the Flash chips. The most common use of these programs is to safely program the BIOS image file into the LPC Flash memory chip. Care must be taken when reprogramming the BIOS, since an error can erase the BIOS, which means the TP600 will stop working.

6.5.1 Programming the LPC Flash Chip

It should not be necessary to reprogram the system BIOS. However, a utility is available to do this. The program is called REFLASH.EXE and it is available as part of the TP600 Support Material.

To program a new BIOS file, type this: REFLASH <filename>

6.5.2 Steps to Perform after Programming BIOS

Once you have re-programmed your system BIOS there are several steps that MUST be undertaken to complete the BIOS update process. These steps are listed below.

1. Re-program the system BIOS as discussed above.
2. Re-boot by powering the TP600 system off and on. Do not use a push button reset or a Ctrl-Alt-Del reset.
3. Enter the Setup program by pressing the DEL key.
4. Load BIOS defaults.
5. Once in Setup, make whatever changes are appropriate.
6. Save the new settings to CMOS memory and exit. This will cause the TP600 to re-boot using the new BIOS parameters.
7. If you have previously run TP3EE.EXE -C (to save CMOS to EEPROM), then you MUST do this again to save the new BIOS parameters into the serial EEPROM.

6.6 FLASH FILE SYSTEM

This section describes the Flash File System, or FFS, for which TP600 is licensed.

The Flash File System is intended for ROM-DOS and MS-DOS. Users of other operating systems may not be able to use the Flash File System.

6.6.1 Overview

The FFS licensed with the TP600 is the FlashFX product from Datalight Inc. DSP Design have paid a license fee for every standard TP600, so you may use the Flash File System on every standard TP600 you buy. Some volume users who do not require the FFS may ask for TP600 boards without the license, to reduce costs.

The Flash File System driver is implemented as a loadable device driver. It can be used when another device (an IDE drive for instance) is the boot device. The loadable device driver places the FFS as the last drive in the system. This will usually be D: or E: depending on what other drives are installed.

The Flash disk must be formatted before use. This can be achieved using the loadable device driver.

The loadable device driver requires the driver to be placed on the boot disk and is activated by an appropriate entry in the CONFIG.SYS file.

The FFS driver operates by intercepting calls to the BIOS disk drive sub-system, which uses software interrupt INT13. Calls that are not intended for the FFS are passed through to the BIOS. Calls that are intended for the FFS are performed by the FFS driver.

The Flash File System is designed for MS-DOS and related operating systems. It is likely that the Flash File System driver will not operate with other operating systems, and will need to be disabled.

6.6.2 Operation of the Flash File System

The standard TP600 is shipped from DSP Design with the Flash disk already formatted. Thus most of this section is for information only, as steps 2 - 5 below have already been performed.

The Flash File System software referred to here is in the TP600 Support Material, in the FFS directory.

To operate with a Flash File System, perform the steps below:

1. Boot your computer from a Compact Flash disk or floppy disk containing the FFS driver in its loadable device driver form and a suitable entry in the CONFIG.SYS file. The loadable device driver is FTP3AMD.SYS and the corresponding entry in CONFIG.SYS is:

```
DEVICE=FTP3AMD.SYS
```

2. When the Flash File System driver loads it will display a sign-on message to confirm that it has been located.

3. Before the Flash File System can be used the Flash disk must be formatted, using a dedicated formatting program called FXFMT.EXE. The syntax of the FXFMT program is:

   FXFMT <drive> /P128 /T<size>M [/options]

   <drive> is the drive letter, usually D: or E:

   <size> is the size of the flash array to format in Mbytes, usually 2.

   [/options] can be any or all of the following:

   /C This is an optional parameter, and tells the program to format the drive without prompting the user for input (not recommended).

   /V This is an optional parameter and allows a volume label to be placed on the disk. After a format, the program will prompt the user for a volume name.

   Most users will type:

   FXFMT D: /P128 /T2M

5. At this point you have a functioning Flash disk.

6.6.3 Write Operations and Garbage Collection

The FFS implements a wear-levelling algorithm, to ensure that all parts of the Flash chip are equally used.

Writes to the Flash disk take longer than reads. This is due to the time taken by the Flash memory chip itself to write data into its memory cells.

When files are deleted the FFS driver does not immediately erase the corresponding Flash memory. Instead, it marks that memory as being “garbage”, and when the Flash memory approaches its capacity the FFS performs a garbage collection process, in which data which is still required is copied into a spare 64k byte sector, freeing another sector to be erased. The nature of the Flash memory is that it can only be erased in 64k byte sectors. The FFS driver thus has the task of allocating logical disk sectors to physical areas of Flash memory.

As a consequence of the garbage collection process, some writes will take longer than others, if they force the FFS to perform its garbage collection operation. This garbage collection process during Flash writes can increase write time by as much as sixty percent, as the number of garbage areas grow. This is described in detail on the Datalight Web site, at http://www.datalight.com/resource.asp .

The TP600 Support Material contains a garbage collection utility called FXRECLM.EXE. This utility can be used to force the FlashFX FFS to perform a garbage collection operation at any time, when executed. Placing an appropriate entry in autoexec.bat would force garbage collection each time the TP600 boots, helping to keep the flash array performance

higher than normal.

FXRECLM.EXE usage:

FXRECLM.EXE <drive> [<count>]

Where <drive> is the drive letter of the flash disk (e.g. C:), and

<count> is the number of successive garbage collection operations to perform on the flash disk. One garbage collection operation will reclaim one 64k sector of flash memory.

The FXRECLM.EXE utility stops the garbage collection process either when <count> has been reached or when there is no more flash memory to recover, whichever comes first.

For 2M bytes of Flash memory there are 32 sectors of 64k bytes each, four of which are reserved for system BIOS use. The remaining 28 sectors are available for flash disk use. Thus to perform garbage collection on all 28 64Kbyte sectors of flash disk memory use the FXRECLM.EXE utility as follows:

FXRECLM C: 28

6.6.4 Flash File System Statistics

The TP600 Support Material also contains a useful utility for reporting the status of the flash disk. It can be used to find out how much flash memory is available, has been used, and is recoverable through the garbage collection process.

FXINFO.EXE usage:

FXINFO.EXE <drive>

Where <drive> is the drive letter of the flash disk.

The FXINFO utility provides a detailed flash disk report, most of which is of little use to TP600 users. However the final section (an example of which is displayed below), is of use in determining flash memory usage, in particular the ‘Recoverable Space’, information.

The following is an extract from a typical FXINFO display:

Media Usage
Data Used : 61K
Free Space : 1796K
Recoverable Space : 33K

The recoverable space is the amount of memory that can be recovered through the garbage collection process. In the example above the recoverable space is reported at 33K bytes.

6.7 SAVING CMOS RAM DATA IN THE SERIAL EEPROM

A serial EEPROM chip on the TP600 provides non-volatile memory storage and also incorporates a watchdog timer. The non-volatile memory can be used to back-up the CMOS SRAM, in systems without batteries, or where the battery may go flat. The serial EEPROM chip used is the Xicor X5043. This chip contains 512 bytes of non-volatile serial EEPROM. The serial EEPROM is accessed through the Utility Register in the W83627 Super I/O chip.

The BIOS includes a feature that checks to see if the contents of the CMOS memory are valid during the boot sequence. If the CMOS memory does not have valid contents (since there was no battery back-up, for instance) then the BIOS will check whether the serial EEPROM contains valid CMOS data. If it does then the data in the serial EEPROM memory will be copied into the CMOS memory and used.

It is the responsibility of the user to program the serial EEPROM. A utility program is provided to do this. It is called TP3EE.EXE and is available in the TP600 Support Material. It should be run with the -C parameter, like this:

```
TP3EE -C
```

(Note that the TP3EE program has other uses - see sections 6.8 and 6.9).

The TP3EE program should be run once the CMOS memory contains valid data - after running the BIOS Setup program for instance. The contents of the CMOS registers are then copied into the serial EEPROM. These values will be returned to the CMOS memory by the BIOS if the CMOS memory contains invalid data during subsequent boot operations.

The CMOS SRAM consists of 256 locations split into two banks of 128. The first 10 locations store date and time information. The following 182 locations contain the BIOS. This leaves a quarter (64 locations) of the CMOS SRAM free.

When the TP3EE.EXE program is run all of the first 192 locations in the CMOS SRAM are copied to the EEPROM. This places both time and date information and the BIOS settings in the Serial EEPROM. A 2 byte checksum is then added immediately after the data. As the serial EEPROM is a 512-byte device there are 318 bytes remaining after this procedure.

During the restore process, when the contents of the serial EEPROM are copied back to the CMOS RAM, all 192 bytes are copied. This restores the time and date, the control registers and the memory locations containing data.

The BIOS makes use of all of the first 192 CMOS memory locations. As mentioned above there are a further 64 bytes of CMOS SRAM available, which can be accessed by setting the bank select bits in the W83627 Super I/O chip. This is discussed in the W83627 data book. Users who require additional SRAM may use the SRAM in other banks.

Although only the first 194 locations in the serial EEPROM are currently used by the BIOS to store the CMOS registers, DSP Design strongly recommends that 256 locations in the serial EEPROM up to and including address 0FFh are reserved for possible future BIOS use. This leaves a further 256 bytes in the serial EEPROM (at addresses 100h - 1FFh) available for users. Section 6.8 describes a program that can be used to read and write CMOS EEPROM locations.

6.8 SERIAL EEPROM PROGRAMMING

The X5043 serial EEPROM has 512 (200h) bytes on non-volatile memory. Section 6.7 describes using the serial EEPROM for saving CMOS RAM settings. Addresses 00h - BFh in the serial EEPROM are reserved for holding CMOS RAM data, addresses C0h and C1h contain a checksum for the CMOS data, and addresses C2h - 0FFH are reserved for future DSP Design use. Addresses 100h - 1FFh remain available for users.

The TP3EE.EXE program allows individual bytes in the EEPROM to be written and read. It also provides a way of testing the EEPROM, enabling and testing the watchdog timer, and copying the CMOS SRAM into the EEPROM. It has the following parameters:

-rxxx -r reads the data from the serial EEPROM at the address <xxx>, and displays it on the screen. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

-wxxx -w writes data into the serial EEPROM at the address defined by the <xxx> parameter. The data written is the hexadecimal byte specified by the -d parameter. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

-dxx -d defines the data value to be written to the serial EEPROM by the -w parameter. The xx parameter is a hexadecimal number in the range 0 - FFh.

-t -t tests the serial EEPROM, by writing to every location. The previous data is destroyed.

-c -c copies the contents of the CMOS SRAM into the serial EEPROM.

-s -s saves the contents of the serial EEPROM into a file on the current drive called TP3CMOS.DAT. All 512 bytes are saved. Together with the –p command this can be used to save and restore known CMOS memory configurations prior to putting TP600 systems into production.

-p -p programs the serial EEPROM with the contents of a file on the current drive called TP3CMOS.DAT. All 512 bytes are written. Together with the –s command this can be used to save and restore known CMOS memory configurations prior to putting TP600 systems into production.

-e -e enables the watchdog timer. The TP600 will be reset unless the watchdog is kicked (see the -k parameter). This is only used for testing purposes.

-kxxx -k kicks the watchdog timer for <xxx> seconds. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

-z Clears keyboard buffer at start of program.

6.9 WATCHDOG TIMER PROGRAMMING

The watchdog timer is contained within the serial EEPROM chip and is controlled through four pins of the Utility Register. Once it is enabled, the watchdog timer will reset the TP600 if it is not accessed (or “kicked”) regularly. It is up to the user to write code to enable and kick the watchdog timer. As an example, the source code of a watchdog timer test program is included in the TP600 Support Material. The test program is called TP3WDOG.EXE.

The TP3WDOG program has a number of command line options. These can be reviewed by executing the program with the following command-line:

TP3WDOG –H

Or:

TP3WDOG -?

or just:

TP3WDOG

To start the watchdog timer test type this:

TP3WDOG -T TP500 (you must include the spaces)

The program enables the watchdog timer, and kicks it regularly, until you type S (in which case the watchdog times out) or anything else, in which case the watchdog timer is disabled.

The general purpose serial EEPROM program, TP3EE.EXE, can also be used to test the watchdog timer - see section 6.9.

The watchdog timer is kicked by the toggling of its chip select pin (/CS), which is driven by the Utility Register bit 31. Users might consider taking the /CS pin low at one point in their program and taking it high again in a different point. This reduces the likelihood that a crashed program could end up executing a small loop that both set and cleared the /CS pin. Similarly, the watchdog accesses should not be part of a timer-based interrupt service routine, since a program could possibly crash and leave a timer interrupt correctly operating.

Care needs to be taken if power management software is to be used. Power management can slow down the processor clock, so that software loops will execute slowly. Thus the possibility exists that watchdog timer would time out unexpectedly.

6.10 LaunchPad APPLICATION DEVELOPMENT KITS

The LaunchPad products are a family of integrated hardware/software development kits for PC/104 computers and embedded operating systems. We've taken care of the tools so you can focus on your applications development.

The LaunchPad products will save significant amounts of development time for most users.

We have two objectives as you begin to use your new LaunchPad Development Kit.

Firstly, we expect that within an hour of receiving your LaunchPad you will have set up the hardware, connected it to your LAN and run the demonstration data acquisition application from a web browser.

Secondly, we expect that within a day you will have installed the development tools, compiled a sample application, downloaded it to the target hardware, and debugged this application remotely from the host computer.

So on the second day you can begin developing your real application.

For full details of the LaunchPad Development kits see our web site at www.dspdesign.com/launchpad. Ordering information is given in Appendix D.

(This page is intentionally blank)

APPENDIX A - SPECIFICATION

This is the specification of the TP600.

A.1 PRODUCT

TP600 Highly integrated PC-compatible single board computer in PC/104 form-factor.

A.2 PROCESSOR

AMD Geode LX800@0.9W x86 processor with CS5536 companion chip, clocked at 400MHz. Can be configured to operate at lower frequency for better power consumption or higher frequency for better performance.

A.3 MEMORY

A.3.1 DRAM

Single 200-pin SODIMM socket. Accepts DDR SODIMM modules, PC2100 or faster, typically 128M bytes, 256M bytes, 512M bytes or 1G bytes.

A.3.2 BIOS

Single 1M byte Flash chip, 32-pin PLCC socket.

A.3.3 Flash File System

Single 29F016 provides 2M byte FFS for DOS using a loadable device driver.

A.4 PERIPHERALS

A.4.1 Display

Display controller integral to Geode chipset. Analog VGA CRT and LCD monitors at up to 1280 x 1024. TFT displays of up to 1024 x 768, with up to 8 bits each of RGB. TFT interface includes signals to turn on and off LCD power and backlight.

A.4.2 USB

Two USB v1.1 ports. On-board current limiting chips limits current to approx 500mA. Two USB peripherals connected through an external connector/filter board, the dual-port TP300USB.

A.4.3 PS/2 Keyboard and Mouse

PS/2 keyboard and mouse ports provided.

A.4.4 Serial Ports

Four serial ports. COM1, COM2 and COM3 are full-function RS232 ports with 3 output signals and 5 input signals. COM2 can optionally be configured as a half-duplex or full-duplex RS485 port. These are accessed through 9-way D-type connectors on the board edge.

COM4 is transmit and receive data only, CMOS-level signals.

A.4.5 Parallel Port

PC compatible parallel port. Bi-directional. EPP and ECP compatible.

A.4.6 Disk Drives

Floppy Disk Controller drives single 3.5 inch floppy disk drive through 26-way flat flexible cable.

An IDE/ATA disk controller in the Geode chipset connects to a 44-way 2mm pin header. An optional CF100 adapter board can accept Compact Flash memory cards of any size for a solid-state disk drive.

USB floppy, CD-ROM and some memory stick disk drives can be used.

A.4.7 Ethernet

A 10/100Base-T Ethernet chip is provided, which is connected to the PCI bus for fast bus master data transfers. Connects to local area network via an external adapter board incorporating an RJ45 connector.

A.4.8 Sound

AC97 audio subsystem supports microphone in, line in and line out. PC beep circuit drives an external speaker (8-ohms or similar).

A.4.9 Analog to Digital Converter

Four channel, 12-bits. External reference. 0V to +5V input range.

A.5 PCI AND ISA EXPANSION

Up to four PCI-104 or PC/104-Plus expansion boards can be added to provide additional functionality. Only one card can use bus mastering (two if Ethernet is not used).

A.6 MISCELLANEOUS FUNCTIONS

A.6.1 Real-Time Clock

On-board real-time clock and CMOS SRAM for storing BIOS settings, using external battery. CMOS settings backed up by on-board serial EEPROM.

A.6.2 Reset Circuit

Power supply monitor holds board reset until power supplies are stable. External reset switch or signal may reset the TP600.

A.6.3 Test and Development

A number of functions are present on the board for test and development use and possible future expansion. DSP Design does not provide support for these functions at present. The functions include: JTAG test port and LPC bus expansion.

A.7 MECHANICAL

A.7.1 PC/104 Form factor

PC/104 form-factor.

A.7.2 Dimensions

PCB - 3.550 inches * 3.775 inches, (90mm * 96mm approx.).

Overall dimensions including connectors, 4.250 inches * 3.830 inches * 0.960 inches, (108mm * 96mm * 26mm approx.).

Maximum height on the component side of the PCB is 0.47 inches (12mm), measured from top surface of lower PCB (heights exclude heatsink/fan).

A.7.3 Weight:

128g (excluding DRAM and heatsink).

A.8 POWER SUPPLY

Single +5V +/- 5%. Power inlet is by a 4-pin pin header or the PC/104 bus. Typical power consumption figures for the TP600 are between 6W and 7W under Windows XP Embedded, and vary depending on activity. These do not include figures for a display or other peripherals.

A.9 ENVIRONMENTAL

A.9.1 Operating Temperature

0 – 55 degrees Celsius when using the DSP-TG533HS passive heatsink.

0 – 70 degrees Celsius can be achieved using an active heatsink / fan assembly.

Ultimately cooling is a system design issue, and it is the responsibility of the system design engineer to select an appropriate heatsink or fan.

A.9.2 Humidity

10% - 90% non-condensing.

APPENDIX B - CONFIGURATION INFORMATION

This appendix describes fitting SDRAM to the TP600, and solder link settings.

The component placement diagrams in Appendix C may be of help in locating the solder links referred to in this appendix.

B.1 PROCESSOR COOLING

The TP600 dissipates approximately 7W, most of which is generated in the processor. Some cooling should be provided, or the processor may overheat. DSP Design can provide a passive heatsink, which may be useful in ambient temperatures of up to 55ºC. Ultimately cooling is a system design issue, and must remain the responsibility of the system design engineer.

Heatsinks should be mounted with a thermal grease or similar to ensure good thermal contact. The passive heatsink listed in Appendix D comes with a square of double-sided adhesive material, with an aluminium substrate. This both provides good thermal contact and also mechanically secures the heatsink.

The TP600 provides four mounting holes surrounding the BGA processor which can be used to secure more substantial heatsinks or fans. Figure C5 shows the mechanical arrangement of these holes.

B.2 SDRAM CONFIGURATION

The TP600 uses 200-pin DDR SODIMM SDRAM modules for memory. The standard TP600 product is delivered as standard with no SDRAM modules fitted. Users may buy SODIMM modules from DSP Design or fit their own. DSP Design carry stock of the SODIMM modules. These modules have been selected to operate correctly with the TP600.

SODIMM speed grade should be chosen to suit the memory clock speed. See Table 2. Appendix D lists the DSP Design part numbers for various memory sizes.

Install your SDRAM SODIMM module in the TP600 SDRAM socket, observing its polarity, and observing proper anti-static precautions. The SODIMM socket has a lug that engages with a cut-out on the module, which prevents incorrect installation.

B.3 SOLDER LINK AREAS

A number of functions can be configured with solder links on the TP600 board. The board layout is so dense we have implemented these configuration options with solder links that take less space than jumpers, as well as being more reliable.

Care must be taken when changing these link areas so that no accidental shorts are produced or created. Default settings are noted below.

B.3.1 LK1 – ADC0 or LINE_IN_R

This link determines whether connector J6 pin 2 is used for the analog to digital converter channel 0 input, or the audio codec Line In Right input.

Pin 2 is A/D converter ADC0: Link 2 - 3

Pin 2 is audio codec Line In Right input: Link 1 - 2 (default)

B.3.2 LK2 – ADC1 or LINE_IN_L

This link determines whether connector J6 pin 4 is used for the analog to digital converter channel 1 input, or the audio codec Line In Left input.

Pin 4 is A/D converter ADC1: Link 2 - 3

Pin 4 is audio codec Line In Left input: Link 1 - 2 (default)

B.3.3 LK3 – ADC2 or LINE_OUT_R

This link deermines whether connector J6 pin 6 is used for the analog to digital converter channel 2 input, or the audio codec Line Out Right output.

Pin 6 is A/D converter ADC2: Link 2 - 3

Pin 6 is audio codec Line Out Right output: Link 1 - 2 (default)

B.3.4 LK4 – ADC3 or LINE_OUT_L

This link determines whether connector J6 pin 8 is used for the analog to digital converter channel 3 input, or the audio codec Line Out Left input.

Pin 8 is A/D converter ADC3: Link 2 - 3

Pin 8 is audio codec Line Out Left output: Link 1 - 2 (default)

B.3.5 LK5 – A/D Converter Reference

This link is used to select the source of the VREF input voltage to the analog to digital converter. Note that when the link is fitted the on-board +5V power supply is not only connected to the A/D converter VREF pin, but is also taken out to the VREF pin on connector J6 (provided that LK6 is also fitted)

VREF is supplied by on-board +5V: Fit Link (default).

VREF is supplied from an external source via J6: Omit Link.

B.3.6 LK6 – VREF or Microphone

This link determines whether connector J6 pin 1 is used for the analog to digital converter VREF input or output, or the audio codec microphone input. See also LK12.

Pin 1 is A/D converter VREF:	Fit link
Pin 1 is audio codec microphone input:	Omit link (default)

B.3.7 LK7, LK8, LK9, LK10 – RS485 Isolation

These links connect the COM2 RS485 transceiver chip to the J4 connector.

To use RS485: fit links

To use RS232: omit links (default).

B.3.8 LK11 - COM2 RS-232/RS-485 Selection

This link is used to select whether COM2 is RS-232 or RS-485.

RS-232:	No link installed. (Default setting)
RS-485:	Link installed.

B.3.9 LK12 – VREF or Microphone

This link determines whether connector J6 pin 1 is used for the analog to digital converter VREF input or output, or the audio codec microphone input. See also LK6.

Pin 1 is A/D converter VREF:	Omit Link.
Pin 1 is audio codec microphone input:	Fit link (default)

B.3.10 LK200 – IDE CBLID Emulation

This link determines the source of the CBLID signal, which connects to the CS5536 GPIO5 pin. This is related to the emulation of 80-way ribbon cables which are used on high-speed UDMA disk drives. The presence of an 80-way cable is an indication that higher speed UDMA operation may occur.

In normal PC systems a pull-up resistor on the disk drive pulls the CBLID signal high. When an 80-way cable is installed the cable pulls CBLID to GND.

On the TP600 there is no possibility of fitting an 80way cable, so if the CBLID signal is to be pulled low then this must be done with solder link LK200.

To leave CBLID pulled high, leave LK200 not fitted (default)

To drive CBLID from J100 pin 34: link 1-2

To pull CBLID low: link 2-3

B.3.11 LK201 – A/D Converter Input ADC3

This link is used to connect the analog to digital converter input ADC3 to the on-board temperature sensor.

ADC3 is connected to on-board temperature sensor: Install link (Default)

ADC3 may be supplied externally: Omit link.

B.3.12 LK202 – Ethernet Transformer CT Voltage

There are two options for the voltage available on connector J106 pin 3 . For use with the TP400ET, which has a 5V to 3.3V regulator, +5V should be used. When connecting directly to the transformer centre tap, +3.3V should be used.

+3.3V: Link 1-2

+5V: Link 2 - 3 (Default)

Note that the +5V option is a switched 5V which is only applied when the +3.3V rail is on. This ensures that backpowering of the +3.3V rail will not occur.

B.3.13 LK203 and LK204 – Ethernet PCI Bus Request/Grant

These allows the Ethernet controller chip to be disconnected from the PCI bus request and bus grant signals (REQ0# and GNT0#). By disconnecting the Ethernet chip from these signals, when it is not being used, the REQ0# and GNT0# signals become available for other PCI bus masters on PC/104-Plus boards.

Ethernet chip uses REQ0#/GNT0#: Link LK203 and LK204 (Default)

Ethernet chip does not use REQ0#/GNT0#: Omit link LK203 and LK204

B.3.14 LK205 – LK209 – Processor and Memory Clock Speed

These five links set the Geode processor and memory clock speeds. They are normally factory set and need not be changed. However, users may want to reduce the processor or memory clock speeds to reduce power consumption or increase speeds for better performance. Note that by default the TP600 is fitted with an LX800 @ 0.9W which has a maximum clock speed of 500MHz, so faster clock settings should not be attempted. The default setting is shown in grey.

CPU CLOCK	SDRAM TX RATE	SDRAM CLOCK	PC-XXXX	LK208	LK207	LK206	LK209	LK205
RSVD	RSVD	RSVD	-	Link 2-3	Link 2-3	Link 2-3	Link 2-3	Link 2-3
166MHz	166MHz	83MHz	PC2100	Link 2-3	Link 2-3	Link 2-3	Link 2-3	Link 1-2
200MHz	200MHz	100MHz	PC2100	Link 2-3	Link 2-3	Link 2-3	Link 1-2	Link 2-3
266MHz	200MHz	100MHz	PC2100	Link 2-3	Link 2-3	Link 2-3	Link 1-2	Link 1-2
266MHz	266MHz	133MHz	PC2100	Link 2-3	Link 2-3	Link 1-2	Link 2-3	Link 2-3
333MHz	200MHz	100MHz	PC2100	Link 2-3	Link 2-3	Link 1-2	Link 2-3	Link 1-2
333MHz	266MHz	133MHz	PC2100	Link 2-3	Link 2-3	Link 1-2	Link 1-2	Link 2-3
333MHz	333MHZ	166MHz	PC2700	Link 2-3	Link 2-3	Link 1-2	Link 1-2	Link 1-2
366MHz	200MHz	100MHz	PC2100	Link 2-3	Link 1-2	Link 2-3	Link 2-3	Link 2-3
366MHz	266MHz	133MHz	PC2100	Link 2-3	Link 1-2	Link 2-3	Link 2-3	Link 1-2
366MHz	333MHZ	166MHz	PC2700	Link 2-3	Link 1-2	Link 2-3	Link 1-2	Link 2-3
400MHz	200MHz	100MHz	PC2100	Link 2-3	Link 1-2	Link 2-3	Link 1-2	Link 1-2
400MHz	266MHz	133MHz	PC2100	Link 2-3	Link 1-2	Link 1-2	Link 2-3	Link 2-3
400MHz	333MHz	166MHz	PC2700	Link 2-3	Link 1-2	Link 1-2	Link 2-3	Link 1-2
400MHz	400MHz	200MHz	PC3200	Link 2-3	Link 1-2	Link 1-2	Link 1-2	Link 2-3
433MHz	266MHz	133MHz	PC2100	Link 2-3	Link 1-2	Link 1-2	Link 1-2	Link 1-2
433MHz	333MHZ	166MHz	PC2700	Link 1-2	Link 2-3	Link 2-3	Link 2-3	Link 2-3
433MHz	400MHz	200MHz	PC3200	Link 1-2	Link 2-3	Link 2-3	Link 2-3	Link 1-2
466MHz	266MHz	133MHz	PC2100	Link 1-2	Link 2-3	Link 2-3	Link 1-2	Link 2-3
466MHz	333MHZ	166MHz	PC2700	Link 1-2	Link 2-3	Link 2-3	Link 1-2	Link 1-2
466MHz	400MHz	200MHz	PC3200	Link 1-2	Link 2-3	Link 1-2	Link 2-3	Link 2-3
500MHz	266MHz	133MHz	PC2100	Link 1-2	Link 2-3	Link 1-2	Link 2-3	Link 1-2
500MHz	333MHZ	166MHz	PC2700	Link 1-2	Link 2-3	Link 1-2	Link 1-2	Link 2-3
500MHz	400MHz	200MHz	PC3200	Link 1-2	Link 2-3	Link 1-2	Link 1-2	Link 1-2
533MHz	266MHz	133MHz	PC2100	Link 1-2	Link 1-2	Link 2-3	Link 2-3	Link 2-3
533MHz	333MHZ	166MHz	PC2700	Link 1-2	Link 1-2	Link 2-3	Link 2-3	Link 1-2
533MHz	400MHz	200MHz	PC3200	Link 1-2	Link 1-2	Link 2-3	Link 1-2	Link 2-3
600MHz	200MHz	100MHz	PC2100	Link 1-2	Link 1-2	Link 2-3	Link 1-2	Link 1-2
566MHz	333MHZ	166MHz	PC2700	Link 1-2	Link 1-2	Link 1-2	Link 2-3	Link 2-3
566MHz	400MHz	200MHz	PC3200	Link 1-2	Link 1-2	Link 1-2	Link 2-3	Link 1-2
600MHz	333MHZ	166MHz	PC2700	Link 1-2	Link 1-2	Link 1-2	Link 1-2	Link 2-3
600MHz	400MHz	200MHz	PC3200	Link 1-2	Link 1-2	Link 1-2	Link 1-2	Link 1-2

TABLE B1 - PROCESSOR AND MEMORY CLOCK SPEEDS

(This page is intentionally blank.)

APPENDIX C - MECHANICAL DRAWINGS

This appendix contains component placement drawings for both boards. These may be of assistance in locating components, connectors and solder links. The appendix also contains mechanical drawings of both boards.

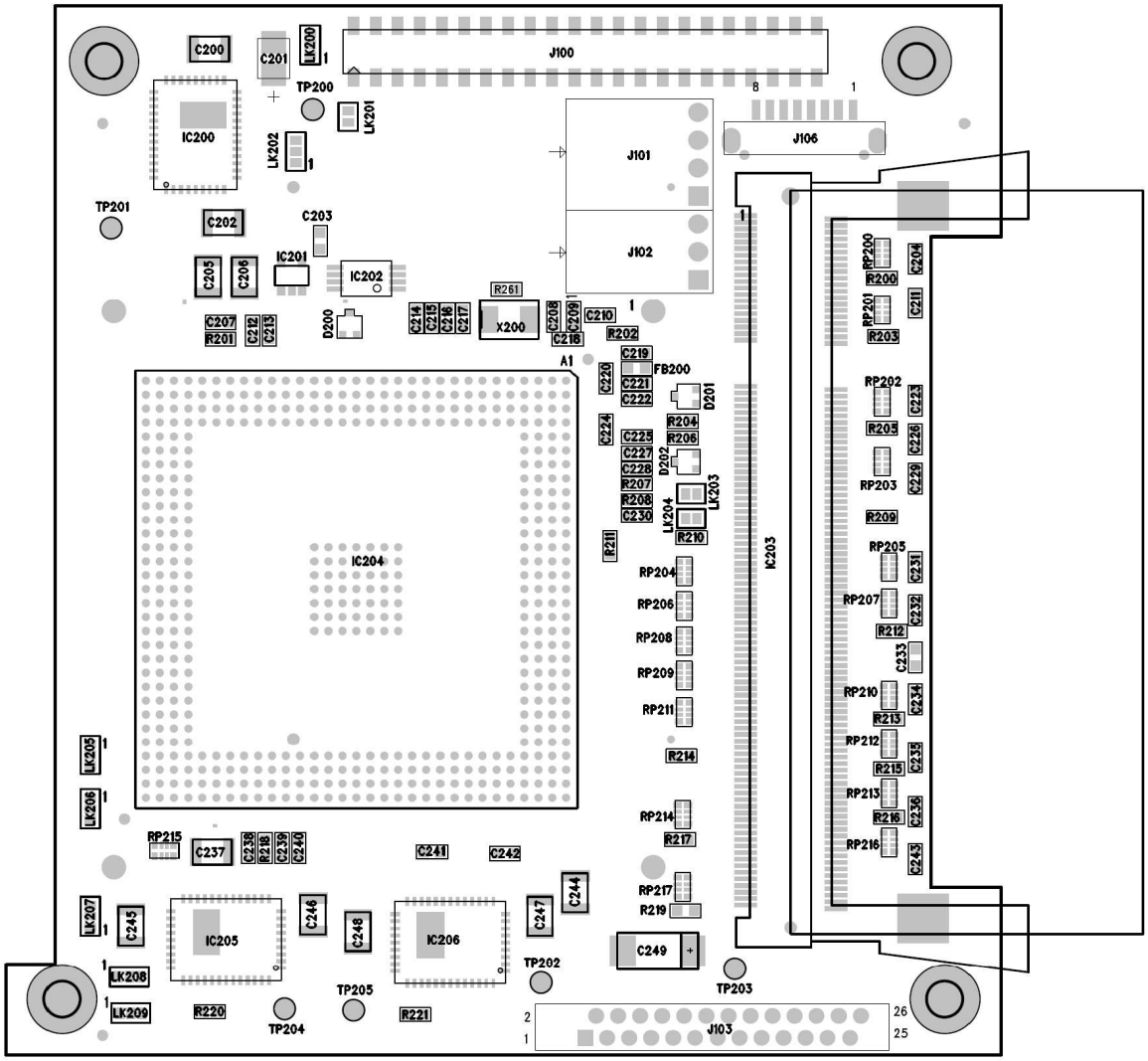


FIGURE C1 - TOP BOARD, TOP SIDE COMPONENT PLACEMENT

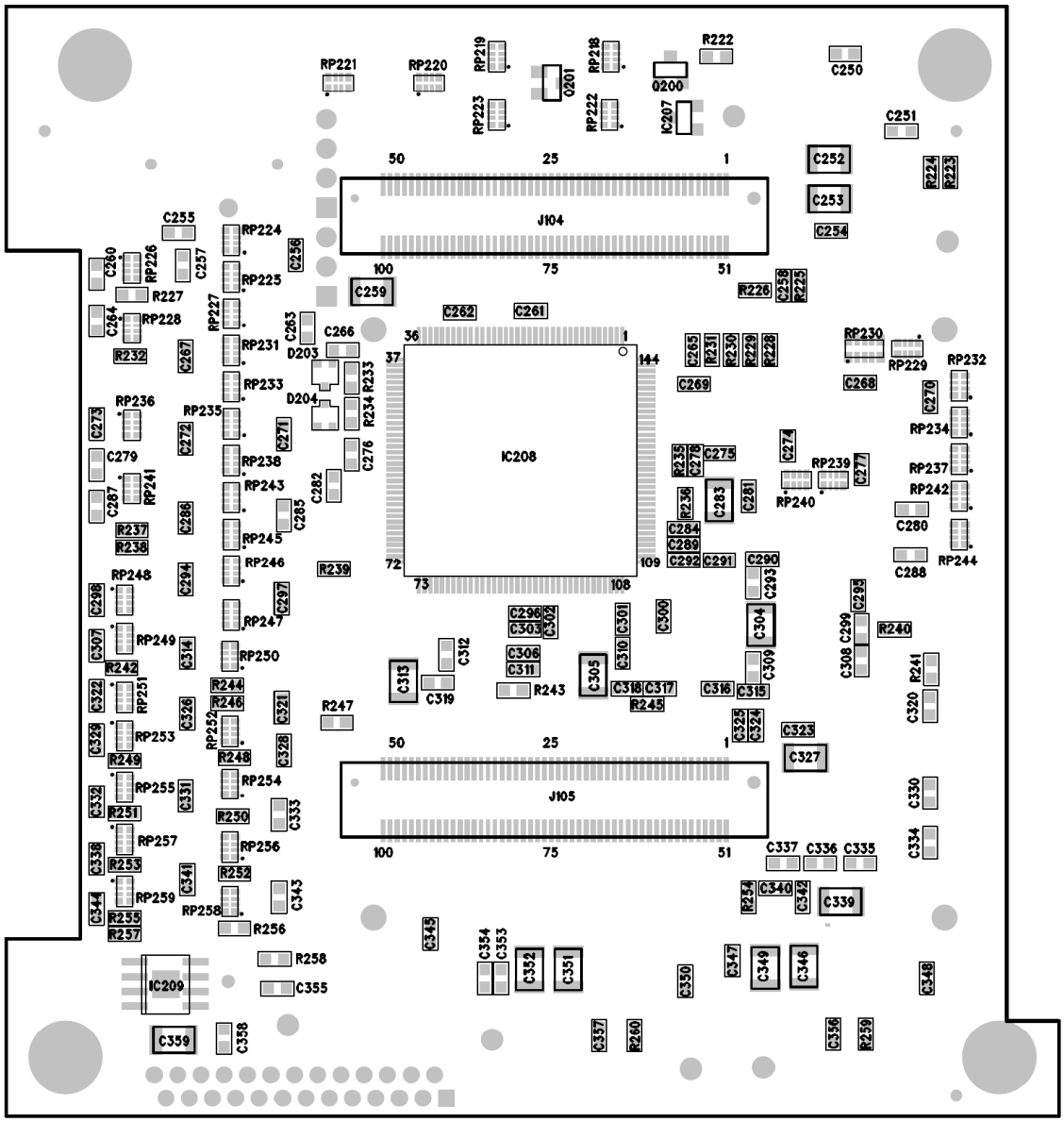


FIGURE C2 - TOP BOARD, BOTTOM SIDE COMPONENT PLACEMENT

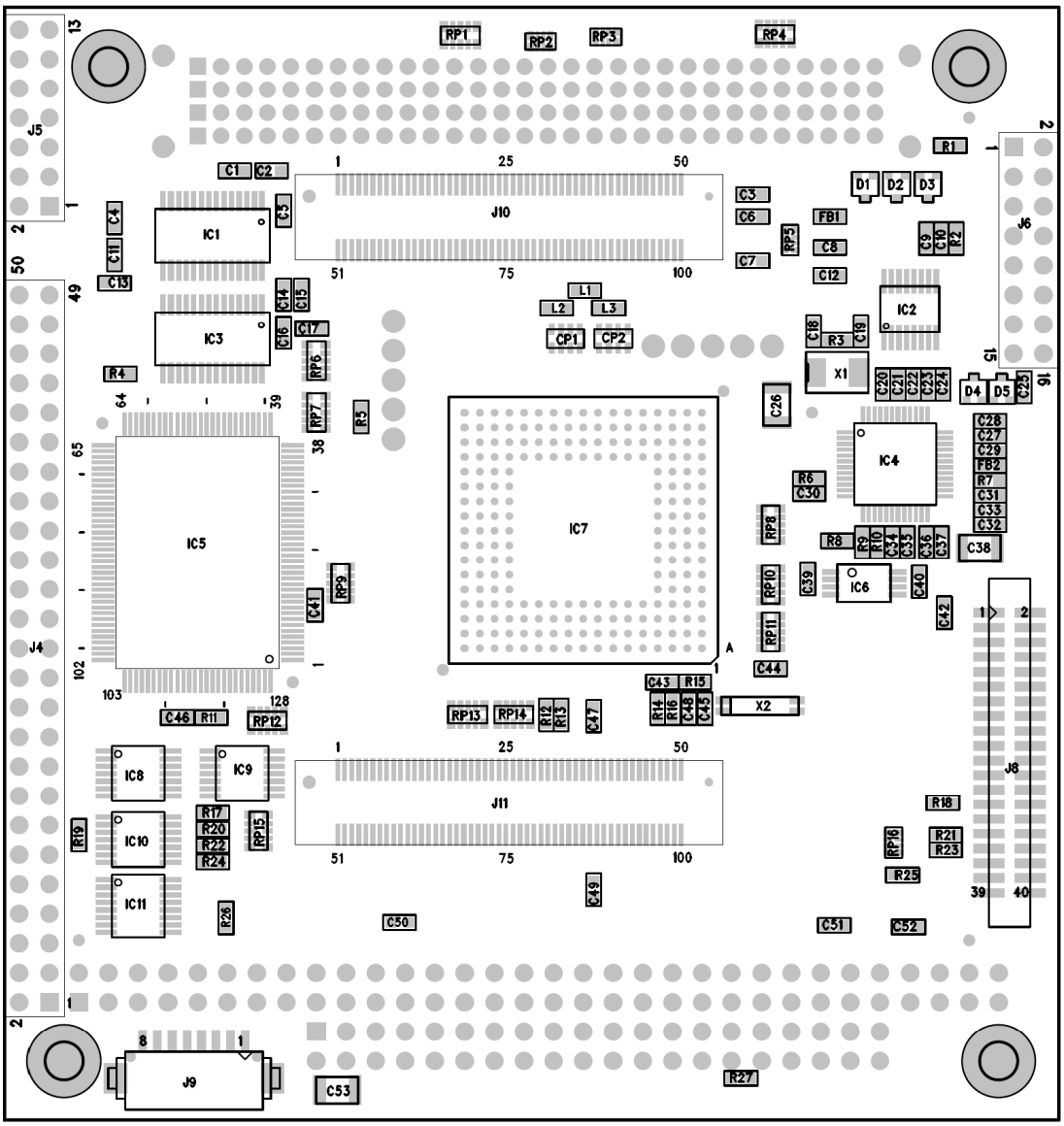


FIGURE C3 - BOTTOM BOARD, TOP SIDE COMPONENT PLACEMENT

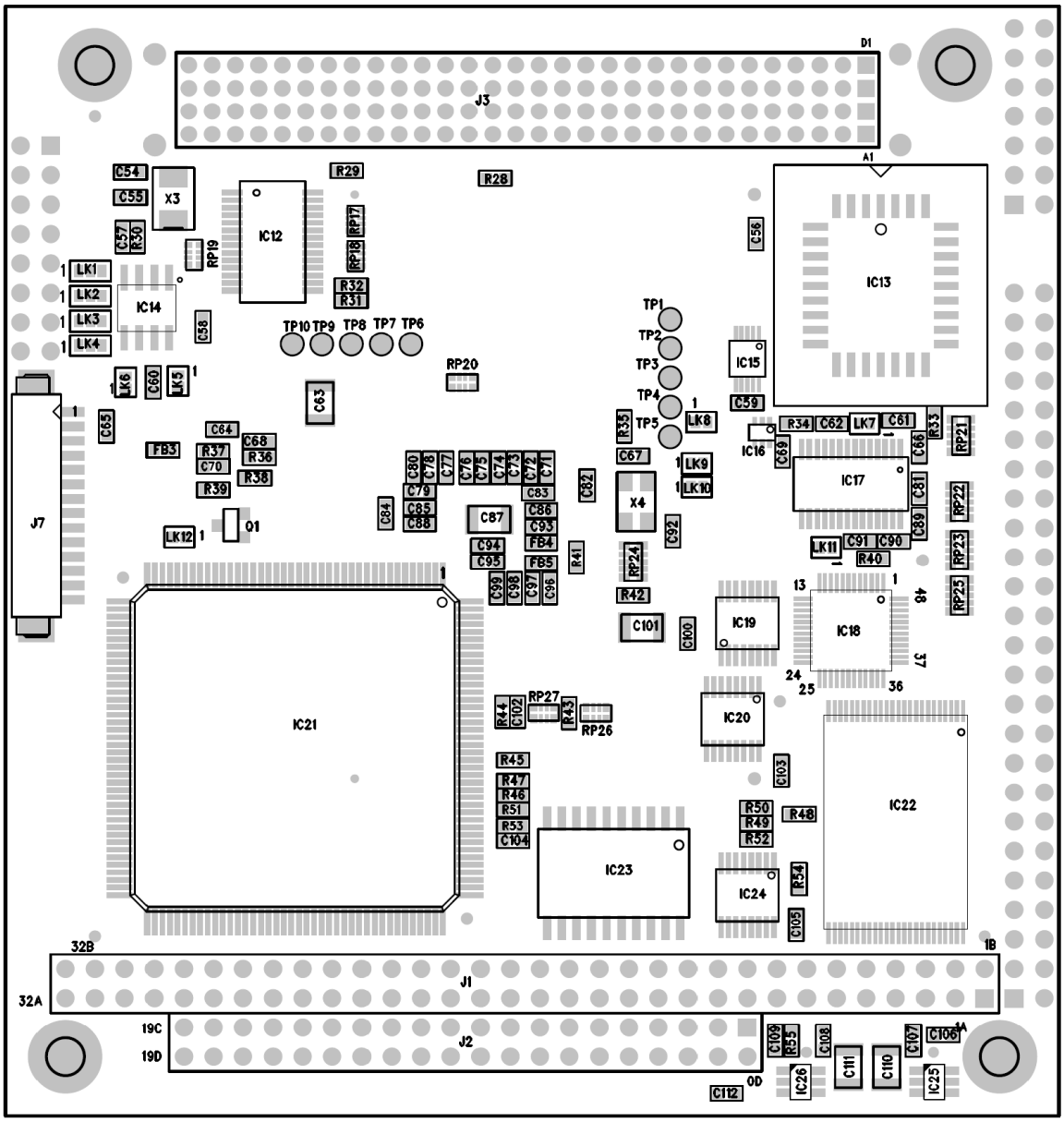


FIGURE C4 - BOTTOM BOARD, BOTTOM SIDE COMPONENT PLACEMENT

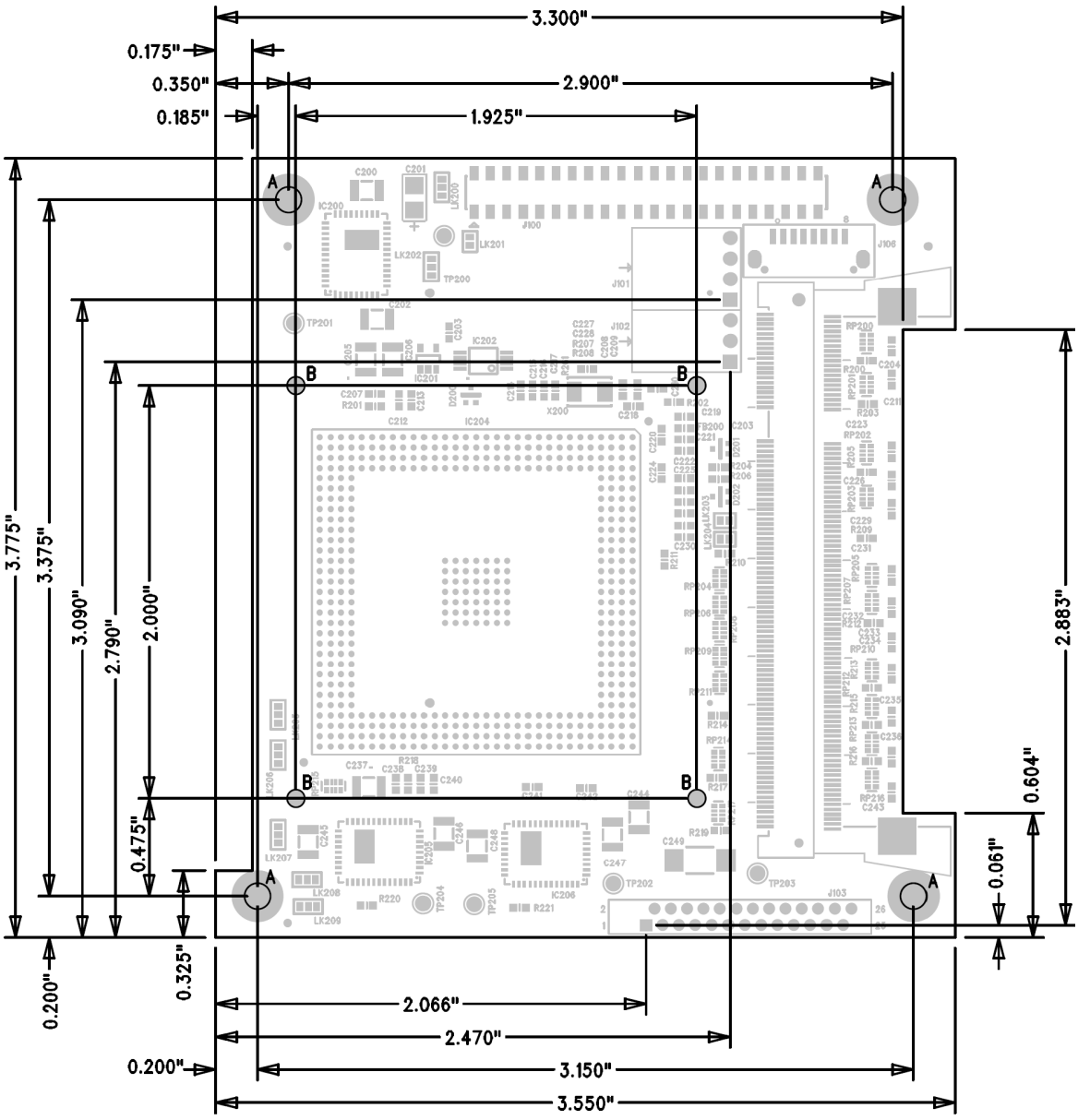
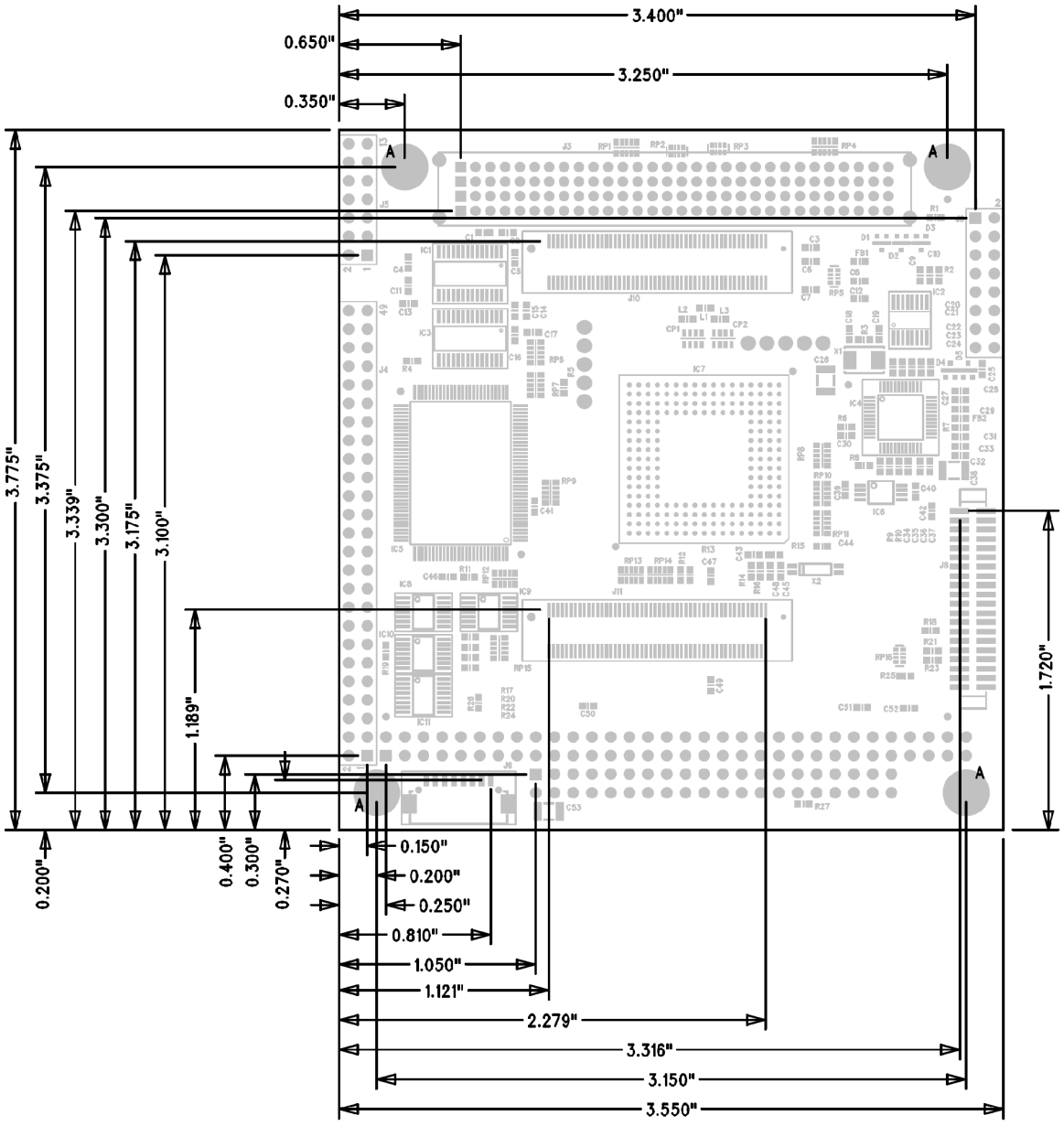


FIGURE C5 - TOP BOARD, MECHANICAL DRAWING



4 x "A" HOLES = 3.2mm +/−0.05mm

FIGURE C6 - BOTTOM BOARD, MECHANICAL DRAWING

APPENDIX D - ORDERING INFORMATION

This Appendix lists some of the range of PC/104 products available from DSP Design, and in particular the products related to the TP600. Note that as new products are being released all the time this list may not be complete. Contact DSP Design for up to date information.

D.1 PROCESSOR BOARDS

Table D1 lists the processor options. These are available with or without operating system licences (the licenced boards include the operating system licence label attached).

ITEM	DESCRIPTION
DSP-TP600	Standard TP600 processor board, with LX800 processor and without SDRAM.

TABLE D1 - PROCESSOR BOARDS

D.2 SDRAM MEMORY MODULES

Table D2 lists the SDRAM options. The TP600 is shipped without SDRAM so that you can choose the memory capacity that you require – use a single DDR module to a maximum of 1GB.

ITEM	DESCRIPTION
DSP-DDR128	128M byte DDR SODIMM SDRAM module
DSP-DDR256	256M byte DDR SODIMM SDRAM module
DSP-DDR512	512M byte DDR SODIMM SDRAM module
DSP-DDR1G	1G byte DDR SODIMM SDRAM module

TABLE D2 - SDRAM MEMORY MODULES

D.3 LAUNCHPAD APPLICATION DEVELOPMENT KITS

The best way of starting a TP600 development project is to buy a LaunchPad; DSP-LP600CE, part of a family of “LaunchPad” products. Each LaunchPad product includes the processor itself, connectivity, power supply and a comprehensive set of manuals, disks and cable assemblies optimized to that particular processor. The LaunchPad products provide most customers with all that they need for their development process, but there are still other accessories that may be of use, and these will need to be ordered separately.

You may also want to order a TFTIF board and LCD cable assembly, and other accessories from the lists in section D.4 and D.5.

The LaunchPad products are a family of integrated hardware/software development kits for PC/104 computers and embedded operating systems. The LaunchPad products will save significant amounts of development time for most users.

There are LaunchPad Development Kits for all the processors developed by DSP Design for several operating systems. For full details of the LaunchPad product range and a list of available LaunchPads for TP600 see our web site at www.dspdesign.com/launchpad.htm.

D.4 DISPLAY ACCESSORIES

Table D3 lists some accessories related to LCD displays.

ITEM	DESCRIPTION
DSP-TFTIF31	Display adapter board - plugs into Sharp 640 x 480 TFT displays (and others with compatible pin assignments) and accepts input from TP600.
DSP-TFTIF41	Display adapter board - plugs into Sharp 800 x 600 TFT displays and some 1024 x 768 displays (and others with compatible pin assignments) and accepts input from TP600.
DSP-TFTIFKYV	Display adapter board – Interfaces a variety of Kyocera displays with the TP600.
DSP-TFTIF-CAB11	40-way cable assembly for TFTIFxx boards, connector at both ends, length 11 inches.
DSP-TFTIF-CAB7	40-way cable assembly for TFTIFxx boards, connector at both ends, length 7 inches.

TABLE D3 - TP600 DISPLAY ACCESSORIES

D.5 OTHER ACCESSORIES

Table D4 lists items that may be of use during your development process, or in production.

ITEM	DESCRIPTION
TP600-UTILS	Support Material (sample software, drivers, data sheets etc.). Available as a download from the DSP Design website.
TRM-TP600	Technical Reference Manual for TP600.
DSP-TP400ET	Ethernet adapter board for TP600
DSP-TP300USB	USB adapter board for TP600
DSP-TB486ET-CAB	Cable assembly to connect TP600 Ethernet and USB connectors to the TP400ET or TP300USB.
DSP-TG533HS10	Heatsink and thermally conductive doubled-sided adhesive tape, to attach to the processor.
DSP-TCONN	Connector breakout PCB for TP600. Standard PC connectors for keyboard, mouse, 3 x serial, printer, VGA, power inlet. With EMC filtering.
DSP-TCONN-PSU	Mains power supply for TCONN. 5V, 2.5A output.
ROMDOS7	Datalight ROM-DOS 7.1 Operating System supplied on disk.

TABLE D4 - OTHER ACCESSORIES

D.6 CF100 COMPACT FLASH IDE

Compact Flash cards are a useful alternative to IDE drives and floppy disks during development. They are reasonably high capacity. You can read and write Compact Flash disks on PCs equipped with PCMCIA sockets on laptop computers (using an adapter), or with USB Compact Flash readers.

The Compact Flash card market is evolving rapidly with larger capacity devices becoming available.

ITEM	DESCRIPTION
DSP-CF100	Adapter board allowing Compact Flash cards to be used as an IDE drive.
DSP-CFWDC128	128M byte Compact Flash memory card
DSP-CFWDC256	256M byte Compact Flash memory card
DSP-CFWDC512	512M byte Compact Flash memory card
DSP-CFWDC01G	1G byte Compact Flash memory card
DSP-CFWDC02G	2G byte Compact Flash memory card
DSP-CF100-IDECA	Optional IDE cable to connect the CF100 to the TP600. Length 120mm.

TABLE D5 - COMPACT FLASH ACCESSORIES

APPENDIX E - CONNECTOR PIN ASSIGNMENTS

This appendix provides pin assignments of the connectors used on the TP600.

E.1 SUMMARY OF CONNECTORS

Table E1 summarises the connectors used on the TP600. Later tables provide the pin assignments of these connectors.

CONNECTOR	TYPE	USE
J1	64-way (2x32) pin header	PC/104 bus (8-bit data bus)
J2	40-way (2x20) pin header	PC/104 bus (16-bit data bus)
J3	120-way female header	PC/104-Plus connector (PCI bus signals)
J4	50-way (2x25) right-angled pin header	I/O
J5	14-way (2x7) right-angled pin header	I/O (COM3 and COM4)
J6	16-way (2x8) right-angled pin header	I/O (CRT, audio and A/D)
J7	14-pin SIL header	Test connector - JTAG, LPC bus
J8	40-way 0.05” pitch pin header	TFT panels
J9	8-way right-angled Hirose DF13 socket	USB
J10	100-way Hirose FX8 connector	Inter-board signals
J11	100-way Hirose FX8 connector	Inter-board signals

TABLE E1 - SUMMARY OF CONNECTORS: BOTTOM BOARD

CONNECTOR	TYPE	USE
J100	44-way (2x22) pin header, 2mm	IDE
J101	4-pin right-angled pin header	Power In
J102	3-pin right-angled pin header	Fan
J103	26-way flat flexible cable	Floppy disk
J104	100-way Hirose FX8 connector	Inter-board signals
J105	100-way Hirose FX8 connector	Inter-board signals
J106	8-way straight Hirose DF13 socket	Ethernet

TABLE E2 - SUMMARY OF CONNECTORS: TOP BOARD

E.2 PC/104 CONNECTORS J1 AND J2

The PC/104 bus connectors J1 and J2 provide the ISA bus compatible signals. The pin assignments for these connectors are shown in Table E4 and E3 respectively. The PC/104-Plus connector J3 provides the PCI compatible signals. The pin assignments for this connector are shown in Table E5.

Note that a number of PC/104 signals are not implemented on the TP600. These are principally DMA signals. The tables below note the actual connection, with the standard signal name in parentheses.

PIN	J2 ROW C	J2 ROW D
0	0V	0V
1	/SBHE	/MEMCS16
2	SA23	/IOCS16
3	SA22	Reserved
4	SA21	Reserved
5	SA20	Reserved
6	SA19	Reserved
7	SA18	Reserved
8	SA17	Pull-up resistor (/DACK0)
9	/MEMR	N/C (DRQ0)
10	/MEMW	Pull-up resistor (/DACK5)
11	SD8	N/C (DRQ5)
12	SD9	Pull-up resistor (/DACK6)
13	SD10	N/C (DRQ6)
14	SD11	Pull-up resistor (/DACK7)
15	SD12	N/C (DRQ7)
16	SD13	+5V
17	SD14	N/C (/MASTER)
18	SD15	0V
19	N/C - KEY	0V

TABLE E3 - PC/104 J2 PIN ASSIGNMENTS

PIN	J1 ROW A	J1 ROW B
1	/IOCHCHK	0V
2	SD7	RESETDRV
3	SD6	+5V
4	SD5	IRQ9
5	SD4	N/C (-5V)
6	SD3	N/C (DRQ2)
7	SD2	N/C (-12V)
8	SD1	/ZEROWS
9	SD0	N/C (+12V)
10	IOCHRDY	(KEY)
11	AEN	/SMEMW
12	SA19	/SMEMR
13	SA18	/IOWR
14	SA17	/IORD
15	SA16	Pull-up resistor (/DACK3)
16	SA15	N/C (DRQ3
17	SA14	Pull-up resistor (/DACK1)
18	SA13	N/C (DRQ1)
19	SA12	/REFRESH
20	SA11	BUSCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	Pull-up resistor (/DACK2)
27	SA4	Pull-up resistor (TC)
28	SA3	ALE
29	SA2	+5V
30	SA1	OSC
31	SA0	0V
32	0V	0V

TABLE E4 - PC/104 J1 PIN ASSIGNMENTS

E.3 PCI CONNECTOR J3

This is a 120-pin connector (4 rows of 30 pins each) on 2mm pitch. It complies with the PC/104-Plus and PCI-104 specifications. Table E5 gives its pin assignments.

PIN	ROW A	ROW B	ROW C	ROW D
1	GND	N/C (Reserved)	VCC	AD0
2	VCC3V (VI/O)	AD2	AD1	VCC
3	AD5	GND	AD4	AD3
4	C/BE0#	AD7	GND	AD6
5	GND	AD9	AD8	GND
6	AD11	VCC3V (VI/O)	AD10	GND (M66EN)
7	AD14	AD13	GND	AD12
8	VCC3V	C/BE1#	AD15	VCC3V
9	SERR#	GND	N/C (Reserved)	PAR
10	GND	PERR#	VCC3V	N/C (Reserved)
11	STOP#	VCC3V	LOCK#	GND
12	VCC3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	VCC3V
14	GND	AD16	VCC3V	C/BE2#
15	AD18	VCC3V	AD17	GND
16	AD21	AD20	GND	AD19
17	VCC3V	AD23	AD22	VCC3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VCC3V	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	VCC	AD28	AD27
22	VCC	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VCC3V (VI/O)
24	GND	REQ0# (REQ2#)	VCC	GNT0#
25	GNT1#	VCC3V (VI/O)	GNT0# (GNT2#)	GND
26	VCC	CLK0	GND	CLK1
27	CLK2	VCC	CLK3	GND
28	GND	INTD#	VCC	PCIRST#
29	N/C (+12V)	INTA#	INTB#	INTC#
30	N/C (-12V)	N/C (REQ3#)	Pull-up resistor (GNT3#)	GND

TABLE E5 - PC/104-PLUS CONNECTOR J3

E.4 PERIPHERAL CONNECTOR J4

Many peripheral devices are connected to the TP600 through a 50 way IDC connector, called J4. The 50 pins on the connector are brought to the outside world through a 50-way 0.1 inch IDC right-angled connector.

The J4 connector pin assignments are identical on all DSP Design PC/104 processor boards.

Table E7 lists the J4 signal name and also the peripheral to which the signal belongs and the pin number of that peripheral's connector. The standard connectors used in PC's for each of the peripherals are:

Centronics Printer: 25 way female D-type

Keyboard: 6 pin mini DIN (PS/2 style)

Mouse: 6 pin mini DIN (PS/2 style)

Serial COM1: 9 way male D-type

Serial COM2: 9 way male D-type

Loudspeaker: N/A

Battery: N/A

Reset Switch: N/A

Table E6 shows how J4 pins change function when COM2 is used for RS-485 operation.

RS-485 SIGNAL	RS-232 SIGNAL	J4 PIN
Transmit, inverting	DTR2	35
Transmit, non-inverting	CTS2	36
Receive, inverting	TXD2	37
Receive, non-inverting	RTS2	38

TABLE E6 - RS485 FUNCTIONS OF THE COM2 SIGNALS

Pin 1 of the J4 connector can be identified by looking at the J4 silk-screen box that surrounds the J4 connector on the TP600. A “1” and “2” are located close to the pin 1 end of J4 and a “49” and “50” are placed close to the pin 50 end. All odd numbered pins are in one row and all even numbered pins are in the other row.

PIN	SIGNAL	PERIPHERAL		PIN	SIGNAL	PERIPHERAL	
		NAME	PIN			NAME	PIN
1	IRRX	IrDA	-	2	IRTX	IrDA	-
3	MCLOCK	MOUSE	5	4	MDATA	MOUSE	1
5	SLCT	PRINTER	13	6	PE	PRINTER	12
7	BUSY	PRINTER	11	8	/ACK	PRINTER	10
9	PD7	PRINTER	9	10	PD6	PRINTER	8
11	PD5	PRINTER	7	12	PD4	PRINTER	6
13	GND	PRINTER	*	14	PD3	PRINTER	5
15	/SLCTIN	PRINTER	17	16	PD2	PRINTER	4
17	/INIT	PRINTER	16	18	PD1	PRINTER	3
19	/ERROR	PRINTER	15	20	PD0	PRINTER	2
21	/AUTOFD	PRINTER	14	22	/STROBE	PRINTER	1
23	GND	RESET SWITCH		24	/RESET	RESET SWITCH	
25	VCC (+5V)	SPEAKER		26	SPKR	SPEAKER	
27	GND	BATTERY	-	28	BATT	BATTERY	-
29	VCC (+5V)	KEYBOARD	4	30	KBDATA	KEYBOARD	1
31	GND	KEYBOARD	3	32	KBCLK	KEYBOARD	5
33	GND	COM2	5	34	RI2	COM2	9
35	DTR2 or RS485 **	COM2	4	36	CTS2 or RS485 **	COM2	8
37	TXD2 or RS485 **	COM2	3	38	RTS2 or RS485 **	COM2	7
39	RXD2	COM2	2	40	DSR2	COM2	6
41	DCD2	COM2	1	42	GND	COM1	5
43	RI1	COM1	9	44	DTR1	COM1	4
45	CTS1	COM1	8	46	TXD1	COM1	3
47	RTS1	COM1	7	48	RXD1	COM1	2
49	DSR1	COM1	6	50	DCD1	COM1	1

NOTES:

***** J4 pin 13 connects to printer port D-type connector pins 18 to 25 inclusive.

** Pins 35 - 38 carry RS485 signals when COM2 operates as an RS-485 port. See Table E6 for details.

TABLE E7 - J4 I/O CONNECTOR PIN ASSIGNMENTS

The connection of PS/2 keyboard and mouse connectors often cause confusion. They are 6-pin mini-DIN connectors with the same pin assignments. For reference, Figure E1 shows the pin positions, as viewed looking into the female connector.

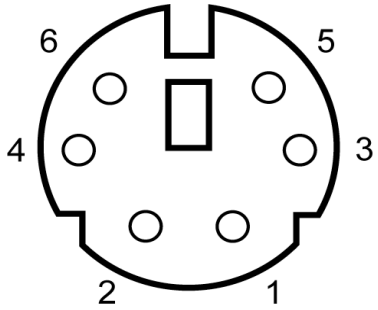


FIGURE E1 - PS/2 KEYBOARD AND MOUSE PIN ASSIGNMENTS

E.5 COM3, COM4 SERIAL PORT CONNECTOR J5

Connector J5 is a 14-way pin header adjacent to J4. It carries the COM3 and COM4 serial port signals. The signals are arranged so that a ribbon cable from J5 can easily crimp onto a 9-pin IDC D-type connector for COM3.

Pin 1 of the J5 connector can be identified by looking at the J5 silk-screen box that surrounds the J5 connector on the TP600. A “1” and “2” are located close to the pin 1 end of J5 and a “13” is placed close to the pin 14 end. All odd numbered pins are in one row and all even numbered pins are in the other row.

J5 PIN	SIGNAL	D-TYPE PIN	J5 PIN	SIGNAL	D-TYPE PIN
1	N/C	-	2	N/C	-
3	GND	5	4	RI3	9
5	DTR3	4	6	CTS3	8
7	TXD3	3	8	RTS3	7
9	RXD3	2	10	DSR3	6
11	DCD3	1	12	VCC (+5V)	-
13	/TXD4	-	14	/RXD4	

TABLE E8 - J5 COM3, COM4 CONNECTOR PIN ASSIGNMENTS

E.6 AUDIO, A/D CONVERTOR AND VGA CONNECTOR

Connector J6 is a 16-pin right angle pin header. It carries the audio or analog to digital converter signals and the signals for a VGA CRT display. Pin assignments for this connector are given in table E9.

Note that either the audio signals or the A/D converter signals are brought to the connector. Thus some pins are given one function in the columns marked "(AUDIO)" and other functions in the columns marked "(A/D)". Appendix B describes how the options are selected.

The VGA CRT display signals are usually connected to a 15-pin high density D-type connector. Pin assignments for this connector are also given in the table.

PIN	SIGNAL (AUDIO)	SIGNAL (A/D)	VGA PIN	PIN	SIGNAL (AUDIO)	SIGNAL (A/D)	VGA PIN
1	MIC IN	VREF	-	2	LINE_IN_R	ADC0	-
3	ADCGND	ADCGND	-	4	LINE_IN_L	ADC1	-
5	ADCGND	ADCGND	-	6	LINE_OUT_R	ADC2	-
7	ADCGND	ADCGND	-	8	LINE_OUT_L	ADC3	-
9	N/C		-	10	RED	RED	1
11	GREEN	GREEN	2	12	BLUE	BLUE	3
13	AGND	AGND	6, 7, 8	14	HSYNC	HSYNC	13
15	VSYNC	VSYNC	14	16	GND	GND	5, 10

TABLE E9 - J6 VGA AND A/D CONNECTOR PIN ASSIGNMENTS

E.7 DISPLAY CONNECTOR J8

This is a 40-pin DIL header on 0.05-inch pitch, providing signals to LCD panels. Table E10 gives its pin assignments.

The LCD panel signal names and may vary from panel to panel, however the signal descriptions should remain virtually the same. See section 3.10.2 for an explanation of the display signals. Note that the TP600 and TP500 have 8 data bits for each of the three colours, as compared to 6 with the TP400B. The two LSBs on the TP400B were connected to GND.

Use Table E10 and Table 7 to help you create an interface cable to connect between the TP600 and your flat panel.

DSP Design can supply a range of cable assemblies and interface boards to suit a variety of LCDs. See Appendix F for details of these interface boards.

PIN	SIGNAL	PIN	SIGNAL
1	ENABKL	2	ENAVDD
3	GND	4	SHFCLK
5	GND	6	HSYNC
7	GND	8	VSYNC
9	R0	10	R1
11	R2	12	R3
13	GND	14	R4
15	R5	16	R6
17	GND	18	R7
19	G0	20	G1
21	GND	22	G2
23	G3	24	G4
25	VCC3V (3.3V)	26	G5
27	G6	28	G7
29	VCC3V (3.3V)	30	B0
31	B1	32	B2
33	VCC (5V)	34	B3
35	B4	36	B5
37	VCC (5V)	38	B6
39	B7	40	ENAB

TABLE E10 - DISPLAY CONNECTOR J8

E.8 TEST CONNECTOR J7

Connector J7 is an 14-way SIL header. It carries JTAG and LPC bus signals. It is intended for DSP Design engineering use only.

PIN	SIGNAL
1	PCIRST#
2	SERIRQ
3	LPCAD3
4	LPCAD2
5	LPCAD1
6	LPCAD0
7	LPCFRAME#
8	VCC
9	LPCCLK
10	GND
11	JTAGTCK
12	JTAGTDO
13	JTAGTDI
14	JTAGTMS

TABLE E11 - TEST CONNECTOR J7

E.9 USB CONNECTOR J9

Connector J9 is an 8-way SIL header. It carries the USB signals to a remote PCB, the TP300USB, which carries the USB connectors. The connector is from the Hirose DF13 family.

PIN	SIGNAL
1	Port 1 Data -
2	Port 1 Data +
3	Port 1 VCC
4	Port 1 GND
5	Port 2 VCC
6	Port 2 GND
7	Port 2 Data -
8	Port 2 Data +

TABLE E12 - USB CONNECTOR J9

E.10 IDE CONNECTOR J100

This connector is for 2.5-inch IDE disk drives, which use 2mm pitch connectors. These disk drives are powered through the ribbon cable, on pins 41-44. Larger IDE drives (3.5-inch disk drives and 5.25-inch CD-ROMs) use 0.1-inch pitch connectors, but pins 1-40 are the same.

PIN	SIGNAL	PIN	SIGNAL
1	/IDE_RST	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N/C
21	DREQ	22	GND
23	/IOW	24	GND
25	/IOR	26	GND
27	IORDY	28	GND
29	/DACK	30	GND
31	IRQ14	32	N/C
33	A1	34	/PDIAG or CBLID
35	A0	36	A2
37	/CS0	38	/CS1
39	N/C (/DASP)	40	GND
41	VCC (+5V)	42	VCC (+5V)
43	GND	44	VCC (+5V)

NOTES:

Pin 34 is /PDIAG or CBLID. See Appendix B for more information.

TABLE E13 - J100 IDE CONNECTOR PIN ASSIGNMENTS

E.11 POWER SUPPLY AND FAN CONNECTORS J101 & J102

Power may be brought to the TP600 through connector J101. It is useful in stand-alone applications. Power may be sent to an optional fan through connector J102. The power supply and fan connectors are AMP HE14 connectors. The mating types are available from AMP distributors. In the UK these can be obtained by RS, whose product codes are: 532-333 (3way), 532-349 (4way) and 532-456 (crimp pins).

Pin 1 of the J101 and J102 connectors can be identified by text reading "1" on the silk screen near pins 1 of the connectors.

PIN	SIGNAL
1	VCC (+5V)
2	VCC (+5V)
3	GND
4	GND

TABLE E14 - J101 POWER SUPPLY CONNECTOR PIN ASSIGNMENTS

PIN	SIGNAL
1	GND
2	VCC (+5V)
3	GND

TABLE E15 - J102 POWER SUPPLY CONNECTOR PIN ASSIGNMENTS

E.12 FLOPPY CONNECTOR J103

The floppy disk drive can be connected through a 26-way flat flexible cable, through connector J103. Pin 26 of the J103 connector can be identified by a small "26" on the top of the plastic moulding of the connector.

PIN	SIGNAL	PIN	SIGNAL
1	VCC (+5V)	2	/INDEX
3	VCC (+5V)	4	/DS0
5	VCC (+5V)	6	/DSKCHG
7	N/C	8	N/C
9	N/C	10	/M0
11	N/C	12	/DIRC
13	N/C	14	/STEP
15	GND	16	/WD
17	GND	18	/WE
19	GND	20	/TK00
21	GND	22	/WPT
23	GND	24	/RDATA
25	GND	26	/HS

TABLE E16 - J103 FLOPPY CONNECTOR PIN ASSIGNMENTS

E.13 ETHERNET CONNECTOR

Connector J106 is an 8-way SIL header. It carries the Ethernet controller signals to a remote PCB, the TP400ET, which carries the Ethernet isolation transformer and RJ45 connector. The connector is from the Hirose DF13 family.

J106 PIN	SIGNAL
1	RxD+
2	RxD-
3	VCC (+5V or 3.3V – see LK202 description)
4	GND
5	/LINKLED
6	/LANLED
7	TxD-
8	TxD+

TABLE E17 - J106 ETHERNET CONNECTOR PIN ASSIGNMENTS

APPENDIX F - LCD SUPPORT

This appendix describes some options for connecting LCDs to the TP600.

F.1 INTRODUCTION

The TP600 supports TFT panels of 640 x 480, 800 x 600 and 1024 x 768 pixel resolution. A range of TFT panels from different manufacturers have been successfully tested with the TP600 under ROM-DOS and Windows XP Professional.

Table F1 shows some of the LCDs tested by DSP Design and the interface boards and cable assemblies required.

Part number	Interface type	Resolution	Interfaced via
NEC NL6448BC26-01	18-bit digital	640 x 480	TFTIF31 + TFTIF-CAB7
Kyocera TCG075VG2AC-G00 (TFTIFKYV75-KIT from DSP Design)	18-bit digital	640 x 480	TFTIFKYV + TFTIF-CAB7 (part of TFTIFKYV75-KIT)
Sharp LQ121S1DG31	18-bit digital	800 x 600	TFTIF41 + TFTIF-CAB7
LG Philips LM151X05	18-bit digital	1024 x 768	TFTIF41 + TFTIF-CAB7

TABLE F1 - INTERFACING TYPICAL DISPLAYS

At present there are three interface boards which can be used with the TP600. The TFTIF31, TFTIF41 and TFTIFKYV boards interface to LCDs with conventional parallel interfaces (6 bits of red, green and blue, plus timing signals).

Note that the TP600 display controller signals are 3.3V voltage levels. Some 5V displays may not work reliably with 3.3V signals. In this event, pull-up resistors (to 5V) on some timing or sync signals may be useful, although users must make their own decisions about this.

The TFTIF31 and TFTIF41 boards are likely to support a number of other displays from other manufacturers, as the 31-way and 41-way connectors on the Sharp display are used by a number of other manufacturers. Different displays may have different pin assignments, however, and users must carefully check the pin assignments on their displays to see that they match the pin assignments on one of the TFTIF boards.

The TFTIF31 and TFTIF41 boards have a solder link area to allow the selection of the correct power supply voltage for the LCD (either +5V or +3.3V). The TFTIF31 and TFTIF41 boards contain power transistors that can switch off the power to the LCD when instructed to do so by the graphics controller logic. This allows the display to be powered down, if required, when the TP600 is in standby or suspend modes.

The TFTIF31 and TFTIF41 boards also feature a connector with the TP600 backlight enable signal (ENABKL) on it. This signal can be sent to the backlight inverter, and used to power off the backlight when instructed to do so by the graphics controller logic.

The TFTIF31 and TFTIF41 include solder links that can invert the image left to right, and top to bottom. These links used together can be used to tip the picture upside down, which can be useful to improve the viewing angle on the displays. Note that this is a feature of some Sharp and Kyocera displays; other LCDs use the same pins for other functions, and so users should check the pin assignments of their LCDs carefully.

F.2 POWERING LCDS

LCDs will require two power sources – a relatively high power source (typically +5V or +12V) for the backlight inverter) and a lower power source for the LCD electronics (usually +3.3V, but sometimes +5V). For convenience, the TP600 and TFTIFxx boards allow the 5V and 3.3V power supplies from the TP600 to be routed through to the LCD electronics.

Note that the TP600 may not be able to supply all of the current required for the LCD's electronics, and you might need to arrange for a separate power supply for the display.

F.3 INSTALLATION

(This section does not apply to the TFTIFKYV board. The TFTIFKYV has its own Technical Reference Manual which provides more information.)

Ensure that the TP600 BIOS is configured in the BIOS Setup program to support an LCD of the desired resolution.

Check the solder links on the TFTIFxx board against the instructions in section F.5 or section F.6.

Plug the 40-way ribbon cable assembly onto the TFTIFxx and to connector J8 on the TP600, ensuring that the cable is correctly aligned with pin 1 at both ends. Note that it may be necessary to orient the cable so that the red wire connects to pin 40, rather than pin 1.

Plug the TFTIFxx board onto the LCD.

Connect a backlight inverter to the TFT LCD and add appropriate wiring to the inverter. **Take care with the backlight inverter as it produces a very high voltage (several hundred volts).**

You may wish to control the backlight inverter's enable and brightness pins with signals from the TFTIFxx boards. See later sections for instructions on this.

Switch on the TP600. You should see clear, crisp graphics on the LCD panel.

F.4 CABLE LENGTHS

The TFTIFxx boards are supplied without the 40-way ribbon cable. This must be ordered separately.

For parallel interfaces cable length is a compromise between reducing electrical noise and increasing convenience. DSP Design has tested the TP600 using the cables listed in Table F1 only and therefore strongly recommends that parallel interface cables be no longer than 7 inches. DSP Design can supply the TFTIF-CAB7 for this purpose.

F.5 TFTIF31

The TFTIF31 is designed to interface with a number of LCDs, from Sharp and other manufacturers, that use a 31-way Hirose DF9 connector. This section describes the TFTIF31, listing the display pin assignments and the solder link settings.

F.5.1 31-Pin Connector Pin Assignments

Table F2 gives the pin assignments of the TFTIF31 display connector. Note that this connector supports 18-bit LCDs (displays with six bits each of red, green and blue data). The TP600 can support 24-bit displays displays with eight bits each of red, green and blue data). The signal names in Table F2 have been adjusted to reflect the fact that the TP600 and TFTIF31 route the six most significant bits of each colour to the LCD. If you look at the data sheet for an LCD you will see the colour data bits described as R0-5 and so on, rather than R2-7, as shown here.

PIN	LCD SIGNAL	PIN	LCD SIGNAL
1	GND	2	SHFCLK
3	HSYNC	4	VSYNC
5	GND	6	R2
7	R3	8	R4
9	R5	10	R6
11	R7	12	GND
13	G2	14	G3
15	G4	16	G5
17	G6	18	G7
19	GND	20	B2
21	B3	22	B4
23	B5	24	B6
25	B7	26	GND
27	ENABLE	28	LCD VCC
29	LCD VCC	30	RIGHT/LEFT
31	UP/DOWN	-	-

TABLE F2 - TFTIF31 DISPLAY PIN ASSIGNMENTS

F.5.2 Power Supply Selection: LK1

The TFTIF31 accepts +3.3V and +5V from the TP600 and passes it on to the LCD, to power its electronics (though not the backlight inverter). The power supply voltage is selected by solder link LK1. The selected voltage is then routed to a transistor switch, which turns on the power to the LCD under control of the TP600 ENAVDD signal.

LK1 can be set to one of two positions. The position marked "5" is for 5V LCD displays. The position marked "3.3" is for 3.3V panels. You may need to change the solder link to match your display.

F.5.3 Pin 30 and 31 Configuration: LK2 and LK3

LK2 and LK3 are connected to the 31-way connector pins 30 and 31 respectively. The links can be used to change the display orientation, at least on some Sharp displays. For a normal image both should be left open, or linked in the 2-3 position. For an upside-down image both should be linked in the 1-2 position.

Some other LCDs use pins 30 and 31 for other purposes, such as additional power supply pins. LK2 and LK3 should therefore be linked to match the requirement of each display. Table F3 lists the connections of the LK2 and LK3 pins, thus allowing suitable connections to be made.

LK2 PIN	LK2 CONNECTION	LK3 PIN	LK3 CONNECTION
1	GND	1	GND
2	PIN 30	2	PIN 31
3	LCDVCC	3	LCDVCC

TABLE F3 - TFTIF31 PIN 30 AND PIN 31 CONNECTIONS

F.5.4 Backlight Enable Signal

The TP600 generates a logic-level signal intended to turn on and off the backlight inverter. This signal is called ENABKL, and is 0V for “off” and +3.3V for “on”. The ENABKL signal can be taken to a backlight inverter from the TFTIF31 connector J3. J3 is a Molex 53261-0390 connector. Pin assignments are given in Table F4. Note that some backlight inverters specify a 5V signal to turn on the backlight, so ENABKL may not work with all inverters.

ENABKL is also available on connector J17 on the TP600.

J3 PIN	SIGNAL
1	VCC (+5V)
2	ENABKL
3	GND

TABLE F4 - TFTIF31 AND TFTIF41 J3 PIN ASSIGNMENTS

F.6 TFTIF41

The TFTIF41 is designed to interface with a small number of LCDs, principally from Sharp, that use a 41-way Hirose DF9 connector. This section describes the TFTIF41, listing the display pin assignments and the solder link settings.

F.6.1 41-Pin Connector Pin Assignments

Table F5 gives the pin assignments of the TFTIF41 display connector. Note that this connector supports 18-bit LCDs (displays with six bits each of red, green and blue data). The TP600 can support 24-bit displays displays with eight bits each of red, green and blue data). The signal names in Table F5 have been adjusted to reflect the fact that the TP600 and TFTIF41 route the six most significant bits of each colour to the LCD. If you look at the data sheet for an LCD you will see the colour data bits described as R0-5 and so on, rather than R2-7, as shown here.

PIN	LCD SIGNAL	PIN	LCD SIGNAL
1	GND	2	SHFCLK
3	GND	4	HSYNC
5	VSYNC	6	GND
7	GND	8	GND
9	R2	10	R3
11	R4	12	GND
13	R5	14	R6
15	R7	16	GND
17	GND	18	GND
19	G2	20	G3
21	G4	22	GND
23	G5	24	G6
25	G7	26	GND
27	GND	28	GND
29	B2	30	B3
31	B4	32	GND
33	B5	34	B6
35	B7	36	GND
37	ENABLE	38	RIGHT/LEFT
39	LCDVCC	40	LCDVCC
41	UP/DOWN	-	-

TABLE F5 - TFTIF41 DISPLAY PIN ASSIGNMENTS

F.6.2 Power Supply Selection: LK1

The TFTIF41 accepts +3.3V and +5V from the TP600 and passes it on to the LCD, to power its electronics (though not the backlight inverter). The power supply voltage is selected by solder link LK1. The selected voltage is then routed to a transistor switch, which turns on the power to the LCD under control of the TP600 ENAVDD signal.

LK1 can be set to one of two positions. The position marked "5" is for 5V LCD displays. The position marked "3.3" is for 3.3V panels. You may need to change the solder link to match your display.

F.6.3 Pin 41 and 38 Configuration: LK2 and LK3

LK2 and LK3 are connected to the 41-way connector pins 41 and 38 respectively. The links can be used to change the display orientation, at least on some Sharp displays. For a normal image both should be left open, or linked in the 2-3 position. For an upside-down image both should be linked in the 1-2 position.

Some other LCDs may use pins 41 and 38 for other purposes, such as additional power supply pins. LK2 and LK3 should therefore be linked to match the requirement of each display. Table F6 lists the connections of the LK2 and LK3 pins, thus allowing suitable connections to be made.

LK2 PIN	LK2 CONNECTION	LK3 PIN	LK3 CONNECTION
1	GND	1	GND
2	PIN 41	2	PIN 38
3	LCDVCC	3	LCDVCC

TABLE F6 - TFTIF41 PIN 41 AND PIN 38 CONNECTIONS

F.6.4 Backlight Enable Signal

The TP600 generates a logic-level signal intended to turn on and off the backlight inverter. This signal is called ENABKL, and is 0V for “off” and +3.3V for “on”. The ENABKL signal can be taken to a backlight inverter from the TFTIF41 connector J3. J3 is a Molex 53261-0390 connector. Pin assignments are given in Table F4. Note that some backlight inverters specify a 5V signal to turn on the backlight, so ENABKL may not work with all inverters.

ENABKL is also available on connector J17.

(This page is intentionally blank)

APPENDIX G - TP400ET ETHERNET ADAPTER BOARD

The TP600's Ethernet chip is connected to the network's twisted pair cable through a small printed circuit board called the TP400ET. This is joined to the TP600 with a short length of CAT5 unshielded twisted pair cable. The TP400ET contains the Ethernet isolation transformer, EMC filters and an RJ45 connector with status LEDs. The TP400ET is designed to be mounted on the enclosure; this location allows EMC filtering to be optimised.

A cable assembly, the TB486ET-CAB, joins the TP600 to the TP400ET.

The TP400ET has two status LEDs. The green LED connects to the LED10 and LED100 pins of the DP83816 and glows whenever the DP83816 receives valid 10Base-T or 100Base-T link pulses. The yellow LED connects to the LEDACT pin of the DP83816 and glows when the DP83816 transmits or receives a frame.

This Appendix contains the mechanical drawing of the TP400ET, allowing users to build their enclosure to accommodate the TP400ET. It also includes the circuit of the TP400ET, for users who would prefer to design the TP400ET circuitry into their own PCBs.

This circuit remains the copyright of DSP Design Limited, but DSP Design grants permission for any or all of the circuit to be used by DSP Design customers who are using the circuit together with DSP Design's processor boards. The circuit is offered on an unsupported basis, and no warranty is given as to the accuracy of the design.

Note that the TP600 can supply either 3.3V or 5V on pin 3 of the 8-way cable, depending on the LK202 link setting. When using the TP600 with the TP400ET, 5V should be supplied.

Care should be taken when tracking the TP400ET circuitry. National Semiconductor do not seem to publish guidelines on PCB tracking, but the Users' manual for the CS8900, which DSP Design use on other processors, gives useful guidance. This is available on the Cirrus logic web site, at www.cirrus.com.

Data on the DP83816 is on the National Web site at www.national.com.

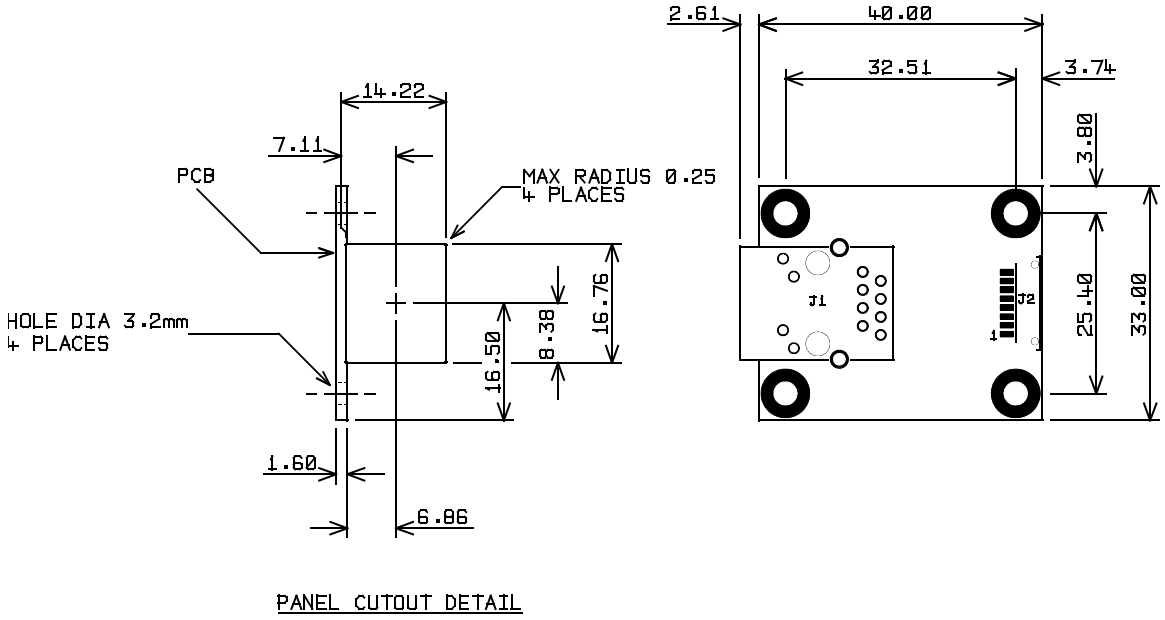


FIGURE G1 - TP400ET MECHANICAL DRAWINGS

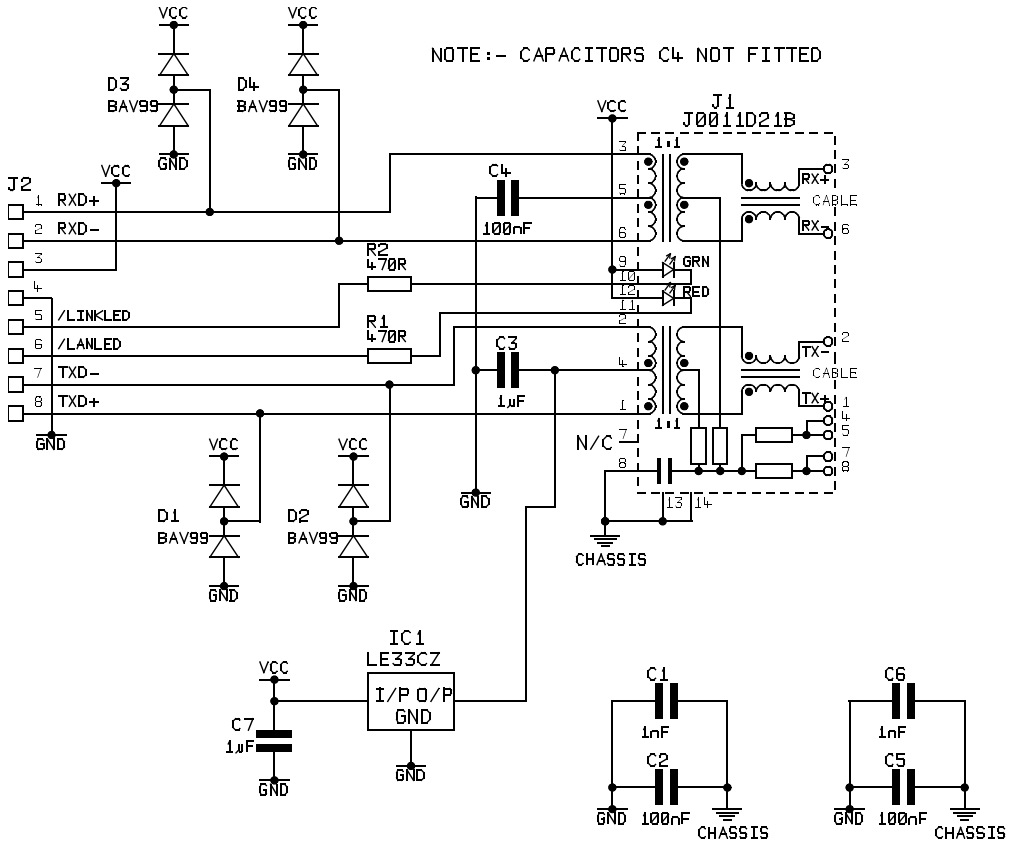


FIGURE G2 - TP400ET CIRCUIT DIAGRAM

APPENDIX H - TP300USB ADAPTER BOARD

The TP600's USB ports are accessed through a small printed circuit board called the TP300USB. This is joined to the TP600 with a short length of CAT5 unshielded twisted pair cable, implemented as a cable assembly called the TB486ET-CAB. The TP300USB contains EMC filters and a dual USB connector with status LEDs. The TP300USB is designed to be mounted on the enclosure; this location allows EMC filtering to be optimised.

This Appendix contains the mechanical drawing of the TP300USB, allowing users to build their enclosure to accommodate the TP300USB. It also includes the circuit of the TP300USB, for users who would prefer to design the TP300USB circuitry into their own PCBs.

This circuit remains the copyright of DSP Design Limited, but DSP Design grants permission for any or all of the circuit to be used by DSP Design customers who are using the circuit together with DSP Design's processor boards. The circuit is offered on an unsupported basis, and no warranty is given as to the accuracy of the design.

Care should be taken when tracking the TP300USB circuitry. Power tracks should be kept thick. The signals tracks should also be wide, and should run as pairs in parallel, avoiding vias and other tracks as far as possible.

The TP300USB is designed for USB v1.1 peripherals (or USB v2.0 peripherals operating at USB v1.1 speeds). It will not work with USB v2.0 peripherals operating at the high USB v2.0 speeds.

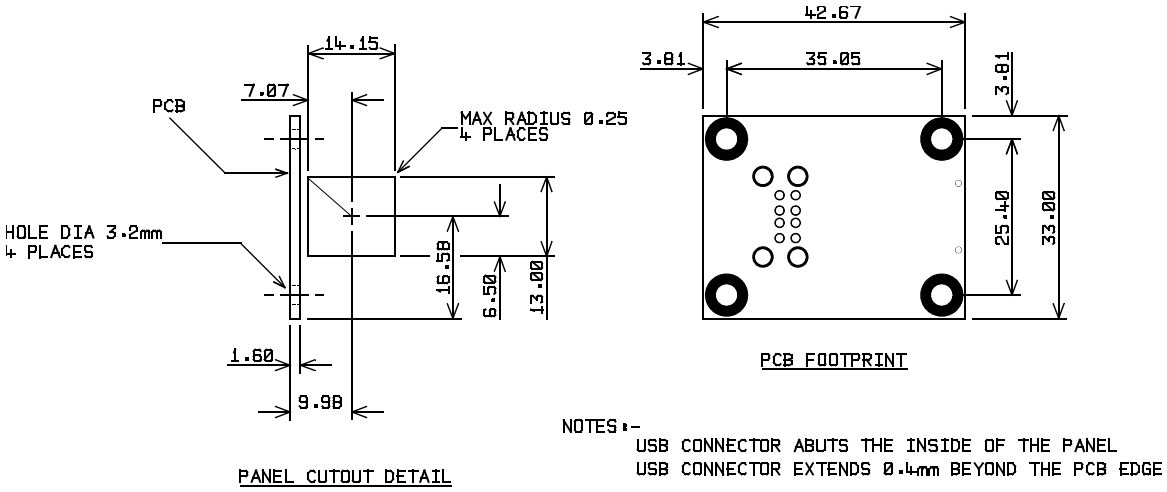
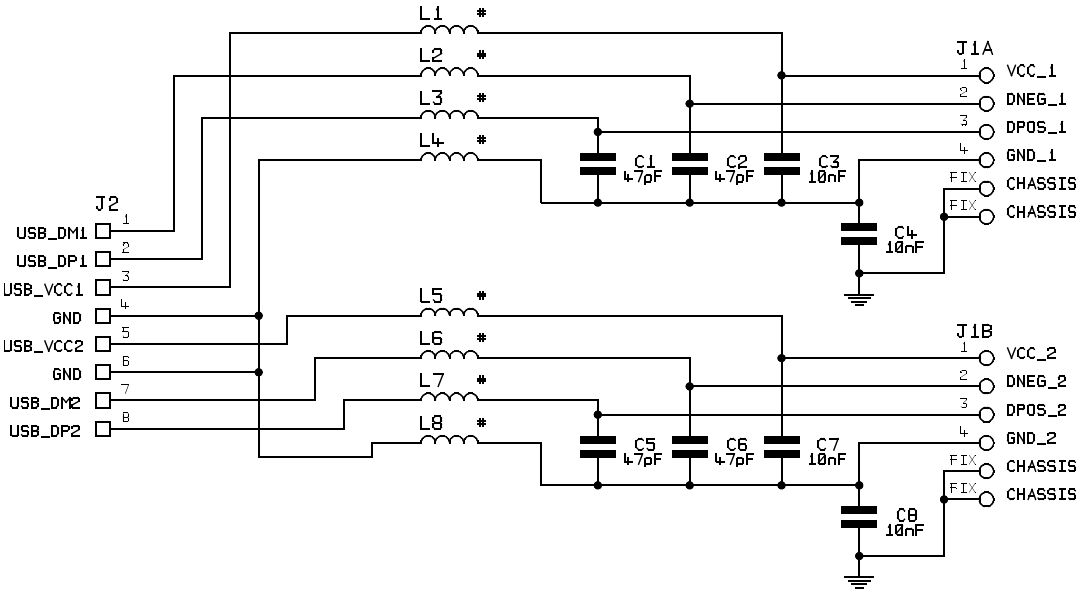


FIGURE H1 - TP300USB MECHANICAL DRAWINGS



REF	MANUFACTURER	PART No.
L2.3.6.7		0805 FERRITE BEAD
L1.4.5.8	PANASONIC	EXCCL3216U (2 AMP RATING)
	RS PART No.	233-5061
J1	AMP	787617-1
J2	HIROSE	DF13-8P-1.25V

FIGURE H2 - TP300USB CIRCUIT DIAGRAM

APPENDIX I - MIGRATING TO THE TP600

I.1 INTRODUCTION

This section is intended to aid customers with existing TP400B or TP500 based products to migrate their designs to use TP600. These three boards are based on different Geode chipsets:

- TP400B is based on a Geode GX1 / CS5530A chip set.
- TP500 is based on a Geode GX2 / CS5535 chip set.
- TP600 is based on a Geode LX800 / CS5536 chip set.

TP600 has very similar functionality to TP500. Aside from the change in chipset, the other major onboard devices such as the Super I/O, PCI to ISA bridge, Ethernet Controller, Audio Codec and Flash are common to both boards. TP600 uses a different BIOS to TP500, and some minor differences in BIOS operation do exist.

The difference between TP600 / TP500 and TP400B is more significant. These boards differ in the following two significant ways:

- Super I/O chip. TP400B uses a PC97317 ISA SIO, TP500 uses a W83627 LPC SIO.
- Utility Register: This is implemented in the Super I/O chip and is therefore different.

This section highlights hardware and BIOS differences between the TP600 and its two predecessors that may have an impact on customer systems.

I.2 REFERENCES

The following documents are available from the DSP Design website at http://www.dspdesign.com.

158004 TP400B Technical Reference Manual

158804 TP500 Technical Reference Manual

158904 TP600 Technical Reference Manual (this manual)

I.3 DIFFERENCES

Table I.1 highlights all differences between TP400B, TP500 and TP600 that may have an impact on customer systems. Please refer to the relevant sections in the Technical Reference Manuals listed in Section I.2 for detailed technical information about specific features that differ.

FEATURE	TP400B	TP500	TP600
CPU	Geode GX1	Geode GX2	Geode LX
CPU Speed Configuration	300MHz	400MHz	400MHz
Companion Chip	CS5530	CS5535	CS5536
Super I/O	NS PC97317	Winbond W83627	Winbond W83627
PC/104 Bus	Yes	Yes	Yes
PC/104-Plus Bus	Yes	Yes	Yes
PC/104-Plus Interrupts	INTA# to INTD#	INTA# to INTD#	INTC# not supported
Memory Map		Differs to TP400B (BIOS & FFS extension addresses)	As for TP500 but no FFS extension.
I/O Map		Differs to TP400B (utility register, sound card & ISA)	Same as TP500
Floppy Controller	Yes	Yes	Yes
IDE Controller	Yes	Yes	Yes
Serial Ports	4	4	4
Serial Port Caps	3 x RS232 + 1 x TTL	3 x RS232 + 1 x TTL	3 x RS232 + 1 x TTL
COM1 Capabilities	RS232	RS232	RS232
COM 1 Resources	IO:3F8h, IRQ:4	IO:3F8h, IRQ:4	IO:3F8h, IRQ:4
COM1 Options	Enable/Disable	Enable/Disable	Enable/Disable
COM2 Capabilities	RS232 / RS485 / (IrDA)	RS232 / RS485 / (IrDA)	RS232 / RS485 / (IrDA)
COM2 Resources	IO:2F8h, IRQ:3	IO:2F8h, IRQ:3	IO:2F8h, IRQ:3
COM2 Options	Enable/Disable	Enable/Disable	Enable/Disable
COM3 Capabilities	RS232	RS232	RS232
COM3 Resources	IO:3E8h, IRQ:5	IO:3E8h, IRQ:5	IO:3E8h, IRQ:5
COM3 Options	Enable/Disable	Always enabled	Aways enabled
COM4 Capabilities	TTL	TTL	TTL
COM4 Resources	IO:2E8h, IRQ:9	IO:2E8h, IRQ:9	IO:2E8h, IRQ:9
COM4 Options	Enable/Disable	Always enabled	Aways enabled
Parallel Port	Bi-Directional /EPP/ECP	Bi-Directional /EPP/ECP	Bi-Directional /EPP/ECP
Memory (SDRAM)	144-Pin SODIMM	200-Pin DDR SODIMM	200-Pin DDR SODIMM
Memory Size Capacities	32-512MB	128-512MB	128-1024MB
BIOS Memory	256K of 2MB Flash	512K	1MB
Flash Memory	2MB	2MB	2MB
Flash File System	Yes (ROM-DOS)	Yes (ROM-DOS)	Yes (ROM-DOS)
Keyboard / Mouse	PS/2 and USB	PS/2and USB	PS/2and USB

FEATURE	TP400B	TP500	TP600
On-board Speaker	Yes	Yes	Yes
USB	2 x v1.0 ports	2 x v1.1 ports	2 x v1.1 ports
Graphics	VGA	VGA	VGA
Graphics CRT Max. Resolution	1280x1024 (SXGA)	1280x1024 (SXGA)	1280x1024 (SXGA)
Graphics TFT Max. Resolution	1024x768 (XGA)	1024x768 (XGA)	1024x768 (XGA)
Graphics Memory Architecture	UMA	UMA	UMA
Graphics Memory Max. Allocation	4.5MB	16MB	60MB
Ethernet	National Semiconductor DP83815	National Semiconductor DP83815	National Semiconductor DP83815
Ethernet Capabilities	10/100Base-T/X	10/100Base-T/X	10/100Base-T/X
Analogue to Digital Converter (ADC)	MAX1247	MAX1247	MAX1247
ADC Capabilities	4 Channel	4 Channel	4 Channel
Temp. Sensor	LM60C on ADC3	LM60C on ADC3	LM60C on ADC3
Audio Compatability	Soundblaster	AC97	AC97
Power supply	5V	5V	5V
PSU	Switched 2.0 / 3.3V	Switched 1.5 / 2.5 / 3.3V	Switched 1.25 / 2.6 / 3.3V
Calendar/Clock	Yes with External Battery	Yes with External Battery	Yes with External Battery
Watchdog Circuit	Yes	Yes	Yes
Power Supply Monitoring Circuit	Yes	Yes	Yes
EEPROM Memory	512Bytes	512Bytes	512Bytes
EEPROM CMOS Backup	Yes	Yes	Yes
Super I/O Utility Register Address	E0-E7	via SIO configuration register	via SIO configuration register
IRQ Default Allocation	PCI & PC/104 interrupt allocation differ.	PCI & PC/104 interrupt allocation differ.	PCI & PC/104 interrupt allocation differ.
DMA	7 Channels	7 Channels	7 Channels
DMA on ISA Bus	Yes	Not implemented	Not Implemented
BIOS Setup Entry Key	F2	F1	DEL
BIOS Setup		No COM3,4	No COM3,4 No ISA IO address, no IRQ routing.
BIOS Extensions	VGA, FFS	VGA, FFS	VGA (No FFS)
BIOS Update Utility	TP3F016	FLASHROM	REFLASH
Flash File System (FFS)	ROM-DOS Loadable Driver + BIOS Extension	ROM-DOS Loadable Driver + BIOS Extension	ROM-DOS Loadable Driver
Flash Utility	TP3F016	TP3F016	TP3F016
Watchdog Utility	TP3WDOG -T TP400B	TP3WDOG -T TP500	TP3WDOG -T TP500

FEATURE	TP400B	TP500	TP600
Dimensions: PCB	90 x 96mm	90 x 96mm	90 x 96mm
Dimensions: (inc. Connectors)	108 x 96 x 26mm	108 x 96 x 26mm	108 x 96 x 26mm
Heatsink Mounting Holes		4 holes, same size and position as for TP400B	4 holes, different size and position to TP400B / TP500.
Weight	180g	144g	128g
Link Settings	Differ	Differ	Differ
Connector Pinout		J1, J3, J6, J8, J100 differ to TP400B	Same as TP500.
LCD Support		Differs from TP400B	As for TP500

TABLE I1 - DIFFERENCES BETWEEN TP600, TP500 AND TP400B

APPENDIX J - TPPCIC ADAPTER BOARD

The TPPCIC is an adapter board that allows a PC/104-Plus processor board to connect to conventional PCI bus boards. The PC/104-Plus processor board plugs into the TPPCIC through the 120-way PC/104-Plus connector, and the PCI board plugs into the TPPCIC through an edge connector.

This edge connector is oriented so that the PCI board, the TPPCIC and the PC/104-Plus processor board all in the same orientation (in contrast with PCI motherboards where the PCI board is at right angles to the motherboard).

The TPPCIC contains solder links that allow the PCI boards to be configured as any of the PCI slots. By default the solder links are configured so that the PCI board is in slot 2.

The solder links allow individual selection of the slot number (with the IDSEL links), the interrupt (with the INT links), the PCI clock (with the CLK links) and the bus master arbitration pins (with the REQ and GNT links). The solder links are on the rear of the PCB, and link positions are identified by text on the PCB.

Users should read section 4.3 and 4.5.2 of this manual to determine appropriate settings for their PCI board.

When plugging in the PCI board, note that it must be inserted the right way round – that is, with the components on the PCI board facing down. Some PCI boards will be able to plug in the other way around as well, and this may damage them, or the TPPCIC, or the PC/104-Plus processor board.

Note that there is an error on the silk-screen of the TPPCIC. The PCI connector pin labelled B2 is in fact pin A61, and the pin labelled B62 is in fact A1. This error has been corrected on some TPPCIC boards by adding paper labels over the incorrect text.

The TPPCIC includes a 6-way power supply connector, J3. This is designed to mate with the TCPSU or TPPSU power supply from DSP Design, which can supply +5V, +12V and –12V to both the PCI board and the PC/104-Plus processor. Note that the TCPSU and TPPSU power connectors are polarized. Ensure that the locking tab on the power supply cable mates with the locking tab on the TPPCIC connector. **Failure to connect the power supply cable assembly correctly may damage the equipment.**

Note that on the TPPSU the mains earth is connected to 0V. This is done in the 6-way connector, with the braid (earth) connecting to one of the 0V wires. Users who are using the TCPSU power supply must explicitly connect the mains earth to their TPPCIC, by plugging the green and yellow earth lead onto the spade terminal soldered to the printer connector.

The TPPCIC includes buffers which allow 5V PCI boards to be connected to the TP600 (the PCI bus on the Geode processor used on the TP600 is not 5V tolerant).

Users should note that the VI/O power supply pins from the PC/104-Plus processor card are routed to the VI/O pins of the PCI socket. In the case of the TP600 VI/O is set to 3.3V. We have encountered a PCI board, which hard wired its VI/O pins to 5V. When this card was inserted into the TPPCIC with a TP600 the 5V and 3.3V rails were thus shorted together. **It is therefore important to check for this situation before plugging a new PCI board into the TPPCIC. If necessary the solder link at LK18 can be changed, or removed entirely.**

A number of test points are provided which allows some of the PCI bus signals to be monitored with an oscilloscope during engineering work.

APPENDIX K - FAULT REPORTING

DSP Design makes every effort to ship products and documentation that are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a “Product Fault Report” form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to DSP Design with the faulty product.

Prior to returning a faulty product, please check the following:

1) The board has been correctly configured for the intended application (see earlier appendix for board installation details).
2) The power supplies are providing correct voltage levels.
3) Cabling to the board is sound and connected correctly.
4) Other cards in the system are known to be correctly configured and functioning.
5) PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT			
CUSTOMER INFORMATION:		**PRODUCT INFORMATION:**	
Company Name:		Product Name:	
Contact Name:		Serial No.:	
Phone No:		Date of return:	
SYMPTOMS OBSERVED:			
SYSTEM CONFIGURATION (e.g. other boards present, operating system and software):			
For DSP Design Use:			
Product Test Report:			
Date of Receipt:		Repaired by:	
Charges to be invoiced:			
Date of Return:		Returned by:	

TABLE K1 - PRODUCT FAULT REPORT FORM

(This page is the inside of the back cover, and is intentionally blank)

DSP Design Limited
Tapton Park Innovation Centre
Brimington Road
Chesterfield S41 0TZ
United Kingdom
Tel +44 (0) 1246 545 910
Fax +44 (0) 1246 540 576
Email info@dspdesign.com
Web www.dspdesign.com