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Aurora AA1100

Embedded PDA

Technical Reference Manual

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REVISION HISTORY

A00 This is the first release of this manual.

B00 This version includes more detail on many topics, includes information on the Rev B01 and B03 PCB versions, provides new information on new LCD interfaces, GPIO pins, expansion bus, power management, corrects some errors and typos, corrects the block diagram and modifies document style.

1 INTRODUCTION

This manual describes the B00, B01 and B03 revisions of the Aurora AA1100 embedded PDA processor board.

Note that when handling the AA1100, and when adding or removing connectors in particular, due anti-static precautions should be taken. Note also that the two SDRAM chips are chip-scale packages and are subject to damage if pressure is applied to them.

1.1 OVERVIEW

The Aurora AA1100 is a member of the Aurora family of products and has been designed using state of the art PDA technology using AMD's Au1100 high performance, low-power, high-integration systems-on-a-chip (SOC) processor designed for hand held and low power portable computing applications. This concept enables the board to run industry standard operating systems and applications, thereby reducing the development time for the user.

The Aurora AA1100 can operate as a standalone module requiring only a single 3.3V input or can interface to a number of other members of the Aurora family to provide a complete system. Alternatively, customers can interface to the Aurora AA1100 with their own hardware using either the three ribbon cable connectors or the high-density board-to-board connectors.

Great care has been taken to design a low power system with a very low suspend power consumption, making the Aurora AA1100 ideal for battery operated systems.

The Aurora AA1100 can be supplied with Windows CE or Linux and can operate with or without a user interface. It is an internet-ready appliance, which has a web browser and server built-in when using DSP Design's pre-configured Windows CE operating system. With a host of I/O functions the Aurora AA1100 can be rapidly configured to be a data entry terminal, video player, messaging system, control system or simply a monitoring unit.

1.2 AURORA AA1100 FEATURES

- AMD's Au1100 processor uses the MIPS32 instruction set, providing high performance at very low power consumption when clocked at a maximum of 400MHz. A 500MHz version is available, subject to a minimum order quantity.

- 64Mbytes of SDRAM soldered to the board. A 128M-byte version is available, subject to a minimum order quantity.

- 32M bytes of AMD MirrorBit Flash capable of containing the operating system. A 64M-byte version is available, subject to a minimum order quantity.

- Flash File System provided non-volatile read-write storage.

- An on-board Compact Flash socket allows a range of Compact Flash cards to be used for memory or peripheral expansion. A second Compact Flash socket is available on the Aurora AAMCA Expansion Board. Alternatively, a second Compact Flash socket or PCMCIA socket can be attached via the expansion bus.

- 10/100 Base-T Ethernet (magnetics and RJ45 socket are remotely mounted).

- Drives mono STN, colour STN and TFT LCDs at resolutions up to 800 x 600. Hardware rotate is available for panel sizes up to 320 x 240. A CRT can be driven with the Aurora AAVGA add-on card.

- Four-wire resistive touch screen controller.

- Keypad controller supporting up to 8 rows and 14 columns.

- Two USB 1.1 host ports (5V is required to power the USB device). One USB port can in principle operate as a USB slave, but software support for this is not available at present.

- SIR compatible IrDA Controller (transceiver remotely mounted).

- Three serial ports. COM1 and COM2 are two-wire RS232. COM3 is an eight-wire RS232 or four-wire RS485.

- Four channel 12-bit ADC with 0-3.3V input range.

- An AC97 codec provides microphone, stereo line inputs, stereo headphone outputs, and a stereo line output capable of driving speakers.

- The watchdog circuit can be used to automatically restart the module if the host application fails.

- A 512 byte serial EEPROM can be used to store setup information.

- Two counter/timers to provide Time of Year (TOY) and Real Time Clock (RTC).

- Users can interface further SRAM, Flash, Compact Flash, PCMCIA or other peripherals to the Aurora AA1100 via a 16-bit expansion bus.

- Some GPIO pins are available for user applications.

- SSI serial bus signals are available for attaching to user's peripherals.

- The Aurora AA1100 consumes very low power from a single 3.3V power supply even when operating at full speed. Power management software switches off unused circuitry for extremely low power consumption in suspend state.

- Most peripherals can be accessed through the 44-way and 50-way 2mm pitch pin headers. These signals are also available, together with the expansion bus signals, on the two high-density board-to-board connectors.

- A single board measuring only 85.4mm x 63.8mm and weighing only 25 grams.

1.3 THE AURORA FAMILY

The Aurora family consists of a number of boards designed to compliment the Aurora AA1100 processor and extend its capabilities. By utilising these Aurora boards, a complete system can be developed quickly and efficiently for many applications. Many of these boards are shown in Figure 2, and Figure 1 shows a block diagram of a system using these boards.

1.3.1 AACONN

The Aurora AACONN is a connector breakout board for the Aurora AA1100. It connects to the Aurora AA1100 using a short length of ribbon cable and provides standard PC type connectors. It has the following features:

- The same size as the Aurora AA1100, so that it can be mounted underneath the Aurora AA1100 using short pillars to obtain a self-contained module. Alternatively the AACONN can be mounted “end on” with the Aurora AA1100.
- An external 5V PSU (TCONN-PSU) supplies power through a 5.5mm input jack. The 5V supply feeds the on-board 3.3V PSU (for the Aurora AA1100), USB ports and LCD backlight inverter.
- Ethernet magnetics, filter components and RJ45 socket.
- Dual USB socket, power switch (500mA rating) and filter components.
- Eight-wire RS232 9-pin D-type socket (male).
- Mono microphone 3.5mm jack and filter components (pink socket).
- Stereo line output 3.5mm jack and filter components (green socket).
- On-board mono speaker connected across the stereo line output. Selected via link option.
- Two debounced switches connected to two Aurora AA1100 GPIO inputs.
- SIR compatible IrDA transceiver. Three power output levels selectable via link options.
- Backlight inverter power socket (5V).
- Reset switch.

1.3.2 AAMCA

The Aurora AAMCA is a daughter board which mounts onto the Aurora AA1100 via two high-density board-to-board connectors and communicates to the Aurora AA1100 via the 16-bit expansion bus. It was designed initially as a technology demonstrator, to assist with the product development, but it can also be used in production systems. It has the following features:

- A hot-swappable second Compact Flash socket configured for memory and I/O modes providing both memory and peripheral expansion. Power switching circuitry and buffers are provided to isolate the Compact Flash card under software control to reduce power consumption when not required.

- Eight memory-mapped digital inputs available on a pin header. Reading from a memory address will read the status of these inputs.

- Eight memory-mapped digital outputs available on a pin header. Writing a bit pattern to a memory address will set the associated output state.

- Eight memory-mapped edge mounted LEDs. Writing a bit pattern to a specific memory address will illuminate the associated LED. The LEDs can be disabled to save power, if required.

- A socket for a Secure Digital memory or I/O card (not fitted or currently supported in software).

1.3.3 AAVGA

The Aurora AAVGA is a small module which plugs directly into the Aurora AA1100 LCD connector or via a ribbon cable. It provides a standard 15-pin D-type connector. The AAVGA converts the LCD signals into analog RGB signals suitable for a conventional monitor. This can be very useful in development when an LCD is not available or for headless applications where occasional use is required.

1.3.4 LCD Interface Boards

Several interface boards are available that allow the Aurora AA1100 to drive a range of different LCD panels. These boards connect directly to the LCD and connect to the Aurora AA1100 LCD connector via a short ribbon cable. Details vary depending on the LCD, but each board typically provides some or all of the following features.

- Converts the Aurora AA1100 LCD signals to different connector types required by each supported LCD panel.

- Allows the Aurora AA1100 to control the LCD power sequencing.

- Allows the Aurora AA1100 to control the backlight inverter power sequencing.

- Allows the Aurora AA1100 to control the display brightness.

- Provides a touchscreen interface connector.

1.4 A TYPICAL AURORA CONFIGURATION

Figure 1 shows a typical system configuration using the three pin-header connectors on the Aurora AA1100's top surface and the two high-density connectors on the rear.

The Aurora AA1100 connects to the AACONN via a short 50-way ribbon cable assembly (AACONN-CAB). The Ethernet cable, USB mouse and USB keyboard plug into the AACONN, along with power from the TCONN-PSU. An RS232 serial port is available. Use either the on-board speaker or connect some external speakers or headphones to the stereo line output socket.

The AAVGA can be used for CRT based applications and can be either mounted directly onto the Aurora AA1100 or via a ribbon cable (TFTIFCAB7 or TFTIFCAB11). For LCD applications, connect one of the LCD interface boards to the associated LCD panel and connect to the Aurora AA1100 via a ribbon cable (TFTIFCAB7 or TFTIFCAB11).

Connecting the AAMCA to the Aurora AA1100 via the high-density connectors will provide a second Compact Flash socket, digital I/O and LEDs.

The 44-way 2mm pitch pin header provides access to the keyboard matrix and to the COM1 and COM2 RS232 serial ports.

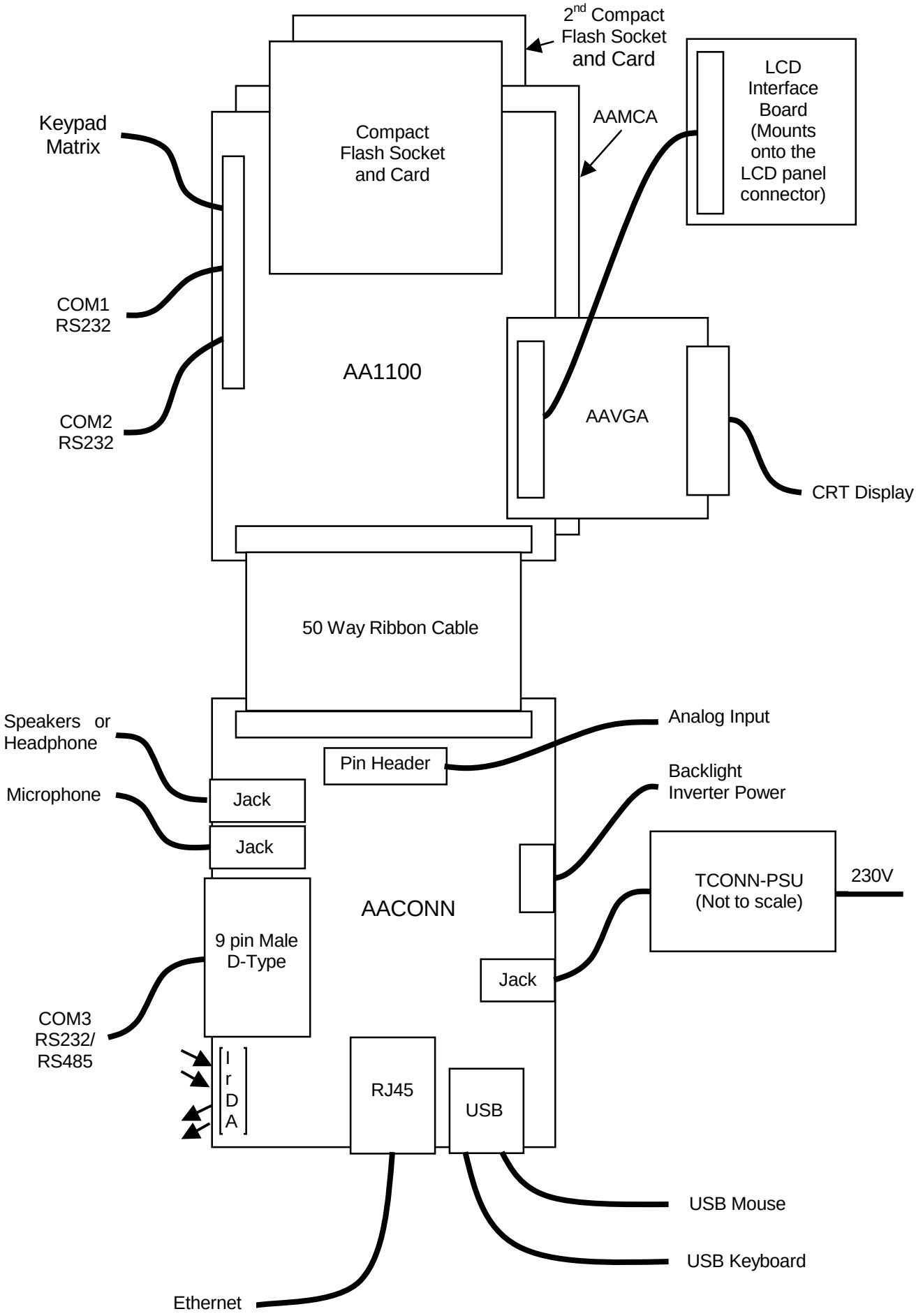

FIGURE 1 – A TYPICAL AURORA SYSTEM

1.5 LAUNCHPAD APPLICATION DEVELOPMENT KIT

DSP Design strongly recommends that you begin your development project by using one of the LaunchPad Application Development Kits. These are complete ready to use embedded computer systems that are waiting for your application to be placed into the solid-state disk. Versions exist for Windows CE and for Linux. Figure 2 shows the LaunchPad hardware. Not shown are the complete set of software, manuals and accessories that are included in the LaunchPad package.

Using the LaunchPad will greatly reduce your development time, so your product will get to market sooner at a fraction of the engineering costs normally associated with this product.

We have two objectives as you begin to use your new LaunchPad Application Development Kit.

Firstly, we expect that within an hour of receiving your LaunchPad you will have set up the hardware, connected it to your LAN and run the demonstration data acquisition application from a web browser.

Secondly, we expect that within a day you will have installed the development tools, compiled a sample application, downloaded it to the target hardware, and experimented with debugging this application remotely from the host computer.

So on the second day you can begin developing your real application.

For full details of the LaunchPad Application Development kits see our web site at www.dspdesign.com/launchpad.

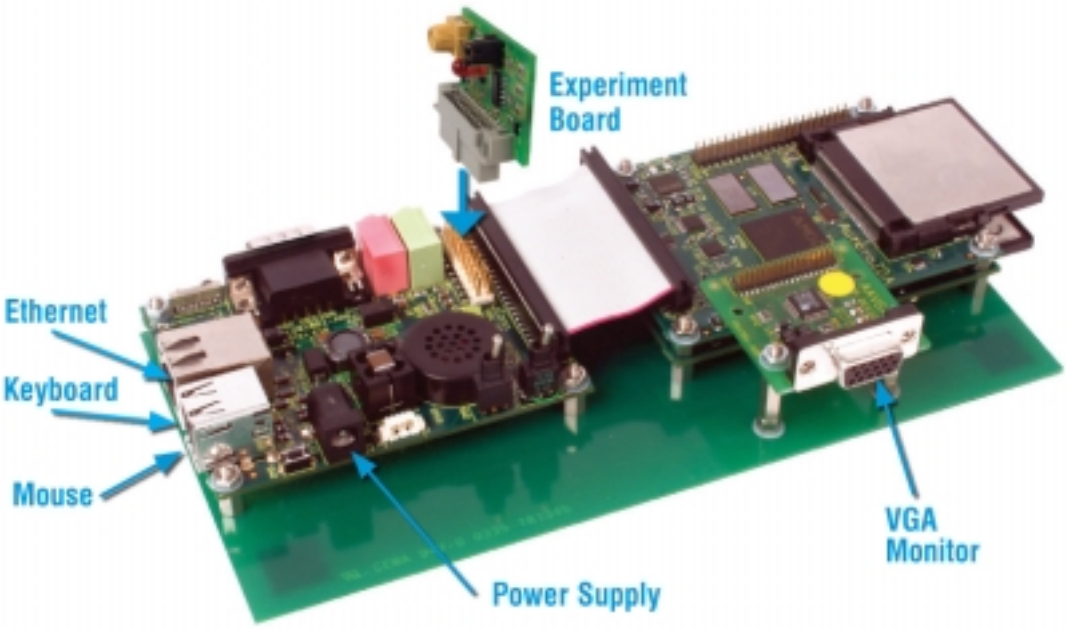

FIGURE 2 – THE AURORA BOARDS CONNECTED FOR LAUNCHPAD

2 HARDWARE

Figure 3 shows the block diagram of the Aurora AA1100.

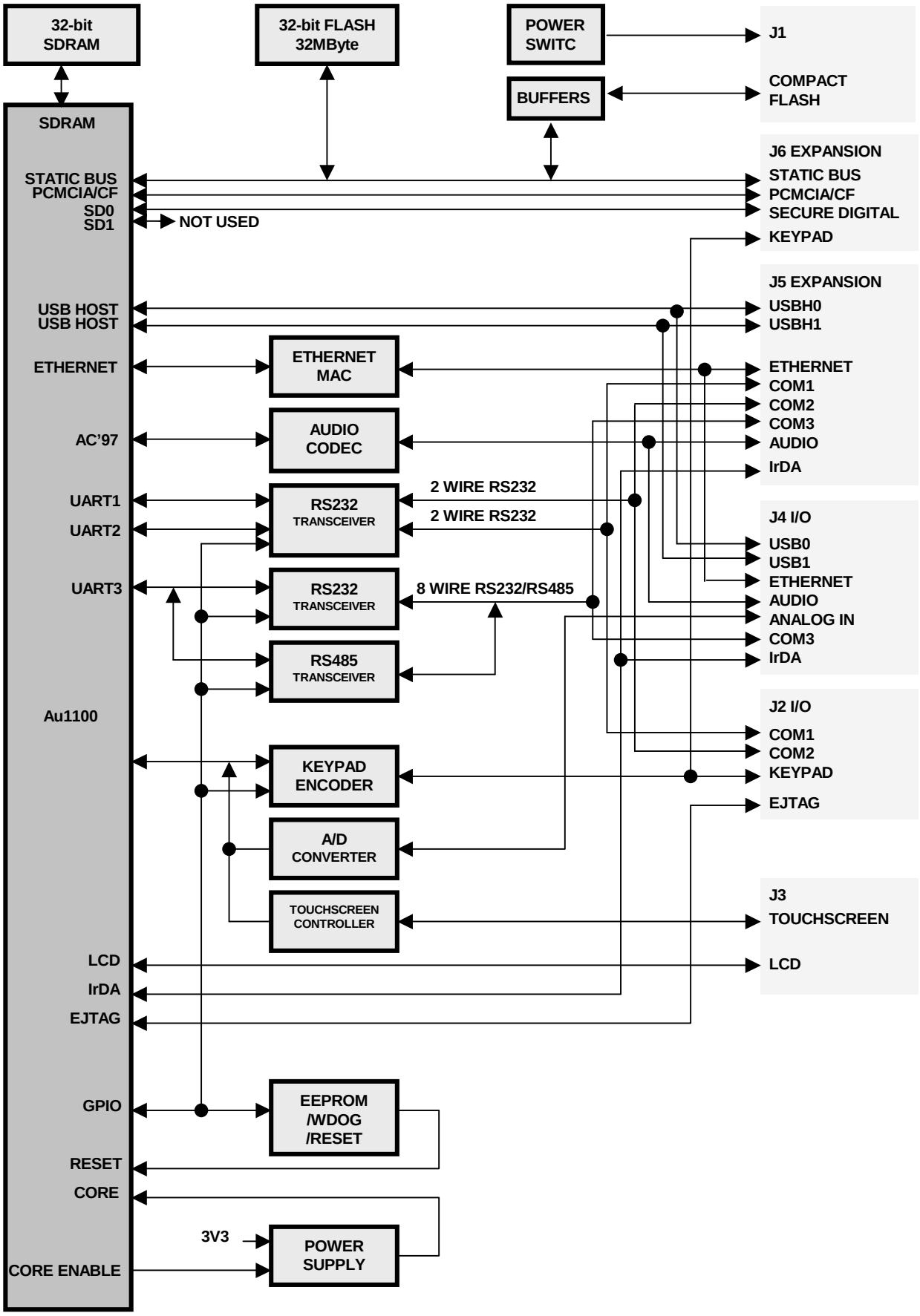

FIGURE 3 – AA1100 BLOCK DIAGRAM

2.1 PROCESSOR

The AMD Alchemy Au1100 processor is a highly integrated device based on a MIPS32 core. Figure 4 shows the Au1100 functional block diagram.

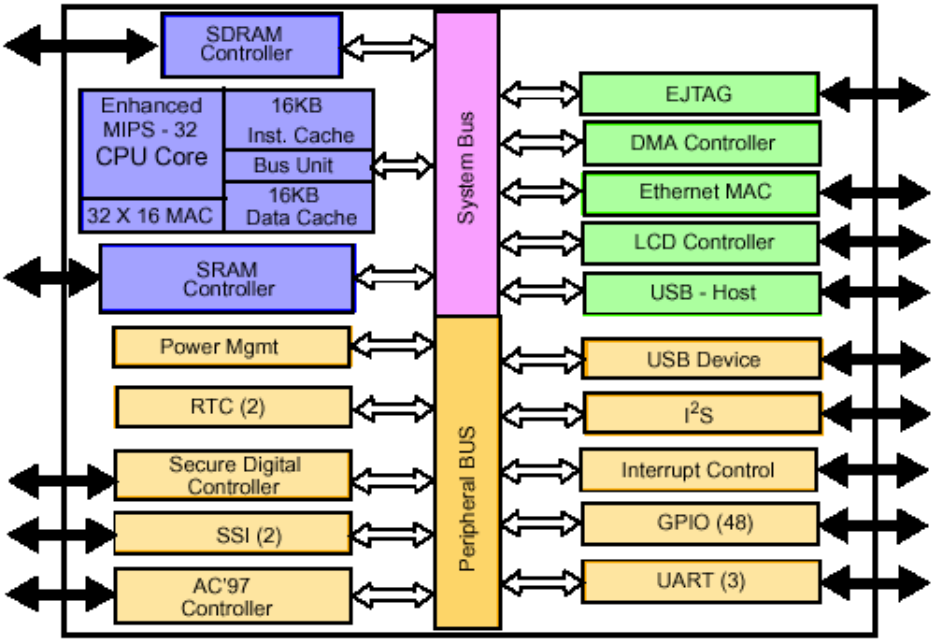

FIGURE 4 – Au1100 BLOCK DIAGRAM

The Au1100 is based on a 32-bit MIPS architecture and includes 16K byte instruction and data caches, a MAC and divide unit, memory controllers and highly integrated system peripherals.

The Au1100 is designed for maximum performance at very low power, dissipating less than 250mW at 400MHz. The Au1100 uses sophisticated power management, including a very low-power suspend state, to reduce power consumption for battery powered operation. The processor core requires a 1.2V power rail which is generated on the AA1100 board. This power supply is switched off in reset and suspend states to minimize power consumption.

The MIPS processor has a single memory address space. This is shared by memory, internal peripherals and external peripherals. There is no separate I/O address space as there is in an x86 processor.

Many of the engineering team that designed the Strong Arm processor (that later became the Intel XScale) were responsible for designing the Alchemy processor family. They used the MIPS processor core instead of the ARM core, and applied the same philosophy to create a processor with an exceptional performance per Watt.

2.2 SDRAM

Main memory is 32-bit wide Synchronous Dynamic RAM (SDRAM) soldered to the Aurora AA1100 PCB. As standard 64M bytes are fitted. This can be replaced by either more or less memory, subject to a minimum order quantity.

The SDRAM is connected to the Au1100 via a dedicated 32-bit wide bus and operates at a quarter of the processor clock (that is, normally 100MHz).

Some of the SDRAM is allocated to the internal LCD controller, using a technique referred to as UMA (unified memory architecture).

2.3 FLASH MEMORY

Program memory is implemented by two 16-bit wide AMD MirrorBit Flash chips soldered to the Aurora AA1100 PCB. As standard 32M bytes are fitted. This can be replaced by either more or less memory, subject to a minimum order quantity.

The Flash is 32-bit wide and is connected to the Static Bus. The Static Bus is also available on the expansion connectors which allows further memory and peripheral devices to be added externally.

The Flash memory typically contains the YAMON monitor program, the Eboot boot-loader and the Windows CE or Linux operating system.

The Windows CE implementation includes a Flash File System driver, allowing part of the Flash memory to be used as read-write file system.

2.4 COMPACT FLASH

The Aurora AA1100 features an on-board Compact Flash socket suitable for memory and I/O cards, thus providing both memory and peripheral expansion.

The Compact Flash socket is most commonly used for additional read-write memory storage.

Power switching circuitry and buffers are provided to isolate the Compact Flash card under software control to reduce power consumption when not required. The Compact Flash socket includes a ‘wake from suspend’ interrupt to the processor, which allows the processor to be woken from suspend state by an interrupt from a Compact Flash I/O card.

A further Compact Flash or PCMCIA socket can be added via the expansion connector with the addition of some simple control logic. Compact Flash and PCMCIA cards are identical from a software perspective and differ only mechanically and electrically.

A second Compact Flash socket is present on the AAMCA Expansion Board.

2.5 SERIAL PORTS

The Aurora AA1100 features three serial ports that are accessed as COM1, COM2 and COM3.

Each UART is similar to the industry standard 16550 UART and can be independently configured for 5-8 data bits, 1-2 stop bits, even, odd, mark or no parity and speeds up to 1.5Mbps (though the RS232 transceiver chip guarantees operation up to 1M bps only). All transmit and receive channels include a 16 byte FIFO.

2.5.1 COM1

COM1 is a two-wire RS232 port (TxD and RxD only). The COM1 signals are present on the 44-way ribbon cable connector J2 and the high-density inter-board connector J5.

The RS232 transceivers have an automatic power-down state that is transparent to users. The chips detect activity on the transmitter and receiver inputs, and valid RS232 signal levels on receiver inputs. When no activity or valid signals levels are detected the chips enter a low-power state after 20 seconds or so. COM1 and COM2 share one RS232 transceiver chip, so this power down occurs when both channels are inactive.

2.5.2 COM2

COM2 is a two-wire RS232 port (TxD and RxD only). The COM2 signals are present on the 44-way ribbon cable connector J2 and the high-density inter-board connector J5.

Activity on the COM2 RxD line can be used to wake the processor from suspend state. See section 5.5 for details. See section 2.5.1 for a discussion of the RS232 transceiver automatic power down.

2.5.3 COM3 IN RS232 MODE

COM3 can be either eight-wire RS232 or four-wire (two twisted pairs) RS485. The selection is made by the RS232 control signal available on connectors J4 and J5. By default, a pull-up resistor on the RS232 signal selects RS232 operation.

When operating as an RS232 port, COM3 is an eight-wire port (TxD, DTR, RTS, RxD, CTS, DSR, DCD and RI).

COM3 includes a wake from suspend interrupt to the processor, which allows the processor to be woken from suspend state by an active high signal on the RI signal. (This feature works even when COM3 is configured for RS485 operation). See section 5.5 for details. See section 2.5.1 for a discussion of the RS232 transceiver automatic power down.

The COM1 signals are present on the 50-way ribbon cable connector J4 and the high-density inter-board connector J5.

2.5.4 COM3 IN RS485 MODE

COM3 can be either eight-wire RS232 or four-wire (two twisted pairs) RS485. The selection is made by the RS232 control signal available on connectors J4 and J5. By default, a pull-up resistor on the RS232 signal selects RS232 operation, so users will need to connect this signal to GND for RS485 operation.

When operating as an RS485 port COM3 provides two twisted-pair (full-duplex) RS485 port.

The RS-485 configuration provides either half-duplex or full-duplex interfaces. In full-duplex mode one twisted pair is used for transmission and another twisted pair is used for reception. Full-duplex mode would normally be used in point-to-point communication between two computers.

In half duplex mode the, transmit and receive twisted pairs are connected together at the Aurora AA1100, by connecting the transmit pair to the receive pair on the cable. In this mode several boards can be connected to a single twisted pair, with no more than one board driving the cable at once. A suitable protocol needs to be agreed by all nodes on the twisted pair to ensure that only one computer transmits at any one time. Users should ensure that this protocol does not switch off the transmitter until the last bit of the character has been transmitted.

On the Aurora AA1100, the RS485 driver is controlled by the RTS bit of the COM3 UART. When RTS is off (inactive) the RS485 transceiver chip does not drive the transmit twisted pair cable. When RTS is set active the RS485 transceiver does drive the transmit twisted pair cable and the Aurora AA1100 can transmit. Note that the receiver part of the transceiver is always enabled. Thus in half-duplex mode COM3 will receive the characters that it transmits itself.

By default the RTS signal is set inactive at reset and in suspend state, so the RS485 transmitter is disabled. (A problem on the Rev B00 version of the AA1100 results in the transmitter being briefly enabled at reset and for a short period following resume from suspend state).

In RS-485 mode the DTR control output has no effect, and the CTS, DCD, DSR and RI status inputs are in the inactive, or unasserted, state (they will be seen as logic 0 by software).

No RS-485 termination resistors are provided on the Aurora AA1100. These must be provided externally if required. RS-485 is designed to run on twisted pair cable, typically with a characteristic impedance of 100 ohms or so. This cable is typically terminated at each end by a termination network of the same impedance as that of the cable. In practice, short cable lengths may not require the termination.

A feature of the RS-485 receiver is that its output goes inactive (high) when the input pins are open circuit.

When operating as an RS-485 port the COM3 RS-232 signals on connectors J4 and J5 are re-assigned as shown in Table 1.

SIGNAL NAME	RS485 INPUT/OUTPUT	DESCRIPTION	CONNECTOR PINS
TXD3	Input	Receive Data, inverting	J4-17, J5-52
RTS3	Input	Receive Data, non-inverting	J4-18, J5-21
DTR3	Output	Transmit Data, inverting	J4-19, J5-51
CTS3	Output	Transmit Data, non-inverting	J4-23, J5-49

TABLE 1 – COM3 RS485 PIN ASSIGNMENTS

2.6 IrDA

The IrDA (Infrared Data Association) peripheral is a serial device that uses an infrared serial bus. The port is IrDA 1.0 compliant and supports SIR mode speeds from 2.4 to 115.2Kbps. MIR and FIR modes are supported in hardware but are currently not supported by software.

There are two signals associated with IrDA operation – the IRTXD transmit data signal and the IRRXD receive data signal. An IrDA optical transceiver is located on the AACONN board.

The IrDA signals are present on the 50-way ribbon cable connector J4 and the high-density inter-board connector J5.

2.7 LCD OVERVIEW

The Aurora AA1100 LCD controller is capable of driving the latest industry standard 1-4 bit grayscale or 4-18 bit colour LCD panels. The controller performs the basic memory based frame buffer to LCD panel data transfer through use of a dedicated DMA controller with double buffering support. It also supports hardware rotation (for up to 320x240 pixels displays) and spatio-temporal dithering (frame rate modulation) for STN type LCD panels.

The controller is capable of driving both active (TFT) and passive (STN) LCD panels through multiplexed signal pins. Colour palette support is accomplished with a 256-entry 16-bit grayscale palette. TFT 16-bit mode allows the display of up to 65,536 simultaneous colours. A wide variety of LCD panels are supported through the use of programmable vertical and horizontal synchronization signals, bias signals and pixel clock rates.

A CRT can be driven with the addition of the AAVGA adapter board. A CRT would normally be of use for development purposes, but the AAVGA can be used for production as well, if required.

The Au1100 is very flexible in the display types and modes that it supports. The next three lists describe the capabilities of the chip, though users should note that not all of these displays and modes are supported by current software.

Panel Support

• 4/8-bit mono single passive matrix STN panels
• 8-bit color single passive matrix STN panels
• 16-bit color dual passive matrix STN panels
• 12/16-bit TFT panels
• 18-bit TFT panels (up to 65,536 colors)
• Panel sizes up to 800x600 are supported

Display Modes

• 1/2/4/8 bpp palletised TFT
• 12/16 bpp non-palletised TFT
• 1/2/4 bpp mono STN
• 1/2/4/8/12 bpp palletised colour STN
• 12 bpp non-palletised colour STN

Miscellaneous Features

• Double buffering support
• Hardware Swivel (90, 180, and 270 degrees) for up to 320x240 pixel displays
• Two pulse width modulation clocks to support digital control of contrast and brightness voltages (requires external RC filter circuits).

The AA1100's display interface is on connector J3. Appendix C contains the pin assignments of connector J3, which also carries touchscreen signals. The connector is an ETEC SS2-040-H070-11/11A or a Samtec FTS-120-01-L-DV. DSP Design offers 40-way ribbon cables in a number of standard lengths. Samtec can provide custom ribbon cable assemblies. Cables should be kept as short as possible to minimise signal integrity problems.

The signals that form the display interface are listed in Table 2.

SIGNALS	DESCRIPTION
LCD_D0-15	Pixel data. The allocation of data on these signals varies depending on the display type in use. See Table 3 for details.
LCD_PCLK	Pixel clock
LCD_LCLK	Line clock (HSYNC)
LCD_FCLK	Frame clock (VSYNC)
LCD_BIAS	A timing signal. The signal on this pin varies depending on the display type in use. See Table 3 for details.
LCD_VCCEN	A GPIO pin that is asserted high by software prior to the LCD signals being driven. It can be used to drive an external circuit to apply power to an LCD.
LCD_VEEEN	A GPIO pin that is asserted high by software prior to the LCD signals being driven. It can be used to drive an external circuit to generate a VEE supply voltage required by some LCDs.
LCD_BLEN	A GPIO pin that is asserted high by software prior to the LCD signals being driven. It can be used to enable a backlight power supply.
LCD_PWM0-1	Two output signals that can be programmed to have an oscillating signal of varying mark-space ratios. External RC filter circuits can be used to derive an analog voltage to adjust backlight brightness or display contrast. LCD_PWM0 is intended for backlight brightness control. At this point there is no software support for these signals.

TABLE 2 – DISPLAY INTERFACE SIGNALS

Table 3 shows how the LCD data signals are connected to different types of display. Users may be able to use this to connect to their own displays.

LCD SIGNAL NAME	MONO STN PANEL		COLOUR STN PANEL		COLOUR TFT PANEL	
	4-BIT	8-BIT	SINGLE	DUAL	12-bit	18-bit
LCD_D0	D0	D0	D0	D0	R0	R1
LCD_D1	D1	D1	D1	D1	R1	R2
LCD_D2	D2	D2	D2	D2	R2	R3
LCD_D3	D3	D3	D3	D3	R3	R4
LCD_D4	Low	D4	D4	D4	G0	R5
LCD_D5	Low	D5	D5	D5	G1	G0
LCD_D6	Low	D6	D6	D6	G2	G1
LCD_D7	Low	D7	D7	D7	G3	G2
LCD_D8	Low	Low	Low	D8	B0	G3
LCD_D9	Low	Low	Low	D9	B1	G4
LCD_D10	Low	Low	Low	D10	B2	G5
LCD_D11	Low	Low	Low	D11	B3	B1
LCD_D12	Low	Low	Low	D12	Low	B2
LCD_D13	Low	Low	Low	D13	Low	B3
LCD_D14	Low	Low	Low	D14	Low	B4
LCD_D15	Low	Low	Low	D15	Low	B5
LCD_BIAS	Square-wave signal of half the HSYNC frequency (could be programmed for alternative frequencies).				Active high display enable.	

TABLE 3 – LCD CONTROLLER DATA PIN USEAGE

Since there are only 16 data bits available from the Au1100 and up to 18 bits (six each of red, green and blue) of data input to the LCD, it is necessary to tie the display's unused least significant bits to GND.

2.8 LCD TYPES SUPPORTED

There are a large number of LCD panels on the market today, but little standardisation. Many displays require specialised interfaces with additional electronics and non-standard connector types. In principle most of these displays can be driven by the AA1100, provided the correct support circuitry and connectors are provided.

To simplify the process of attaching an LCD panel to the Aurora AA1100, DSP Design has pre-selected a range of colour TFT, colour STN and mono STN panels and provided suitable interface boards and operating system support for them. Customers are urged to use these panels where possible, at least for development work. DSP Design may be able to provide assistance in creating customised support electronics for other displays on a consultancy basis.

The list of display types is given in Table 4, together with the model that DSP Design used to test the display timing and resolution. Note that different display models may require adjustments to the Au1100 display timing registers, to adjust vertical and horizontal positions. This accounts for the two entries for the 800 x 600 TFT.

The LP1100Config program is used to select a different display type from a drop-down list. When a selection is made the display parameters are stored in the persistent registry. In the event that you make a selection and are unable to view the Windows CE GUI on the next boot you will have to erase the persistent registry to return to 640 x 480 CRT operation.

DISPLAY TYPE	MODEL USED FOR TESTING
240 x 320 Colour STN	Kyocera KCS038AA1AAC-G21
320 x 240 TFT	Sharp LQ038Q5DR01
320 x 240 Colour STN	Hitachi SC09Q002-A
640 x 240 Colour STN	Kyocera KC062HV1AA-A21
640 x 480 CRT	CRT
640 x 480 TFT	NEC6448BC20-08E and Sharp LQ64D343
800 x 600 CRT	CRT
800 x 600 TFT	Sharp LQ12S41
800 x 600 LVDS	Samsung LTN104S2-L01 (This is a TFT display with an LVDS interface).

TABLE 4 – DISPLAY TYPES SUPPORTED

The Aurora AA1100 was designed to drive 3.3V-powered LCDs. Some LCDs when powered from 5V will not operate with the 3.3V levels generated by the Aurora AA1100.

2.9 LCD INTERFACE BOARDS AND KITS

To facilitate connecting to some of the above LCDs, DSP Design has created a number of interface boards and display kits.

The interface boards plug into the 40-way ribbon cable from the AA1100 and also into the LCD, thus routing the AA1100's display signals to the appropriate pins on the LCD. Depending on the LCD type they may also generate additional voltages, provide connections to backlight inverters and touchscreens etc.

The kits include the LCD, backlight inverter, interface boards, touchscreen and cables – everything you need to get the display working with the AA1100.

2.9.1 Support for 240 x 320 TFT

The AATFT038KIT is a kit that supports the 3.8" Sharp LQ038Q5DR01 240 x 320 TFT display. The kit also includes an AALQ038 interface board, a TDK CXA-L0605-VJL backlight inverter, a touchscreen (attached to the display), a TFTIF-CAB11 40-way ribbon cable assembly and a backlight cable assembly.

The AALQ038 interface board converts the Aurora AA1100 interface signals to those required by the LCD. The board mounts directly onto the display's connector and can be secured using one of the panel mounting points. A TFTIF-CAB11 ribbon cable assembly is then used to connect the AALQ038 to the Aurora AA1100. The interface board also has a connector for the touchscreen, which is attached to the display. The

backlight cable assembly connects between the backlight inverter, AALQ038 and AACONN.

This kit can be ordered using the part number AATFT038KIT.

Alternately, most of the components of this kit may be ordered individually. Please refer to section B.3 Display Accessories.

2.9.2 Support for 640 x 480 TFT

The AATFT064KIT is a kit that supports the 6.4" NEC NL6448BC20-O8E TFT display. The kit also includes an AANL064 interface board, an AANLTS interface board, a 65PWB31 backlight inverter, a touchscreen (attached to the display), a TFTIF-CAB11 40-way ribbon cable assembly and a backlight cable assembly.

The AANL064 interface board converts the Aurora AA1100 interface signals to those required by the LCD. The board mounts directly onto the display's connector. A TFTIF-CAB11 ribbon cable assembly is then used to connect the AANL064 to the Aurora AA1100. The touchscreen is connected to the AANLTS interface board. The backlight/touchscreen cable assembly connects between the AANLTS, AANL064, backlight inverter and AACONN.

This kit can be ordered using the part number AATFT064KIT.

Alternately, most of the components of this kit may be ordered individually. Please refer to section B.3 Display Accessories.

2.9.3 CRT Support

The AAVGA interface board converts the Aurora AA1100 interface signals to those required by a standard CRT or LCD monitor. The board plugs directly into the Aurora AA1100 and provides the standard 15 way D-type connector.

2.9.4 LVDS Support

Many of the larger LCD panels (800x600 and above) use Low Voltage Differential Signaling (LVDS) interfaces instead of the traditional parallel interfaces. The TFTIFLVDS Interface board converts the Aurora AA1100 LCD interface signals into LVDS. The board plugs directly into the Aurora AA1100 and connects to the LCD panel via a twisted pair cable assembly. There are two types of LVDS interface (using four or five twisted pairs). Contact DSP Design for assistance in selecting an LVDS interface for your display.

2.9.5 Other Displays

As mentioned above, users are strongly encouraged to choose one of the supported displays, for development work at least, and preferably for production. If a different display type must be used then some additional hardware and software work may be required.

The hardware work may be to create a transition PCB that matches the AA1100 display connector to the display's connector, as well as adding circuitry for supplying non-standard voltages, interfaces to backlight power supplies etc.

From a software viewpoint, it may also be necessary to adjust LCD timing register values, for example to correctly position the image on the LCD.

DSP Design may be able to provide assistance with this on a consultancy basis.

2.10 ETHERNET

The Aurora AA1100 provides a 10/100 Base-T Ethernet port. The Au1100 chip includes the Ethernet MAC (Media Access Controller), and an external PHY (Physical layer) chip provides connection to transmit and receive twisted pairs.

The Aurora AA1100's Ethernet circuit is connected to the network's twisted pair cable via a small circuit, which includes the isolation transformer, EMC filters and an RJ45 connector with status LEDs. These components have been omitted from the Aurora AA1100 to allow the RJ45 connector to be positioned at the system's enclosure. This circuit is present on the AACONN.

The signals that form the Ethernet interface are listed in Table 5.

SIGNALS	DESCRIPTION
N0_TXP and N0_TXN	Transmitter twisted pair, positive and negative. Connect to one side of the isolation transformer, with 3.3V applied to the centre tap.
N0_RXP and N0_RXN	Receiver twisted pair, positive and negative. Connect to one side of the isolation transformer.
/LINKLED	Link activity LED, goes low when an Ethernet link is established. An LED and current-limiting resistor connect between this pin and 3.3V
/LANLED	LAN activity LED, goes low when data is transmitted or received. An LED and current-limiting resistor connect between this pin and 3.3V

TABLE 5 – ETHERNET SIGNAL DESCRIPTION

The Ethernet signals are present on the 50-way ribbon cable connector J4 and the high-density inter-board connector J5.

2.11 USB

The Aurora AA1100 contains two USB 1.1 compliant host ports. Although hardware exists for one of the host ports to be configured as a device port, there is currently no software support.

The USB signaling is carried on twisted pairs – one twisted pair per port.

The signals that form the USB interface are listed in Table 6.

SIGNALS	DESCRIPTION
USBH0P and USBH0N	USB host port 0 twisted pair, positive and negative. These signals can be reconfigured as a USB device port, although there is no software support for this at present.
USBH1P and USBH1N	USB host port 1 twisted pair, positive and negative.

TABLE 6 – USB SIGNAL DESCRIPTION

The Aurora AA1100's USB circuit is connected to a USB device via a small circuit, which includes the power switch, EMC filters, protection diodes and connector. These components have been omitted from the Aurora AA1100 to allow the USB connectors to be positioned at the system's enclosure. This circuit is present on the AACONN.

USB devices require a 5V supply, which is not otherwise required by the Aurora AA1100 and which therefore must be supplied from an external PSU. This is available on the AACONN when using the TCONN-PSU. The external PSU must be capable of supplying either 100mA or 500mA per port, depending on the type of USB device used. For mouse and keyboard operation 100mA is sufficient.

The USB signals are present on the 50-way ribbon cable connector J4 and the high-density inter-board connector J5.

2.12 AUDIO

The Aurora AA1100 includes an audio record/replay subsystem, providing mono microphone input, stereo headphone output, mono speaker output and stereo line input and output. The circuit is implemented partly inside the Au1100 processor, and partly within an AC97 codec, which provides the analog to digital and digital to analog conversions.

The signals that form the audio interface are listed in Table 7. Not all of the signals present on the AC97 codec are accessible in the standard AA1100 design.

SIGNALS	DESCRIPTION
MIC1	Microphone input. An external DC blocking capacitor is required.
MICGND	A signal GND for the microphone
MICBIAS	This output provides a reference voltage of typically 2.9V. It can be used with an external resistor for biasing electret type microphones.
LINEINL and LINEINR	Stereo line inputs. The DC blocking capacitors are fitted to the Aurora AA1100.
AINGND	A signal GND for the LINEIN signals.
LINEOUTL and LINEOUTR	These are designed to differentially drive an 8-ohm mono speaker without the need for DC blocking capacitors. They can also be used as a stereo line output pair with the addition of two external DC blocking capacitors and protection resistors.
AOUTGND	A signal GND for the LINEOUT and HPOUT signals.
HPOUTL and HPOUTR	These are designed to drive 16-ohm or 32-ohm headphones with the addition of two external DC blocking capacitors.
OUT3	An additional audio output signal that can be configured by software for a number of purposes (not currently supported).
AUDIOGPIO	A GPIO input signal that can be used to detect the presence of headphones, switches etc. Not currently supported by software.

TABLE 7 – AUDIO SIGNAL DESCRIPTION

The AACONN provides a mono microphone input via a 3.5mm socket, stereo line output via a 3.5mm socket and the associated passive components. The AACONN also includes a mono speaker connected across LINEOUTR and LINEOUTL.

MICGND, AINGND and AOUTGND are connected to GND at a single point on the Aurora AA1100.

The AC97 codec used is the Wolfson WM9712. This chip has many non-standard features. It also has a number of additional input and output signals that we have not been able to bring to connectors, due to a lack of pins. If you have a volume requirement for features that are supported by the WM9712 and which are not described in this section, DSP Design may be able to implement your requirements on a consultancy basis.

2.13 ANALOG TO DIGITAL CONVERTER

The Aurora AA1100 includes a four-channel 12-bit analog to digital converter chip. The converter allows external analog signals to be monitored.

The analog to digital converter is a Maxim MAX1247. It has four inputs, called ADC0, ADC1, ADC2 and ADC3. The input voltages can be between ADCGND (0V) and 3V3 (+3.3V). The input voltages must not extend beyond this range, or else internal protection diodes will begin conducting. If there is a chance of the input voltages exceeding the supply rails then current limiting resistors must be added external to the Aurora AA1100, to limit this current to 4mA. This same restriction applies when the power is switched off - if the analog voltage is still applied to the A/D chip when the Aurora AA1100 is powered off then the internal protection diodes will conduct, and so the current limiting resistors must be used.

The voltages are measured as a proportion of a reference voltage, VREF. VREF defines the input voltage that provides the full-scale digital reading. The VREF pin on the A/D is connected to the on-board 3V3 (+3.3V) supply voltage.

Measurements can be made as single-ended or differential measurements, as programmable options. In single-ended mode each of the four inputs is measured with respect to the ADCGND (0V) pin. (ADCGND is connected to the GND at a single point on the Aurora AA1100). In differential mode the difference between two inputs is measured. (Contact DSP Design if you need to use differential mode).

Measurements can also be made as unipolar or bipolar, as programmable options. In unipolar mode an input voltage of ADCGND will give a digital output of 0000h, and an input voltage of VREF will give a digital output of 0FFFh. In bipolar mode an input voltage of VREF/2 will give a digital output of 0000h, an input voltage of VREF will give a digital output of 07FFh, and an input voltage of ADCGND will give a digital output of 800h. Voltages between ADCGND and VREF/2 are treated as negative voltages, and converted into two's complement negative numbers. It is probably only sensible to use bipolar mode in conjunction with differential mode, where the difference between two inputs can be negative as well as positive.

In some applications the analog inputs can be susceptible to noise. Filter capacitors can optionally be fitted on the input pins of the A/D converter. Typically 10nF 0603 capacitors could be used. By default these are not fitted. Table 8 identifies the capacitor sites for each of the four channels. The component placement diagrams in Appendix A can be used to locate these capacitors. Users should be warned that some op-amps are unstable when driving capacitive loads.

The A/D converter input signals are present on the 50-way ribbon cable connector J4 and the high-density inter-board connector J5.

On the Rev B01 and B03 boards ADC3 is also routed to the IN pin of the touchscreen controller.

A/D CHANNEL	FILTER CAPACITOR
ADC0	C35
ADC1	C36
ADC2	C37
ADC3	C34

TABLE 8 – A/D CONVERTER FILTER CAPACITOR SITES

The Au1100 communicates with the A/D chip through a synchronous serial interface (SSI) serial link. The Au1100 processor includes an SSI interface functional block, which is also used for the touchscreen controller, the keypad encoder and possibly external SSI peripherals. Using this communications link the Au1100 may configure the A/D converter or make conversions.

Since the A/D converter shares the SSI bus with other peripherals, a mechanism is provided to enable only one peripheral at a time, so that SSI accesses reach that peripheral and not the others. This is achieved using three of the Au1100's GPIO pins. These pins must be controlled by device driver software, which must set the pins appropriately for the duration of the SSI transfer. Such software must prevent

contention for the SSI devices. Table 9 lists the settings of the GPIO pins for each of the SSI peripherals.

GPIO PINS			SSI FUNCTION SELECTED
/TSEN	/ADCEN	/KPEN	
1	1	1	Off-board SSI device (Rev B01 and Rev B03 boards only)
1	1	0	Keypad Encoder
1	0	1	A/D converter
1	0	0	Reserved
0	1	1	Touchscreen controller
0	1	0	Reserved
0	0	1	Reserved
0	0	0	Reserved

TABLE 9 – SELECTING SSI PERIPHERALS

2.14 TOUCHSCREEN

The Aurora AA1100 includes a four-wire touchscreen controller as standard. A five-wire controller can be fitted subject to a minimum order quantity.

The touchscreen controller has two auxiliary inputs – one measures a proportion of the 3.3V power supply rail (which could allow the A/D converter readings to be calibrated. On the Rev B01 and B03 boards the other input is also connected to the ADC3 Pin, which allows for a depopulated option – no A/D converter chip but still having the possibility of measuring one external analog signal. At the time of writing there is no software support for these two analog measurements.

Table 10 provides a description of the touchscreen signals.

SIGNALS	DESCRIPTION
TSXP	Touchscreen X+ terminal. Typically X+ is the right-hand terminal.
TSXN	Touchscreen X- terminal. Typically X- is the left-hand terminal.
TSYP	Touchscreen Y+ terminal. Typically Y+ is the top terminal.
TSYN	Touchscreen Y- terminal. Typically Y- is the bottom terminal.

TABLE 10 – TOUCHSCREEN SIGNAL DESCRIPTION

The touchscreen signals are present on the 40-way ribbon cable connector J3. This connector also carries the LCD interface signals. Many of DSP Design's LCD interface boards connect to both an LCD and a touchscreen.

The touchscreen controller has two additional analog inputs, which are not currently supported by software. The VBATT pin is connected to the 3.3V power supply rail, and can thus be used to measure this power supply rail. The IN pin is connected to GND on the Rev B00 version of the AA1100, but is connected to A/D converter ADC3 on the Rev B01 version.

The Au1100 communicates with the touchscreen controller chip through a synchronous serial interface (SSI) serial link. The Au1100 processor includes an SSI

interface functional block, which is also used for the A/D converter, the keypad encoder and possibly external SSI peripherals. Using this communications link the Au1100 may configure the touchscreen controller and read the stylus position. See section 2.13 for details of this.

2.15 KEYPAD

The Aurora AA1100 includes a keypad encoder capable of scanning, debouncing and encoding keypad matrices of up to 14 columns by 8 rows. Smaller size matrices can be accommodated, by simply leaving unused pins open circuit. The keypad encoder is a Semtech UR5HCSPI-SA01.

When active, the encoder selects one of the column lines (COL0-13) every 512us and then reads the row data lines (ROW0-7). A key closure is detected as a zero in the corresponding position of the matrix. A complete scan cycle for the entire keyboard takes approximately 9.2ms. Each key found pressed is debounced for 20ms. Once the key is verified, the corresponding key code is loaded into the transmit buffer and an interrupt is generated to the processor. The transmit buffer contains both make and break key codes.

In any scanned contact switch matrix, whenever three keys defining a rectangle on the switch matrix are pressed at the same time, a fourth key positioned on the fourth corner of the rectangle is also sensed as being pressed. This is known as the “ghost” or “phantom” key problem. To eliminate this problem, keys that are intended to be used in combinations (e.g. CTRL+ALT+DEL) should be placed in the same row or column.

Table 11 provides a description of the touchscreen signals. The keypad signals are available on the 44-way ribbon cable connector J2 and the high-density inter-board connector J6. Due to a PCB error, prior to Revision B03 PCBs the keypad signal SW0 on the keypad encoder chip was not connected to I/O connectors. Contact DSP Design if this is a problem for you.

SIGNALS	DESCRIPTION
ROW0-7	Keypad rows (inputs)
COL0-13	Keypad columns (outputs)
XSW	External switch input
SW0	External switch input
LED	General purpose Input/Output – can be used to drive an LED

TABLE 11 – KEYPAD SIGNAL DESCRIPTIONS

The Au1100 communicates with the keypad encoder chip is through a synchronous serial interface (SSI) serial link. The Au1100 processor includes an SSI interface functional block, which is also used for the touchscreen controller, the A/D converter and possibly external SSI peripherals. Using this communications link the Au1100 may configure the keypad controller and read the key presses. See section 2.13 for details of this.

2.16 EXTERNAL SSI DEVICE

The Au1100 processor includes a synchronous serial interface (SSI) functional block, which is used for the touchscreen controller, the A/D converter and keypad controller. SSI interfaces are also known as SPI, QSPI and Microwire interfaces. See section 2.13 for details of this.

On Rev B01 and B03 boards this interface can, in principle, be used for external SSI peripherals. It should be noted that at this point there is no software support for external SSI devices. DSP Design may be able to provide software support on a consultancy basis.

Table 12 provides a description of the SSI signals. The signals are available on the high-density connector J5.

SIGNALS	DESCRIPTION
/EXT_SDEN	Active low chip select to external SSI device. It will be asserted during any SSI access to chips other than the three on-board SSI devices.
SCK	Clock
SDOUT	Serial data output from the Au1100
SDIN	Serial data input to the Au1100

TABLE 12 – SSI SIGNAL DESCRIPTIONS

2.17 SERIAL EEPROM AND I2C INTERFACE

The Aurora AA1100 uses a 512-byte serial EEPROM for storing configuration information. The same chip (a Xicor X4043) also provides a watchdog timer function and a power-on reset function.

The serial X4043 uses an I2C bus. The I2C addresses are 0A0h for the serial EEPROM and 0B0h for the watchdog timer.

The I2C signals are Au1100 processor GPIO pins, which are manipulated by software to communicate with the I2C devices. Table 13 provides a description of the I2C signals.

SIGNALS	DESCRIPTION
SCL	I2C clock. Driven by the Au1100 processor.
SDA	I2C data. This is a bi-directional signal.

TABLE 13 – I2C SIGNAL DESCRIPTIONS

The signals are available on the high-density connector J6. On the Rev B01 version of the AA1100 the I2C signals are also available on the 44-way ribbon cable connector J2. From here it can be used for accessing external I2C peripherals. It should be noted that at this point there is no software support for external I2C devices. DSP Design may be able to provide software support on a consultancy basis.

2.18 COUNTER/TIMERS

The Au1100 contains two programmable counters designed for use as a time of year clock (TOY) and real time clock (RTC). Each counter operates identically, using the same register set and 32.768KHz source.

Because the TOY continues counting through suspend, a TOY counter match can be used as a wake-up source. The RTC, however, will power down in suspend state.

2.19 HARDWARE RESET

A full set of hardware reset options exist for the Aurora AA1100.

2.19.1 General

The reset circuit is built around the X4043 serial EEPROM chip, which provides reset functions as well as memory. This chip includes a power supply monitor and a watchdog timer. An external reset signal is also provided.

To avoid glitches on the reset signal, the X4043 will always hold the reset signal asserted for approximately 200ms, ensuring all circuitry is properly reset.

The X4043 chip's reset output, connected to a signal called /RESET, drives the Au1100 processor's reset input pin, as well as the reset pins of some peripherals.

2.19.2 Power Supply Monitor

The X4043 monitors the +3.3V supply voltage. When the supply drops below about 2.7V the X4043 will assert the /RESET signal. Once the input voltage returns to within specification, the reset signal will be released after a further 200ms. This circuit prevents power "brown-out" causing unpredictable behaviour.

Users should note that if the voltage drop across the cables that link the external power supply to the Aurora AA1100 is excessive then the power supply monitor may reset the Aurora AA1100. This may also happen if there are noise spikes on the power supply. It is recommended that all power supply cables be as thick and short as possible to minimize the voltage drop across them.

2.19.3 Watchdog Timer

A watchdog timer exists in the X4043. The function of a watchdog timer is to reset a computer if the software has crashed. The correct operation of the timer relies on software to access the watchdog timer hardware on a regular basis. If the software crashes, the watchdog timer will not be "kicked" and so eventually it will time-out and reset the computer.

The watchdog timer is enabled, by writing an enable command to the X4043. Once this has been initiated, an internal clock to the X4043 starts counting and will continue

to count until it times out, until the watchdog timer is "kicked" by the user's application software, or until the watchdog timer is disabled by a disable command sent to the X4043.

The watchdog timer period can be set to approximately 1.4s, 600ms or 200ms. Once it has been enabled the watchdog timer must be accessed repeatedly by the user's software. If the watchdog timer is allowed to time out the X4043 chip will issue a hardware reset.

At present there is no software support for the watchdog timer.

2.19.4 The /RESET Signal

The Aurora AA1100 can be reset by pulling the /RESET signal low. In this way a system reset can be generated by an external signal or switch.

The AACONN has a push button switch (SW3) connected between /RESET and GND. Pressing this switch momentarily will reset the system.

The /RESET signal should be used to reset any of the user's circuitry on the expansion bus.

The /RESET signal is present on the 44-way ribbon cable connector J2, the 50-way ribbon cable connector and the high-density inter-board connector J5.

2.20 GENERAL-PURPOSE INPUT/OUTPUTS

The Au1100 processor chip has many general-purpose input/output (GPIO) pins, most of which have alternative functions (configurable by software) and most of which are assigned functions on board the Aurora AA1100. Nevertheless, some GPIO pins are available for use in users' applications.

For most purposes, the Aurora AA1100 provides three general-purpose input/output pins – GPIO6, GPIO17 and GPIO18. All three have pull-up resistors. All three can be programmed to generate interrupts when configured as inputs. GPIO6 and GPIO17 may be used by bootstrap software to determine boot operation, but thereafter become available for other uses. See the LaunchPad Developer's Guides and release notes for a description of the use of these pins by bootstrap code.

On Rev B01 and B03 boards GPIO6 serves as a wake from suspend signal. Taking this pin low will wake the AA1100 from the suspend state. See section 5 for further details.

GPIO6 and GPIO17 are present on the 50-way ribbon cable connector J4 and the high-density inter-board connector J5. GPIO18 is present on the high-density inter-board connector J6.

On Rev B01 and Rev B03 boards, GPIO200 is made available on the inter-board connector J6. It has no function allocated to it, so could be used for user-defined purposes.

As some GPIO pins are intended for use by other off-board functions (support for a second Compact Flash socket, for instance), it is possible that some GPIO pins could be redeployed for users' applications, if they were not otherwise in use. However this would involve software work. DSP Design may be able to provide assistance with this on a consultancy basis.

At the time of writing there is no software support for users to make use of the GPIO pins from within their software. This situation may change in the future. Until then, access to GPIO pins from within software requires work by DSP Design on a consultancy basis.

Appendix D includes a full list of the GPIO pins and their uses.

2.21 MEMORY MAP

The peripheral devices on the Au1100 contain memory-mapped registers visible to software. The addresses are 36 bits wide. Table 14 shows the memory map for the peripheral devices and physical memory. For full details see the Au1100 Data Sheet.

Start Address	End Address	Size (MB)	Function
0x0 00000000	0x0 0FFFFFFF	256	Memory KSEG 0/1
0x0 10000000	0x0 11FFFFFF	32	I/O Devices on internal Peripheral Bus
0x0 12000000	0x0 13FFFFFF	32	Reserved
0x0 14000000	0x0 17FFFFFF	64	I/O Devices on internal System Bus
0x0 18000000	0x0 1FFFFFFF	128	Memory Mapped
0x0 18000000	0x0 1803FFFF	256k	Typical address for /CE1
0x0 19000000	0x0 1903FFFF	256k	Typical address for /CE2
0x0 20000000	0x0 7FFFFFFF	1536	Memory Mapped
0x0 80000000	0x0 EFFFFFFF	1792	Memory Mapped
0x0 F0000000	0x0 FFFFFFFF	256	Debug Probe
0x1 00000000	0xC FFFFFFFF	4096	Reserved
0xD 00000000	0xD FFFFFFFF	4096	I/O Device
0xE 00000000	0xE FFFFFFFF	4096	External LCD Controller Interface
0xF 00000000	0xF FFFFFFFF	4096	Compact Flash Interface

TABLE 14 – AA1100 MEMORY MAP

The on-board Flash is located at 0x01E00000. Table 15 shows the allocation of memory within the Flash memory chips for Windows CE .NET.

MEMORY OFFSET	MEMORY ADDRESS	USE
0 – 7FFFFh	BE000000h – BE07FFFFh	Persistent Registry
80000h – 15FFFFFh	BE080000h – BF5FFFFFh	Operating System Image
1600000h – 1BFFFFFh	BF600000h – BFBFFFFFh	Flash File System
1C00000h – 1CFFFFFh	BFC00000h – BFCFFFFFh	YAMON
1D00000h – 1DFFFFFh	BFD00000h – BFDFFFFFh	Eboot
1E00000h – 1EFFFFFh	BFE00000h – BFEFFFFFh	Ethernet MAC address
1F00000h – 1FFFFFFh	BFF00000h – BFFFFFFFh	Reserved

TABLE 15 –USE OF THE 32M BYTE FLASH MEMORY

Table 16 shows the memory map for the Au1100 internal system bus devices mapped at addresses starting from 0x014000000.

Start Address	End Address	Size (KB)	Function
0x0 14000000	0x0 14000FFF	512	SDRAM Memory Controller
0x0 14001000	0x0 14001FFF	512	SRAM/FLASH Memory Controller
0x0 14002000	0x0 14002FFF	512	DMA
0x0 14004000	0x0 14004FFF	512	Ethernet DMA
0x0 15000000	0x0 15005FFF	512	LCD Controller

TABLE 16 – INTERNAL SYSTEM BUS MEMORY MAP

Table 17 shows the memory map for the Au1100 internal peripheral bus devices mapped at addresses starting from 0x010000000.

Start Address	End Address	Size (MB)	Function
0x0 10000000	0x0 100FFFFF	1	AC97 Controller
0x0 10100000	0x0 101FFFFF	1	USB Host
0x0 10200000	0x0 102FFFFF	1	USB Device
0x0 10300000	0x0 103FFFFF	1	IrDA
0x0 10400000	0x0 104FFFFF	1	Interrupt Controller 0
0x0 10500000	0x0 105FFFFF	1	Ethernet MAC
0x0 10600000	0x0 106FFFFF	1	SD Controller
0x0 10700000	0x0 10FFFFFF	9	Reserved
0x0 11000000	0x0 110FFFFF	1	I2S Controller
0x0 11100000	0x0 111FFFFF	1	UART0
0x0 11200000	0x0 112FFFFF	1	UART1
0x0 11300000	0x0 113FFFFF	1	Reserved
0x0 11400000	0x0 114FFFFF	1	UART3
0x0 11500000	0x0 115FFFFF	1	Reserved
0x0 11600000	0x0 116FFFFF	1	SSI
0x0 11700000	0x0 117FFFFF	1	Secondary GPIO
0x0 11800000	0x0 118FFFFF	1	Interrupt Controller 1
0x0 11900000	0x0 119FFFFF	1	System Control

TABLE 17 - INTERNAL PERIPHERAL BUS MEMORY MAP

3 STAND-ALONE OPERATION AND EXPANSION BUS

The Aurora AA1100 will operate as a stand-alone single board computer, or it can use the expansion bus interface to expand its capabilities.

3.1 STAND-ALONE OPERATION

The Aurora AA1100 will operate as a single board computer with the addition of the appropriate peripherals and a single +3.3V power supply.

The board was designed such that most peripherals that are appropriate for use in a stand-alone system are available on three ribbon cable connectors – J2, J3 and J4. Appendix C gives the pin assignments for these connectors, but in summary, J2 carries keypad, COM1 and COM2 signals, J3 carries the display and touchscreen signals, and J4 carries USB, Ethernet, COM3, IrDA, audio and A/D signals.

Power can be supplied via the ribbon cable connectors J2 and J4. Users should take care to provide power to the Aurora AA1100 through cables that are as short and thick as possible, and to make use of as many of the power and ground pins as possible, connecting them in parallel. This is to minimise the voltage drop that will occur through the resistance of the power cables.

3.2 EXPANSION BUS

The expansion bus provides a general-purpose interface to a variety of external peripherals and memory devices. Either 8-bit or 16-bit peripherals may be added. Some GPIO pins are available for use as interrupt request signals.

The signals that form the expansion bus are listed in Table 18.

SIGNALS	DESCRIPTION
DATA0-15	Data bus. The Au1100 has a 32-bit data bus, but only the lower 16 bits are available for external devices.
ADDR0-27	Address bus. The Au1100 has a 32-bit address bus, but only the lower 28 bits are available for external devices.
/CE0-3	Active low chip selects. Each chip select is programmed to be active over a particular address range, and is associated with a particular type of device. /CE0 is reserved for use by the on-board flash memory. /CE3 is reserved for Compact Flash sockets. /CE1 and /CE2 are available for external devices.
/OE	Active low output enable. Low on all expansion bus reads.
/WE	Active low write enable. Low on all expansion bus writes.
/BE0-1	Active low byte enables. /BE0 is low on reads and writes on DATA0-7. /BE1 is low on reads and writes on DATA8-15. It may be necessary to use these signals to gate /WE to external devices.
/EWAIT	Active low wait signal. This signal can be pulled low by external logic to extend bus cycles for slow peripherals. It would normally be driven by an open-drain driver. The AA1100 has a 100k pull-up resistor on this signal; a lower value resistor should be added on the external circuit.
/RESET	Active low reset signal. This is an open-drain signal.
/SLEEP	Not strictly part of the expansion bus, but this could be of use to some users. It is the Au1100's PWR_EN signal, which is low during reset and while the Au1100 is in suspend state. It can be used to power down circuitry during the suspend state. This signal is not available on the Rev B00 version of the Au1100.
GPIOx	Some GPIO pins can be used as interrupt request signals. They can be programmed as active low or active high, and level or edge sensitive. Contact DSP Design for details.

TABLE 18 – DESCRIPTION OF EXPANSION BUS SIGNALS

The AA1100 has four programmable chip selects, two of which (/CE1 and /CE2) can be used for users' peripherals on the expansion bus. (Note that these are used for the AAMCA GPIO and LEDs). Initialisation code running on the AA1100 configures address decoding and bus timing registers to allocate address ranges and cycle times for these devices.

The AA1100 has a 32-bit data bus (DATA0-31), but only 16 bits (DATA0-15) are brought out to the expansion connectors. This means that memory accesses to addresses corresponding to D16-31 will not access peripheral chips. This has the consequence that a 16-bit peripheral will appear on addresses ending in 0 and 1, and

not on addresses ending in 2 and 3. Similarly, an 8-bit peripheral will appear on addresses ending in 0, and not on addresses ending in 1, 2 and 3.

GPIO pins that are not used for other purposes can be used as interrupt inputs. Interrupts can be edge or level sensitive and of either polarity.

Note that this Technical Reference Manual does not give users sufficient information to allow the design of boards that interface with the expansion bus. In addition, some software adjustments may be required to adjust address ranges, bus speeds and interrupt configuration. This may be available on a consultancy basis. Contact DSP Design for help and advice for your expansion bus projects.

3.3 EXTERNAL COMPACT FLASH/PCMCIA

The Aurora AA1100 has one Compact Flash socket, and can support an external Compact Flash or PCMCIA socket with the addition of external circuitry. This allows for further expansion using memory and peripheral cards. The external Compact Flash circuit is implemented on the AAMCA, which adds a second Compact Flash socket.

Compact Flash cards and PCMCIA cards are identical from a software perspective. Apart from the different connectors, there are only minor differences from a hardware perspective.

The Compact Flash and PCMCIA interface shares the expansion bus data and address signals and has dedicated control signals. Most of the signals are routed to both sockets, but some are dedicated to one socket only. Address line A26 determines which socket sees Compact Flash memory accesses - when A26 is low accesses are to the AA1100 socket. The Compact Flash signals for an external socket are shown in Table 19.

SIGNALS	DESCRIPTION
DATA0-15	Data bus.
ADDR0-25	Address bus (Compact Flash cards use only A0-A10).
ADDR26	When 0 selects AA1100 socket and when 1 selects external socket.
/PREG	Attribute memory select.
/PIOR	Strobe for I/O read cycle.
/PIOW	Strobe for I/O write cycle.
/PCE0	Card enable 1.
/PCE1	Card enable 2.
/PIOCS16	16-bit port select.
/PWE	Strobe for memory write cycle.
/POE	Strobe for memory read cycle.
/PWAIT	Extends access cycle.
/EXTENABLE	Enables external socket.
/EXTDETECT	External card detect.
/EXTRDYBSY	External ready/busy or interrupt request.
EXTRESET	External socket reset.

TABLE 19 – COMPACT FLASH SIGNAL DESCRIPTIONS

4 SOFTWARE

At the time of writing the AA1100 supports Windows CE and Linux operating systems. Users are referred to the LaunchPad Developer's Guides which contain extensive information about the implementation of these operating systems.

The next three sections provide a brief summary of the software provided.

Software resides in the on-board Flash memory chip, and optionally in a Compact Flash memory card.

Software is being refined continually, so check with DSP Design for the latest details of software.

4.1 YAMON

Following a hardware reset, the AA1100 boots YAMON from on-board Flash memory. YAMON is a monitor program which performs a similar function to a BIOS in x86 architectures. YAMON provides the following functions:

- Processor and peripheral initialisation.
- RAM size/type detection and auto configuration.
- Shell with command line history and editing through serial port COM3
- Traditional shell commands (display and change memory locations, load, go, dump, erase flash memory etc)
- Ethernet support for downloading of files using TFTP, and ping.
- Ability to launch a program from the command line or automatically using the "start" environment variable.

Communication with Yamon is by way of the COM3 serial port. Communication is at 115.2k baud with 8 data bits, one stop bit and no parity. COM3 will only be used for Yamon and Eboot if GPIO pins GPIO6 and GPIO17 (connected to AACONN SW1 and SW2) are set in certain ways. Section E.4 discusses this.

YAMON pauses for two seconds prior to executing the start environment variable. In the case of typical Windows CE systems, this starts the Eboot boot loader. In the case of typical Linux systems this starts the Linux loader. To halt at the YAMON prompt, type CTRL-C.

4.2 EBOOT

Eboot is only used in Windows CE systems. It is the Windows CE .NET boot loader, and it also resides in the on-board Flash memory.

After initialising the hardware, YAMON will normally run Eboot. Eboot will copy the Windows CE .NET image from either Compact Flash card or on-board Flash into SDRAM before executing the code from SDRAM.

Eboot provides the following functions:

- Ability to copy an NK.BIN file from the Compact Flash card to on-board Flash memory with the **image** command.
- Ability to clear Windows persistant registry with the **perreg –erase** command.

Communication with Eboot is by way of the COM3 serial port. Communication is at 115.2k baud with 8 data bits, one stop bit and no parity. COM3 will only be used for Yamon and Eboot if GPIO pins GPIO6 and GPIO17 (connected to AACONN SW1 and SW2) are set in certain ways. Section E.4 discusses this.

Eboot is normally started by YAMON. See section 4.1 for details of this.

4.3 OPERATING SYSTEMS

DSP Design supports Windows CE and Linux, through the LaunchPad Application Development Kits for the Aurora AA1100.

DSP Design strongly recommend using the LaunchPad Application Development Kits, which are complete ready to use embedded computer systems, that are waiting for your application to be placed into the solid state disk.

Using the LaunchPad will greatly reduce your development time, so your product will get to market sooner at a fraction of the engineering costs normally associated with embedded product development.

We have two objectives as you begin to use your new LaunchPad Application Development Kit.

Firstly, we expect that within an hour of receiving your LaunchPad you will have set up the hardware, connected it to your LAN and run the demonstration data acquisition application from a web browser.

Secondly, we expect that within a day you will have installed the development tools, compiled a sample application, downloaded it to the target hardware, and experimented with debugging this application remotely from the host computer.

So on the second day you can begin developing your real application.

For full details of the LaunchPad Application Development kits see our web site at www.dspdesign.com/launchpad.

5 POWER MANAGEMENT

5.1 OVERVIEW

The Au1100 processor chip contains a robust power management scheme allowing multiple levels of power conservation. In addition, the AA1100 circuitry has been designed to minimize power consumption, particularly in suspend mode. This results in a board that is well suited for battery-powered applications.

In the Au1100 processor, power management can be broken into two different areas:

- CPU - The Au1100 processor can be put into two Idle states and a suspend or sleep state. The peripherals can be individually disabled.

- Peripherals - each peripheral can have its clocks disabled when not in use thus significantly reducing the power drawn by those blocks not in use.

5.2 IDLE

The Au1100 can be put into low power idle modes by using the wait instruction. In this state the CPU clock stops but the rest of the device remains operational.

At all times the Memory Management Unit (MMU), data cache, execution and MAC blocks are placed in a low power state if they are not being used.

The Au1100 wakes from the idle states upon receiving an interrupt.

5.3 SUSPEND

(Note: AMD refers to this state as Sleep, and Microsoft as Suspend. We have chosen to use the term Suspend).

The suspend state of the Au1100 puts the entire device into a low power state. Suspend is the lowest power state of the part and requires a complete system initialization on wakeup.

During suspend all clocks within the Au1100 are stopped, with the exception of the 32kHz oscillator, which maintains the TOY (time of year) counter. The VCORE power supply is turned off. Prior to entering the suspend state, software disables on-chip peripherals (as well as off-chip devices) and places the SDRAM into a low-power self-refresh state.

The Au1100 hardware is designed to exit suspend state on receipt of one or more of the following interrupts sources (if enabled by software prior to entering suspend state). Note that at the time of writing software does not support all of these modes. Contact DSP Design if you want to use suspend.

Wake from suspend sources:

- Keypad press.
- Touchscreen press.
- COM3 RI signal being asserted
- COM2 RxD data arriving.
- GPIO6 asserted low, or high (depends on software).
- Interrupt from a Compact Flash I/O card in the AA1100 socket.
- TOY timer matching a pre-programmed value.

The Rev B00 versions of the AA1100 do not support all of these wakeup events.

5.4 INTERNAL PERIPHERALS

Peripheral power management is handled through clock management and the disabling of unused peripherals.

5.5 EXTERNAL PERIPHERALS

Most external peripherals can be placed into a low-power state by software prior to entering the suspend state. Those peripherals that can be power managed include the Ethernet PHY chip, keypad encoder, touchscreen controller, analog to digital converter chip, audio codec, and Compact Flash socket. In addition, USB devices can be placed in a low power state by software commands.

The RS232 transceivers have an automatic power-down state that is transparent to users. The chips detect activity on the transmitter and receiver inputs, and valid RS232 signal levels on receiver inputs. When no activity or valid signals levels are detected the chips enter a low-power state after 20 seconds or so.

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APPENDIX A – MECHANICAL DRAWINGS

This appendix includes mechanical drawings of the Aurora AA1100 (Figures A1 and A2), showing the position of pin 1 of each connector. It also includes a pair of assembly drawings (Figures A3 and A4) showing the location of each component.

The assembly drawings are of the Rev B01 version of the board, which has some minor component changes from the Rev B00 version. The mechanical drawings are the same for both versions. The Rev B01 and B03 boards have identical component placements.

The AA1100 PCB is 1.0mm thick. The tallest component above the PCB is the Compact Flash socket, which is 6.6mm high, although when a ribbon cable assembly mates with the 44-way or 50-way connectors, the maximum height above the board is 10.7mm. The tallest components below the PCB are the inter-board connectors, which extend 3.8mm below the PCB. When the A1100 is mounted on another PCB using the inter-board connectors, the gap between the faces of the two PCBs is 4.0mm.

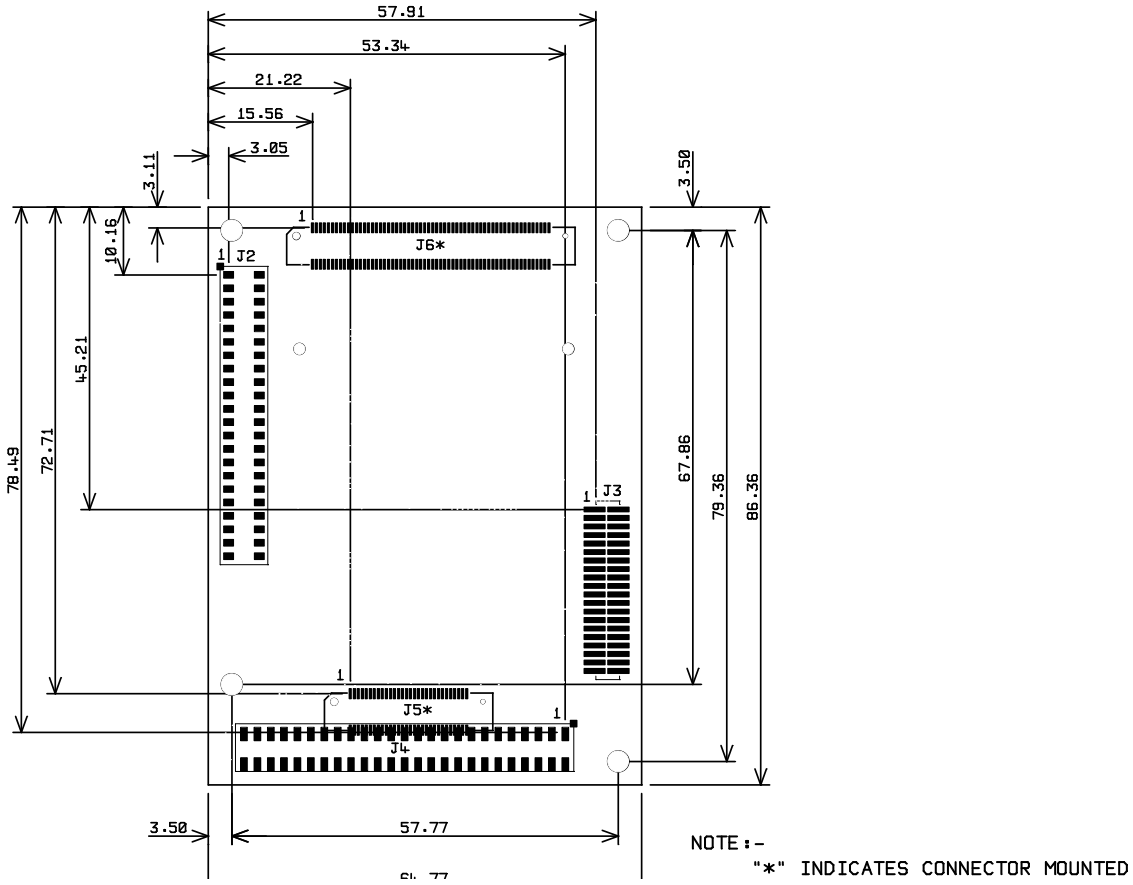
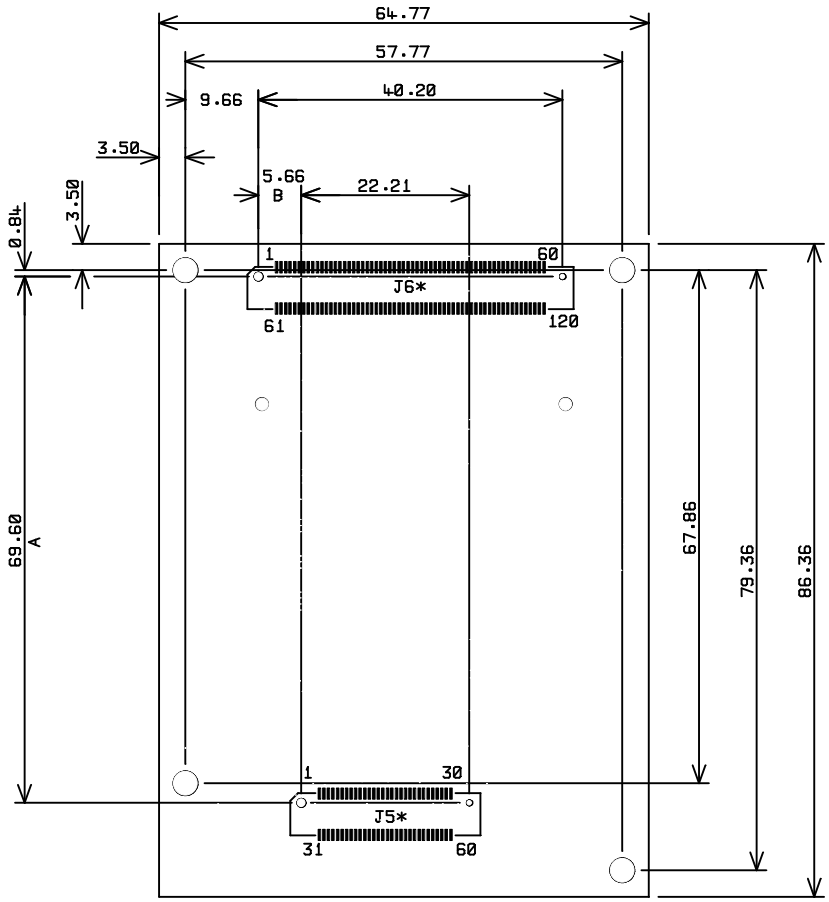


FIGURE A1 – AA1100 DIMENSIONS – TOP SIDE



Note: This shows the inter-board connectors as viewed from the top side.

FIGURE A2 – AA1100 DIMENSIONS – INTER-BOARD CONNECTORS

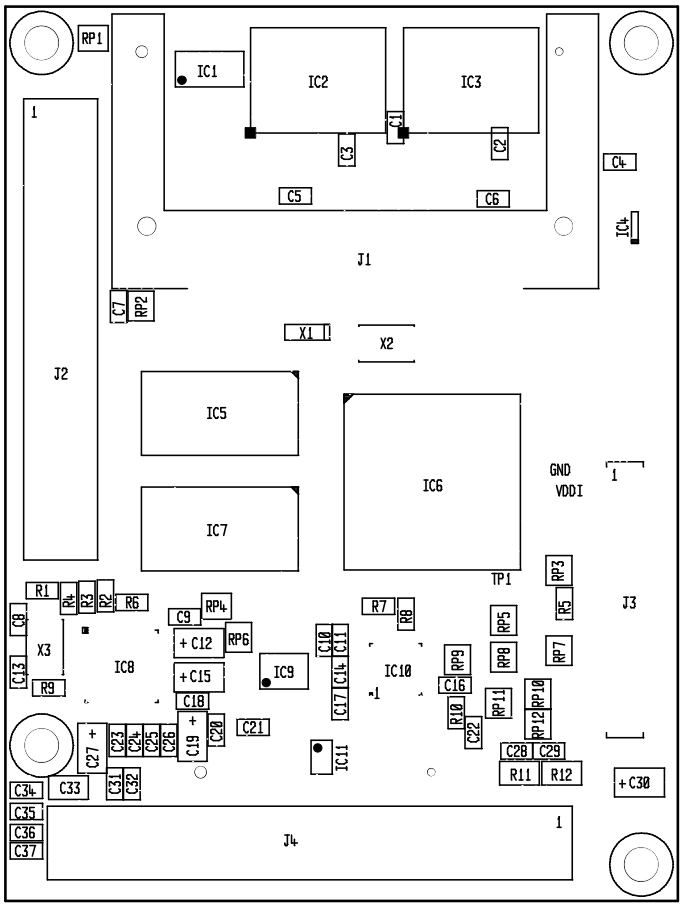


FIGURE A3 – AA1100 COMPONENT PLACEMENT – TOP SIDE

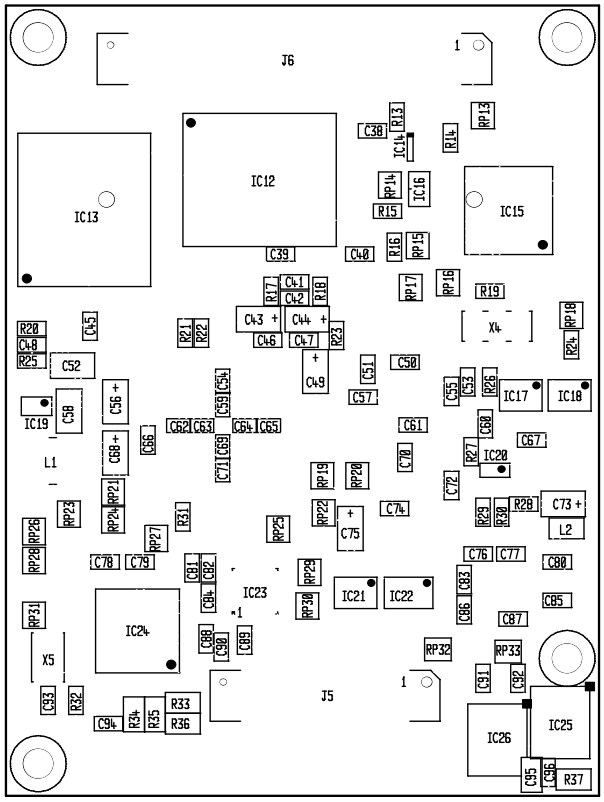


FIGURE A4 – AA1100 COMPONENT PLACEMENT – BOTTOM SIDE

APPENDIX B – OPTIONS AND ORDERING INFORMATION

This appendix lists the range of products available from DSP Design related to the Aurora AA1100.

B.1 PROCESSOR MODULES

ITEM	DESCRIPTION
AA1100	Aurora AA1100 processor module (no operating system)
AA1100NET	Aurora AA1100 processor module with Windows CE .NET version 4.2 Professional license
AA110E	Reduced specification Aurora processor board.

TABLE B1 – PROCESSOR MODULES

B.2 I/O MODULES

ITEM	DESCRIPTION
AACONN	Connector board for the Aurora AA1100
AAMCA	Memory card adaptor and digital I/O board for the Aurora AA1100

TABLE B2 – I/O MODULES

B.3 DISPLAY ACCESSORIES

ITEM	DESCRIPTION
AAVGA	CRT adaptor board for the Aurora AA1100
TFTIF-CAB7	40 way cable assembly for AATFT31, AATFT41 and AALQ038 boards, connectors at both ends, length 7 inches
TFTIF-CAB11	40 way cable assembly for AATFT31, AATFT41 and AALQ038 boards, connectors at both ends, length 11 inches
AALQ038	Interface board for the Sharp LQ0385DR01 3.8" QVGA TFT LCD panel
AATFTIF31	Interface board for Sharp LQ64D341, NEC NL6448BC26-01 or similar LCD panels
AANL064	Interface board for NEC NL6448BC20-08E 6.4" TFT LCD panel
AANLTS	Interface board for touchscreen on NEC 6.4" TFT LCD panel
AATFT038KIT	3.8" QVGA (landscape) TFT LCD kit with backlight inverter, touchscreen and cables to connect to AA1100 & AACONN.
AATFT064KIT	6.4" VGA TFT LCD kit with backlight inverter, touchscreen and cables to connect to AA1100 & AACONN.

TABLE B3 – DISPLAY ACCESSORIES

B.4 OTHER ACCESSORIES

ITEM	DESCRIPTION
AACONN-CAB	Aurora AA1100 to AACONN 50 way ribbon cable
TCONN-PSU	PSU for the AACONN

TABLE B4 – OTHER ACCESSORIES

B.5 LAUNCHPAD APPLICATION DEVELOPMENT KITS

ITEM	DESCRIPTION
LP1100NET	Windows CE .NET LaunchPad Application Development Kit
LP1100LIN	Linux LaunchPad Application Development Kit

TABLE B5 – LAUNCHPAD APPLICATION DEVELOPMENT KITS

APPENDIX C – CONNECTOR PIN ASSIGNMENTS

This Appendix describes the connectors used on the Aurora AA1100.

Note that when handling the AA1100, and when adding or removing connectors in particular, due anti-static precautions should be taken. Note also that the two SDRAM chips are chip-scale packages and are subject to damage if pressure is applied to them.

C.1 SUMMARY OF CONNECTORS

Tables C1 and C2 summarise the connectors used on the Aurora AA1100.

NAME	FUNCTION	NO. OF PINS	CONNECTOR TYPE
J1	Compact Flash	50 (2 x 25)	Compact Flash Socket
J2	I/O	44 (2 x 22)	Straight pin header, 2mm
J3	LCD/Touchscreen	40 (2 x 20)	Straight pin header, 0.05”
J4	I/O	50 (2 x 25)	Straight pin header, 2mm
J5	Expansion	60 (2 x 30)	Hirose FX8-60P-SV(21) (mates with FX8-60S-SV(21)
J6	Expansion	120 (2 x 60)	Hirose FX8-120P-SV1(21) (mates with FX8-120S-SV(21)

TABLE C1 – SUMMARY OF CONNECTORS

NAME	FUNCTION
J1	Compact Flash Socket
J2	Keypad matrix, COM1, COM2, JTAG test port, reset
J3	LCD and touchscreen
J4	USB, Ethernet, COM3, IrDA, audio, analog inputs, reset
J5	USB, Ethernet, COM1, COM2, COM3, IrDA, audio, analog inputs
J6	Keypad matrix, expansion bus

TABLE C2 – CONNECTOR FUNCTIONS

C.2 I/O CONNECTORS

There are two 2mm pitch pin headers carrying most of the signals to I/O devices. You can use 2mm IDC connectors and ribbon cable to make connection to these connectors. A 0.05" pitch pin header carries the display and touchscreen signals. The AAVGA plugs onto this connector directly, or you can use ribbon cable to make connection between this connector and an LCD.

Great care must be taken when fitting and removing the 44-way connector J2 as it is close to the two SDRAM chips. Pressure on the SDRAM chips can crack the silicon.

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	ROW0	Keypad row input	2	ROW1	Keypad row input
3	ROW2	Keypad row input	4	ROW3	Keypad row input
5	ROW4	Keypad row input	6	ROW5	Keypad row input
7	ROW6	Keypad row input	8	ROW7	Keypad row input
9	COL0	Keypad column output	10	COL1	Keypad column output
11	COL2	Keypad column output	12	COL3	Keypad column output
13	COL4	Keypad column output	14	COL5	Keypad column output
15	COL6	Keypad column output	16	COL7	Keypad column output
17	COL8	Keypad column output	18	COL9	Keypad column output
19	COL10	Keypad column output	20	COL11	Keypad column output
21	COL12	Keypad column output	22	COL13	Keypad column output
23	XSW	Keypad switch input	24	SW0	Keypad switch input
25	/RESET	System reset in/out	26	/WE	Memory write strobe
27	/TRST	JTAG signal	28	TDI	JTAG signal
29	TDO	JTAG signal	30	TMS	JTAG signal
31	TCK	JTAG signal	32	GND	Ground
33	3V3	Power	34	RXD1	COM1 receive data
35	RXD2	COM2 receive data	36	TXD1	COM1 transmit data
37	TXD2	COM2 transmit data	38	GND	Ground
39	GND	Ground	40	LED	Keypad LED output
41	SCL	I2C bus clock *	42	N/C	Reserved. Do not connect. *
43	SDA	I2C bus data *	44	N/C	

* Note: Pins 41 and 43 are N/C on Rev B00 boards. Pins 42 and 44 were connected to other keypad signals on Rev B00 boards. SW0 was not connected to the keypad chip until the Rev B03 board.

TABLE C3 – J2 PIN ASSIGNMENTS

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	LCD_BLEN	Backlight enable	2	LCD_VCCEN	LCD power enable
3	GND	Ground	4	LCD_PCLK	Pixel clock
5	GND	Ground	6	LCD_LCLK	Line clock (HSYNC)
7	GND	Ground	8	LCD_FCLK	Frame clock (VSYNC)
9	TSXP	Touchscreen	10	TSXN	Touchscreen
11	GND	Ground	12	LCD_D0	Display data bit 0
13	GND	Ground	14	LCD_D1	Display data bit 1
15	LCD_D2	Display data bit 2	16	LCD_D3	Display data bit 3
17	GND	Ground	18	LCD_D4	Display data bit 4
19	LCD_VEEEN	VEE power enable	20	ADC3	A/D converter input
21	GND	Ground	22	LCD_D5	Display data bit 5
23	LCD_D6	Display data bit 6	24	LCD_D7	Display data bit 7
25	3V3	Power	26	LCD_D8	Display data bit 8
27	LCD_D9	Display data bit 9	28	LCD_D10	Display data bit 10
29	3V3	Power	30	TSYN	Touchscreen
31	TSYP	Touchscreen	32	GND	Ground
33	LCD_PWM0	Pulse width mod. output	34	LCD_D11	Display data bit 11
35	LCD_D12	Display data bit 12	36	LCD_D13	Display data bit 13
37	LCD_PWM1	Pulse width mod. output	38	LCD_D14	Display data bit 14
39	LCD_D15	Display data bit 15	40	LCD_BIAS	Display timing signal

TABLE C4 – J3 PIN ASSIGNMENTS

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	USBH0P	USB port 0, positive	2	USBH0N	USB port 0, negative
3	USBH1N	USB port 1, negative	4	USBH1P	USB port 1, positive
5	GPIO17	GPIO (AACONN SW1)	6	GPIO6	GPIO (AACONN SW2)
7	GND	Ground	8	3V3	Power
9	N0_TXN	Ethernet transmit, negative	10	N0_TXP	Ethernet transmit, positive
11	N0_RXN	Ethernet receive, negative	12	N0_RXP	Ethernet receive, positive
13	/LINKLED	Ethernet LED	14	/LANLED	Ethernet LED
15	GND	Ground	16	RXD3	COM3 receive data
17	TXD3	COM3 transmit data	18	RTS3	COM3 RTS output
19	DTR3	COM3 DTR output	20	RI3	COM3 RI input
21	DSR3	COM3 DSR input	22	DCD3	COM3 DCD input
23	CTS3	COM3 CTS output	24	RS232	RS232/RS485 selection
25	GND	Ground	26	GND	Ground
27	IRTXD	IrDA transmit data	28	/RESET	System reset in/out
29	IRRXD	IrDA receive data	30	3V3	Power
31	Reserved	Pin removed for connector polarisation	32	3V3	Power
33	MIC1	Microphone input	34	MICGND	Analog ground (audio)
35	LINEINL	Audio line in left	36	MICBIAS	Voltage for electret microphones
37	AINGND	Analog ground (audio)	38	LINEINR	Audio line in right
39	LINEOUTR	Audio line out right, mono speaker out	40	LINEOUTL	Audio line out left, mono speaker out
41	HPOUTR	Headphone out right	42	HPOUTL	Headphone out left
43	AUDIOGPIO	Audio GPIO	44	OUT3	Extra audio output
45	ADC0	A/D converter input	46	AOUTGND	Analog ground (audio)
47	ADC2	A/D converter input	48	ADC1	A/D converter input
49	ADCGND	Analog ground (A/D)	50	ADC3	A/D converter input

TABLE C5 – J4 PIN ASSIGNMENTS

C.3 INTER-BOARD CONNECTORS

Two high-density board-to-board connectors are provided to carry signals from the AA1100 to other boards. This allows the AA1100 to be used as processor sub-systems that can be added as components to customers' own designs. These connectors carry most of the signals present on the two 2mm ribbon cable connectors, which means that these connectors are not required in such systems.

The connectors used on the AA1100 are the Hirose FX8-60P-SV1(21) (for J5) and the Hirose FX8-120P-SV1(21) (for J6). These mate with the FX8-60S-SV(21) FX8-120S-SV(21) respectively. This gives a 3mm inter-board gap. Other versions of the mating connectors are available for a 4mm inter-board gap.

Tables C6 and C7 provide the pin assignments for these connectors. (Table C7 is split into two parts).

Note that this Technical Reference Manual does not give users sufficient information to allow the design of boards that interface with the expansion bus. Contact DSP Design for help and advice for your expansion bus projects.

PIN	SIGNAL	PIN	SIGNAL
1	ADC3	31	ADCGND
2	ADC1	32	ADC2
3	AOUTGND	33	ADC0
4	OUT3	34	AUDIOGPIO
5	HPOUTL	35	HPOUTR
6	LINEOUTL	36	LINEOUTR
7	LINEINR	37	AINGND
8	MICBIAS	38	LINEINL
9	MICGND	39	MIC1
10	LED	40	3V3
11	GND	41	SDIN
12	TXD2	42	SDOUT
13	RXD2	43	SCK
14	TXD1	44	/EXT_SDEN
15	RXD1	45	N/C
16	GND	46	IRRXD
17	/RESET	47	IRTXD
18	RS232	48	GND
19	DCD3	49	CTS3
20	RI3	50	DSR3
21	RTS3	51	DTR3
22	RXD3	52	TXD3
23	/LANLED	53	3V3
24	/LINKLED	54	GPIO6
25	3V3	55	GPIO17
26	USBH1P	56	N0_TXP
27	USBH1N	57	N0_TXN
28	GND	58	GND
29	USBH0N	59	N0_RXP
30	USBH0P	60	N0_RXN

TABLE C6 – J5 PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
1	COL12	61	COL13
2	COL10	62	COL11
3	COL8	36	COL9
4	COL6	64	COL7
5	COL4	65	COL5
6	COL2	66	COL3
7	COL0	67	COL1
8	ROW6	68	ROW7
9	ROW4	69	ROW5
10	ROW2	70	ROW3
11	ROW0	71	ROW1
12	SW0	72	XSW
13	GND	73	/SLEEP
14	SCL	74	DISABLE
15	SDA	75	GND
16	ROMSIZE	76	GPIO200
17	GPIO18	77	SDDAT0
18	SDDAT1	78	SDDAT2
19	SDDAT3	79	SDCMD
20	SDCLK	80	/EXTRDYBSY
21	EXTRESET	81	/EXTENABLE
22	/EXTDETECT	82	GND
23	/LWAIT	83	/PCE0
24	LCLK	84	/PWAIT
25	GND	85	/POE
26	/PWE	86	/PIOCS16
27	/PIOW	87	3V3
28	/PCE1	88	/PIOR
29	/PREG	89	/EWAIT
30	/CE3	90	GND

TABLE C7a – J6 PIN ASSIGNMENTS (Part)

PIN	SIGNAL	PIN	SIGNAL
31	/CE1	91	/CE2
32	3V3	92	/CE0
33	ADDR1	96	/BE1
34	/BE0	94	/OE
35	ADDR3	95	ADDR0
36	ADDR4	96	/WE
37	GND	97	ADDR22
38	ADDR5	98	ADDR21
39	ADDR6	99	GND
40	ADDR7	100	ADDR10
41	ADDR8	101	ADDR11
42	GND	102	ADDR12
43	ADDR9	103	ADDR13
44	ADDR23	104	3V3
45	ADDR20	105	ADDR14
46	ADDR19	106	ADDR15
47	ADDR26	107	ADDR16
48	ADDR27	108	ADDR17
49	ADDR18	109	GND
50	DATA15	110	ADDR24
51	3V3	111	ADDR25
52	DATA7	112	ADDR2
53	DATA14	113	DATA13
54	DATA6	114	DATA5
55	DATA1	115	DATA12
56	GND	116	DATA4
57	DATA2	117	GND
58	DATA8	118	DATA11
59	DATA9	119	DATA3
60	DATA10	120	DATA0

* Note: On Rev B00 boards pins 73 and 76 were N/C

TABLE C7b – J6 PIN ASSIGNMENTS (Part)

APPENDIX D – GPIO PINS

The Au1100 processor has two groups of GPIO pins – GPIO0-31 and GPIO200-215. many of these pins have alternative functions (connecting to the Ethernet PHY chip, or as UART pins, for example. Most of the GPIO pins are assigned functions on the AA1100.

Tables D2 and D3 list the GPIO0-31 pins and GPIO200-215 pins respectively and their functions. Table D1 provides a guide in interpreting tables D2 and D3.

COLUMN	INTERPRETATION
BIT	GPIO bit
USE	AA1100 signal name
GPIO/ALT	Used as a GPIO or an alternative function
IN/OUT	Input or output. The direction of pins controlled by their alternative function is given in parentheses. GPIO pins to be used as open drain are either programmed as inputs or as outputs at logic 1.
DESCRIPTION	Notes on the use of the pins

TABLE D1 – INTERPRETING TABLES D2 AND D3

Note that GPIO0, GPIO1 and GPIO3 differ between Rev B00 boards on one hand and Rev B01 and B03 boards on the other. The Rev B00 function is listed first.

In the Rev B01 and B03 boards an inverter is introduced between /KEYPADIRQ and the Au1100 GPIO0 pin, and GPIO1 becomes the output of a NAND gate whose inputs are /PENDOWN, GPIO6, /AC97IRQ and /CFRDYBSY (CF interrupt).

In all versions of the boards the GPIO3 function is determined by fitting one of two resistors. On Rev B00 boards /AC97IRQ is selected and on the Rev B01 and B03 boards COM2IRQ is selected.

BIT	USE	GPIO/ALT	IN/OUT	DESCRIPTION
0	/KEYPADIRQ or KEYPADIRQ	GPIO	IN	Interrupt from keypad encoder. (See text.)
1	/PENDOWN or wakeup NAND gate	GPIO	IN	Interrupt from keypad encoder, or wake from suspend signal. (See text.)
2	COM3IRQ	GPIO	IN	Ring Indicator from COM3.
3	/AC97IRQ or COM2IRQ	GPIO	IN	Interrupt from /AC97 codec or RxD from COM2. (See text.)
4	/CFDETECT	GPIO	IN	AA1100 Compact Flash card detect signal.
5	/EXTDETECT	GPIO	IN	External Compact Flash card detect signal.
6	GPIO6 (SW2)	GPIO	IN	GPIO signal – connects to SW2 on AACONN.
7	/CFRDYBSY	GPIO	IN	AA1100 Compact Flash Ready/Busy or interrupt.
8	AUCFRESET	GPIO	OUT	AA1100 Compact Flash socket reset.
9	/CTS3	UART	(IN)	COM3 UART signals.
10	/DSR3	UART	(IN)	
11	/DCD3	UART	(IN)	
12	/RI3	UART	(IN)	
13	/RTS3	UART	(OUT)	
14	/DTR3	UART	(OUT)	
15	/EXTRDYBSY	GPIO	IN	External Compact Flash Ready/Busy or interrupt.
16	/CFENABLE	GPIO	OUT	Enable signal for AA1100 Compact Flash socket.
17	GPIO17 (SW1)	GPIO	IN	GPIO signal – connects to SW1 on AACONN.
18	GPIO18	GPIO	IN	Uncommitted GPIO signal.
19	SDA	GPIO	Open drain	I2C bus data.
20	/TSEN	GPIO	OUT	Taken low during an SSI access to the touchscreen controller.
21	EXTRESET	GPIO	OUT	External Compact Flash socket reset.
22	/KPEN	GPIO	OUT	Taken low during an SSI access to the keypad controller.
23	SCL	GPIO	Open drain	I2C bus clock.
24	PHYTXEN	PHY	(OUT)	MMI interface to Ethernet PHY chip.
25	PHYTXD0	PHY	(OUT)	
26	PHYTXD1	PHY	(OUT)	
27	PHYTXD2	PHY	(OUT)	
28	PHYTXD3	PHY	(OUT)	
29	/EXTENABLE	GPIO	OUT	Enable signal for External Compact Flash socket.
30	/KEYPADWU	GPIO	Open drain	Power control signal to keypad encoder.
31	/ADCEN	GPIO	OUT	Taken low during an SSI access to the A/D converter.

TABLE D2 – THE USE OF THE GPIO0-31 PINS

BIT	USE	GPIO/ALT	IN/OUT	DESCRIPTION
200	GPIO200	GPIO	IN	Uncommitted GPIO pin. Not available on Rev B00 boards.
201	LCD_VEEEN	GPIO	OUT	Enable signal for LCD VEE generator.
202	LCD_VCCEN	GPIO	OUT	Enable signal for LCD VCC power supply.
203	LCD_BLEN	GPIO	OUT	Enable signal for LCD backlight.
204	/PREG	PCMCIA	(OUT)	Compact Flash/PCMCIA control signals.
205	/PCE0	PCMCIA	(OUT)	
206	/PCE1	PCMCIA	(OUT)	
207	/PWE	PCMCIA	(OUT)	
208	SDOUT	SSI	(OUT)	SSI interface control signals.
209	SCK	SSI	(OUT)	
210	/SDEN	SSI	(OUT)	
211	IRTXD	IrDA	(OUT)	IrDA transmit data.
212	TXD1	UART	(OUT)	UART signals.
213	TXD2	UART	(OUT)	
214	TXD3	UART	(OUT)	
215	PHYMDC	PHY	(IN/OUT)	MMI interface to Ethernet PHY chip.

TABLE D3 - THE USE OF THE GPIO200-215 PINS

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APPENDIX E – AACONN

The Aurora AACONN is a connector breakout board for the Aurora AA1100. It connects to the Aurora AA1100 using a short length of ribbon cable and provides standard PC type connectors. Its features are listed in section 1.3.1.

This appendix lists AACONN configuration and connectors.

E.1 SOLDER LINK SETTINGS

A number of functions can be configured with solder links on the AACONN. The board layout is so dense we have implemented these configuration options with solder links that take up less space than jumpers, as well as being more reliable.

LK1 SW1 Enable

This link connects SW1 to GPIO17. By default the link is fitted.

LK2 SW2 Enable

This link connects SW2 to GPIO6. By default the link is fitted.

LK3 Mono Speaker Enable

This links connects one terminal of the mono speaker to LINEOUTR. The other terminal is permanently connected to LINEOUTL. By default the link is fitted.

LK4 Microphone Biasing

This link connects the AC97 codec MICBIAS signal to the 3.5mm microphone connector tip terminal, through a 680 ohm resistor. It thus supplies a DC voltage for electret type microphones which accept a bias voltage on the tip terminal. By default the link is not fitted.

LK5 Microphone Biasing

This link connects the AC97 codec MICBIAS signal to the 3.5mm microphone connector ring terminal, through a 680 ohm resistor. It thus supplies a DC voltage for electret type microphones which accept a bias voltage on the ring terminal. By default the link is fitted.

LK6, LK7 IrDA Optical Transmitter Power

These links select the IrDA optical transmitter power output. By default both links are omitted.

LK6	LK7	
Omitted	Omitted	1/3 Power (default setting)
Omitted	Fitted	Transmitter and Receiver Shutdown
Fitted	Omitted	2/3 Power
Fitted	Fitted	Full power

TABLE E1 – IRDA TRANSCEIVER CONFIGURATION

E.2 SUMMARY OF CONNECTORS

This section lists the connectors on the AACONN. Only the pin assignments for connectors J2 and J6 are listed in the next section. Connector J1 has the same pin assignments as the AA1100 connector J4, which ii connects to. The serial port, audio, Ethernet and USB connectors have standard pin assignments. The power input J7 is also standard, with the sleeve of the jack being GND.

NAME	FUNCTION	NO. OF PINS	CONNECTOR TYPE
J1	Connection to AA1100 J4	50 (2 x 25)	Straight pin header, 2mm
J2	ADC and audio. Used by LaunchPad Experiment Board.	20 (2 x 10)	Straight pin header, 0.1”
J3	Stereo line, speaker or headphone output	3 (tip, ring, sleeve)	3.5mm socket, lime green
J4	Microphone input	3 (tip, ring, sleeve)	3.5mm socket, pink
J5	COM3	9	D-type, male
J6	5V power supply, typically an output for LCD backlight inverters	4	Molex 53261-0490
J7	5V power input jack	-	5.5mm power jack
J8	Ethernet	-	RJ45 Pulse J0011D21B
J9	Not fitted		
J10	Dual USB	-	AMD787617-1

TABLE E2 – SUMMARY OF AACONN CONNECTORS

E.3 J2 CONNECTOR PIN ASSIGNMENTS

This section gives pin assignments for the J2 connector.

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	3V3	Power supply	2	ADC0	A/D input
3	ADCGND	A/D Ground	4	ADC1	A/D input
5	ADCGND	A/D Ground	6	ADC2	A/D input
7	ADCGND	A/D Ground	8	ADC3	A/D input
9	LINEINL	Audio Line In Left	10	LINEINR	Audio Line In Right
11	AINGND	Audio Ground	12	GND	Power supply
13	TXD3	COM3 TxD	14	3V3	Power supply
15	HPOUTL	Headphones Out Left	16	HPOUTR	Headphones Out Right
17	GND	Power supply	18	OUT3	Audio OUT3 signal
19	AUDIOGPIO	Audio GPIO pin	20	AOUTGND	Audio Ground

TABLE E3 – J2 PIN ASSIGNMENTS

PIN	NAME
1	VCC (5V)
2	GND
3	GND
4	VCC (5V)

TABLE E4 – J6 PIN ASSIGNMENTS

E.4 SWITCH FUNCTIONALITY

The AACONN board includes two switches which are attached to two Au1100 processor GPIO pins. During the bootstrap process these are used to determine what software is booted. After operating systems boot they can be used for other purposes.

The function of the switches differs somewhat between Windows CE and Linux, and may change with subsequent software releases. See the LaunchPad Developer's Guides and release notes for a description of the use of these switches by bootstrap code.

Table E5 lists the functions of the switches with Windows CE at the time of writing. The most common use will be to boot Windows CE from the on-chip flash memory. This occurs when both GPIO17 and GPIO6 are logic 1 – which is the default state if the AACONN is not fitted, due to the pull-up resistors on these GPIO pins.

GPIO6 (SW2)	GPIO17 (SW1)	SERIAL PORT MESSAGES	BOOT OPERATION
0 (SW2 set towards SW1)	0 (SW1 set towards SW2)	Yes	Stop at EBOOT command prompt
0 (SW2 set towards SW1)	1 (SW1 set away from SW2)	Yes	EBOOT downloads CE via Ethernet
1 (SW2 set away from SW1)	0 (SW1 set towards SW2)	No	Boot CE from Compact Flash
1 (SW2 set away from SW1)	1 (SW1 set away from SW2)	No	Boot CE from Flash

TABLE E5 – EFFECT OF SWITCH SETTINGS AT BOOT TIME

Users who want to use the switches themselves should contact DSP Design for guidance.

E.5 IrDA OPTICAL TRANSCEIVER

An IrDA optical transceiver module is provided on the AACONN. It is connected to the AA1100 IrDA transmit and receive signals. Solder links LK6 and LK7 determine the transmit power. These are documented in section E.1.

E.6 POWER SUPPLY

The AACONN features a jack plug for a 5V power supply, and a 5V to 3.3V switch mode power supply. This provides 3.3V for the AA1100, and for circuitry on the AACONN.

The 5V is also routed to the USB connectors (via a current limiting chip) and to connector J6 (which is designed for providing 5V to LCD backlight inverters). No other circuitry requires 5V.

We have found that the 5V to 3.3V power supply circuit does a good job of providing a regulated 3.3V from Lithium Ion batteries. It will continue to operate with a battery voltage down to 3.3V, at which point it switches to a linear mode and routes the battery voltage direct to the 3.3V rail.

E.7 RESET SWITCH

Switch SW3 connects the AA1100 /RESET pin to GND when pressed. This resets the AA1100.

APPENDIX F – AAMCA

The Aurora AAMCA is a daughter board which mounts onto the Aurora AA1100 via two high-density board-to-board connectors and communicates to the Aurora AA1100 via the 16-bit expansion bus. It was designed initially as a technology demonstrator, to assist with the product development, but it can also be used in production systems. Its features are listed in section 1.3.2.

This appendix lists AAMCA configuration and connectors.

F.1 SOLDER LINK SETTINGS

A number of functions can be configured with solder links on the AAMCA. We have implemented these configuration options with solder links that take up less space than jumpers, as well as being more reliable.

LK1 Secure Digital Socket Card Detect

This link connects the Secure Digital card detect signal to the digital input channel 0. By default the link is not fitted. (By default the Secure Digital card is not fitted).

LK2 LED Enable

This link enables the LEDs by connecting the cathodes to GND. Remove the link if you want to save the power used by the LEDs. By default the link is fitted.

F.2 SUMMARY OF CONNECTORS

This section lists the connectors on the AAMCA. Only the pin assignments for connector J4 are listed in the next section. Connectors J1 and J2 have the same pin assignments as the AA1100 connectors J5 and J6. The Secure Digital connector is not fitted. The Compact Flash connector has standard pin assignments.

NAME	FUNCTION	NO. OF PINS	CONNECTOR TYPE
J1	Expansion	120 (2 x 60)	Hirose FX8-120S-SV(21)
J2	Expansion	60 (2 x 30)	Hirose FX8-60S-SV1(21)
J3	Compact Flash	50	Compact Flash socket
J4	Digital I/O	44 (2 x 22)	Straight pin header, 2mm
J5	Secure Digital Card	11	(By default not fitted)

TABLE F1 – SUMMARY OF AAMCA CONNECTORS

F.3 J4 CONNECTOR PIN ASSIGNMENTS

J4 PIN	NAME	J4 PIN	NAME
1	GND	2	GND
3	OUT0	4	IN0
5	OUT1	6	IN1
7	OUT2	8	IN2
9	OUT3	10	IN3
11	OUT4	12	IN4
13	OUT5	14	IN5
15	OUT6	16	IN6
17	OUT7	18	IN7
19	3V3	20	3V3
21	N/C	22	N/C
23	N/C	24	N/C
25	N/C	26	N/C
27	N/C	28	N/C
29	N/C	30	N/C
31	N/C	32	N/C
33	N/C	34	N/C
35	N/C	36	N/C
37	N/C	38	N/C
39	N/C	40	N/C
41	N/C	42	N/C
43	N/C	44	N/C

TABLE F2 – J4 CONNECTOR PIN ASSIGNMENTS

F.4 COMPACT FLASH CONNECTOR

The AAMCA includes a second Compact Flash connector. It can be used by both memory and I/O Compact Flash cards.

The connector uses almost identical interface circuitry as the Compact Flash connector on the AA1100. Section 3.3 describes the AA1100's Compact Flash interface.

F.5 DIGITAL I/O AND LEDS

The AAMCA includes two 8-bit output latches and an 8-bit input buffer. These are attached to the expansion bus.

One of the output latches drives eight LEDs. Processor data bits DATA0-7 are latched by any writes that assert chip select /CE1. Writing a 1 lights the corresponding LED. All of the LEDs can be disabled by removing link LK2. The system reset signal /RESET turns off all the LEDs.

The other output latch drives eight general-purpose output signals which are available on connector J4. Processor data bits DATA0-7 are latched by any writes that assert

chip select /CE2. Writing a 1 sets the corresponding OUT signal. The system reset signal /RESET resets all bits to 0.

The 8-bit input buffer reads data from the eight general-purpose input signals IN0-7 which are available on connector J4. These pins each have 22k pull-up resistors. The IN0-7 signals are read onto processor data bus DATA0-7 by any read cycle that asserts /CE2.

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APPENDIX G – DIFFERENCES BETWEEN B00, B01 AND B03 VERSIONS

In the middle of 2004 DSP Design revised the AA1100 design, moving from PCB Revision B00 to Revision B01. A revision B03 was also created. This appendix describes the differences between the three versions of the AA1100.

The three versions can be identified by the number that appears in several places on the boards – the Revision B00 board has the number 280000.B00, the Revision B01 board has the number 280000.B01 and the Revision B03 board has the number 280000.B03. Revision B02 was not manufactured. With one minor exception the Rev B01 and Rev B03 boards are functionally identical, and both may be in production simultaneously.

There are no mechanical differences between the boards.

CHANGE	REASON AND EFFECT
Corrected PCB error.	This removes a wire link modification.
Add I2C signals SDA and SCL to J2 pins 41 and 43 (previously N/C) through series resistors.	This is a feature required by one customer which we can now offer to everyone. The resistors could be removed to allow the pins to remain N/C if required.
Two unused keypad signals removed from J2 pins 42 and 44.	These signals were not previously used. Pins 42 and 44 are now available for future use.
Changed resistors on serial port outputs from pull-down to pull-up.	On Rev B00 boards this gives rise to break conditions at reset and resume from suspend, and RS485 transmitter enabled at reset and resume from suspend. The change corrects this. It also allows the revision of the board to be determined by s/w (prior to enabling UARTs).
SSI decoding circuit changed.	On Rev B00 boards external SSI devices are difficult to use since /SDEN on J5 pin 44 is asserted for both on-board and off-board devices. On Rev B01 and B03 boards /EXT_SDEN on this pin is not asserted for on-board devices. No changes made to on-board SSI device decoding.
Connected Au1100 GPIO200 to J6 pin 76 (previously N/C)	This makes the GPIO200 pin accessible, either as a GPIO pin or as an external display interface.
Added inverter between /KEYPADIRQ and Au1100 GPIO0	Active low interrupt on /KEYPADIRQ was the wrong polarity to use as wake from suspend event. The inverter corrects the problem.
Added gates on four wakeup signal sources and fed the result to Au1100 GPIO1, in place of /PENDOWN interrupt.	Signal levels on /PENDOWN, GPIO6, /AC97IRQ and Compact Flash interrupt were the wrong polarity to use as wake from suspend events. The gates create a composite wake event on GPIO1. /PENDOWN is no longer available on GPIO1.

TABLE G1 – CHANGES FROM REV B00 TO REV B01 BOARDS (Part)

CHANGE	REASON AND EFFECT
Routed COM2IRQ to Au1100 GPIO3.	Build-time population options allow either COM2IRQ or /AC97IRQ to be routed to GPIO3. COM2IRQ is a more useful selection and is implemented on Rev B01 and B03 boards.
Connected unused analog input on the touchscreen controller to ADC0.	This allows a partial depopulation (removing the A/D converter) while retaining a single 12-bit A/D input.
Changed some passive components.	This will reduce power consumption, especially in suspend state.
Added inverter to drive keypad encoder WUKO from Au1100 PWR_EN signal.	WUKO is designed to be driven by the processor to signal “wakeup keys only”. The inverter drives WUKO when the Au1100 switches to suspend mode. Previously WUKO was not driven by the processor.
Au1100 PWR_EN signal is taken via a series resistor to an unused pin on J2 (pin 73), now called /SLEEP.	/SLEEP can now be used to power down external circuitry during suspend.
Added test points.	Facilitate testing. No functional change.

TABLE G1 – CHANGES FROM REV B00 TO REV B01 BOARDS (Part)

CHANGE	REASON AND EFFECT
Connected SW0 to keypad encoder.	A PCB error came to light: keypad signal SW0 on the keypad encoder chip was not connected to I/O connectors. This fixes this problem.
Added different test points.	Facilitate testing at different facility. No functional change.

TABLE G2 – CHANGES FROM REV B01 TO REV B03 BOARDS

APPENDIX H – FAULT REPORTING

DSP Design makes every effort to ship products and documentation that are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a “Product Fault Report” form. If you ever have cause to return a module for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to your supplier.

Prior to returning a faulty product, please check the following:

1. The module has been correctly configured for the intended application.

2. The power supplies are providing correct voltage levels.

3. Cabling to the module is sound and connected correctly.

4. Other cards and equipment in the system are known to be correctly configured and functioning.

PLEASE INCLUDE A WRITTEN DESCRIPTION OF THE FAULT.

PLEASE RETURN THE MODULE TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT

CUSTOMER INFORMATION	PRODUCT INFORMATION
COMPANY NAME:	PRODUCT/DOCUMENT:
INDIVIDUAL CONTACT:	SERIAL NO:
PHONE NO:	DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE MODULE USUALLY USED? (WHAT OTHER MODULES, WHAT SOFTWARE ETC.)?

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