

# Implications for LEDs of the shift to large-diameter sapphire wafers

**Faisal Nabulsi**, Rubicon's senior VP, operations, explains technology and market trends for sapphire wafers over the last few years, and how larger diameters and patterned sapphire substrates are impacting LED manufacturing.

**T**he market for sapphire LED wafers has undergone significant changes over the past two years, reflecting two significant trends: the transition to larger-diameter wafers and the transition to the purchase of patterned sapphire substrates (PSS).

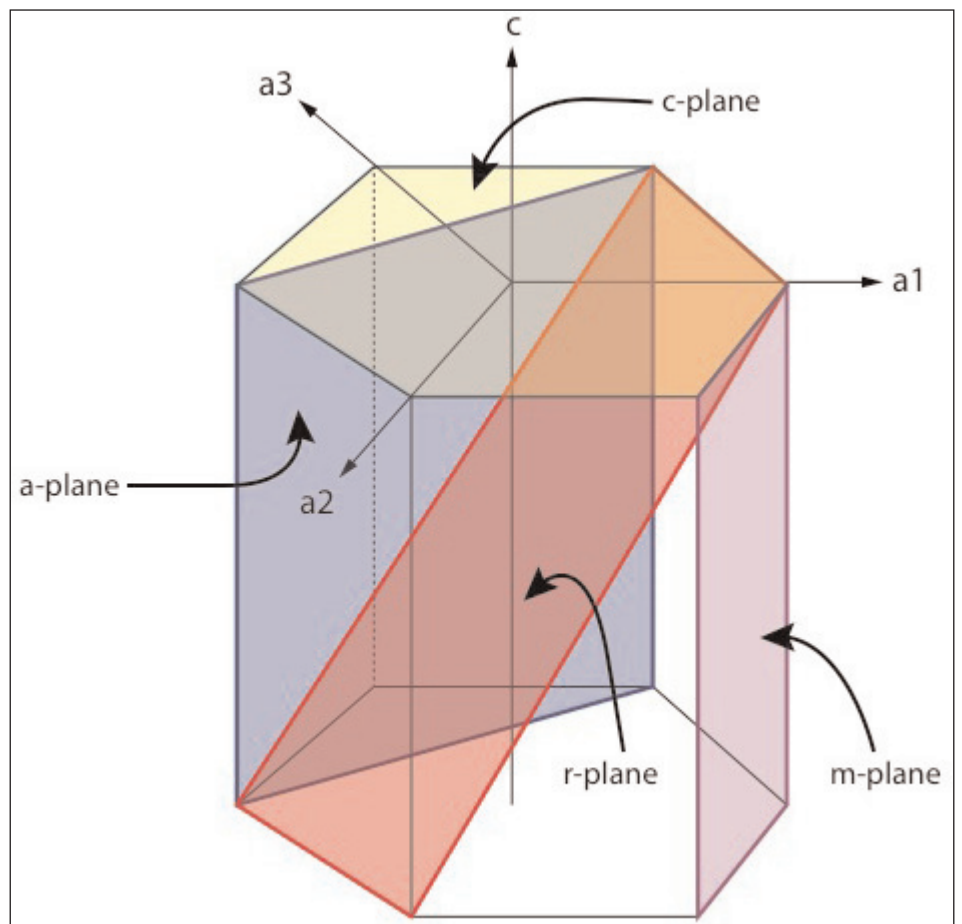
The heart of the LED sapphire market has moved up from 2" wafers to 4" wafers. Four-inch wafers now constitute the majority of LED sapphire wafer area, while two-inch sapphire has declined to less than 20% of the wafer area used in LEDs today. All regions including China are making the move to larger diameters.

Still in the minority — but clearly the fastest-growing part of the sapphire wafer market — is 6" sapphire. Market research firm Yole Developpement forecasted in August 2014 that the use of 6" wafers will double between 2014 and 2016, to about 25% of the LED sapphire market.

Alternative applications for sapphire, such as lens covers and smart watch faces, are absorbing much of the 2" core in the market, although not so much as to drive up the price of cores or wafers.

During the same time frame, the purchase of patterned sapphire substrates (PSS) has also climbed rapidly. Patterned wafers provide a significant increase in light extraction efficiency. The LED chip manufacturers first developed their proprietary patterns and the capacity for patterning internally, but more recently they have been willing to outsource.

PSS now accounts for the majority of sapphire sales in dollar terms although perhaps not yet in area terms. This shift reflects both the appearance of third-party patterning companies and the growing capabilities of



**Schematic diagram showing sapphire's various crystal planes.**

the sapphire producers themselves. Much of the sapphire sold as CSS (conventional sapphire substrates) is patterned by chip manufacturers themselves. Third-party patterning capability, which had originally focused on 2" wafers, is now moving also to larger diameters.

Sapphire has a hardness of 9 on the Mohs scale, and the challenges involved in fabricating this material to very precise orientation and flatness specifications are intensified at larger diameters. Here we present an overview of these challenges and the sapphire industry's current methods for addressing them.

## Sapphire crystal growth for large-diameter wafers

By now everyone knows that the two most effective methods of growing large-diameter sapphire crystal are Kyropoulos, a bulk growth method, and EFG (edge-defined film-fed growth), which produces sapphire in sheets. There are advantages and disadvantages to either method, but both have proven to be successful in the large-diameter wafer market.

During crystal growth, stress management of material is critical, especially for large-diameter products. The Kyropoulos growth method is very natural. The boule is grown in suspension with no contact with the crucible or any other element of the system. Growth is initiated by the vertically fixed seed on a pulling shaft at the top. As the seed makes contact with the melt at the right temperature, crystallization will occur naturally. Crystallization of the molten material across the solid-liquid phase line (seed to molten) emerges as a programmed heating profile takes place. With no pulling and zero rotation, the process results in a complete and practically stress-free crystal, suspended from the seed at the top. This process is as close as it gets to the growth of sapphire as produced by nature.

One of the best advantages of the Kyropoulos method is its low defect density across the grown material indiscriminately. This attribute makes it relatively manageable for scaling up, and the uniformity of the material quality across large-diameter wafers is excellent. In addition, the Kyropoulos growth cycle encompasses an effective annealing cycle which eliminates all built-up stresses due to the cooling process at the end of the cycle. Annealing is an integral part of the growth. The single hot-zone design, which completely surrounds the entire crucible, makes the annealing process very simple, efficient and uniform. On the other hand, the EFG hot-zone design may become rather complex if annealing is required. A second heater with a separate controlling circuit must be added to achieve a low-stress sheet of sapphire.

The geometric symmetry of C-plane versus R-plane makes the Kyropoulos-grown material more practical from the point of view of fabrication. The material is grown in the A-direction in a roughly cylindrical shape. The result is that the C-plane direction is only 57° apart from the R-plane along the boule's perimeter. This feature makes all grown material potentially good inventory for both C-plane of any size (2" through 8") and R-plane simultaneously. Inventory in boule form can therefore play a key role in responding to market needs in a timely fashion.

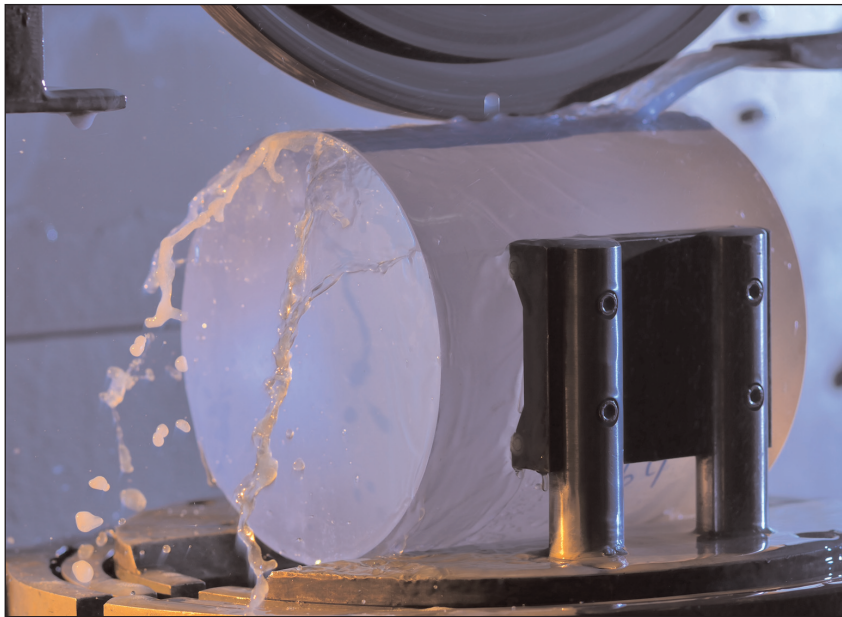


**Rubicon's 2", 4", 6", 8" and 12"-diameter sapphire wafers.**

## Fabrication of large-diameter cores and wafers

Drilling large-diameter cores from the bulky large Kyropoulos boules at an accurate orientation target with sub-degree tolerance has been a challenging task to master. All major LED chip manufacturers mandate a very tight orientation tolerance (as low as one tenth of one degree). The challenge has been in the handling of the massive and irregularly shaped boule to such a degree of accuracy in the x-ray alignment tool. The boule is fixed on a reference plate using two mixed bonding agents. No movements are allowed during curing of the bonding agents. The coring process, which involves a relatively harsh wet environment inside the CNC machines, must be designed to introduce no spatial or rotational movement to such a big crystal. The material must be firmly secured in the drilling machine to a great degree of stability for many hours while the drilling takes place and with the presence of high-pressure coolant.

The use of the diamond wire has been a definite advantage in slicing large-diameter sapphire. However, the main challenge in slicing 6" ingots is twofold. The first part is anchoring the ingot in the wire saw at one tenth of one degree accuracy to guarantee the orientation spec. Holding such accuracy through the duration of slicing (which may exceed 20 hours) has been a major mechanical undertaking. However, the availability of well-designed wire saws that can handle large ingots (which may be, for example, 10-inches in length) has made it possible to achieve good results in a reasonable timeframe. The second part is the constant challenge of holding the slicing process parameters stable within a tight, sweet window to produce flat wafers. The flatter the wafers out of slicing, the easier it is to move the products through the subsequent operations with minimal process time and cost. Bow and warp values of large-diameter wafers such as 6" are drasti-



**Core fabrication — finishing the outer diameter of the core to ensure conformance with both orientation specs and dimensional requirements.**

cally influenced by the smallest variation in the size and/or the concentration of the diamonds on the wire. Unlike Kyropoulos, EFG technology has no need for slicing. Avoiding slicing cost can be an advantage in total cost of ownership.

The next process is to flatten the large-diameter wafers further. Lapping wafers by using loose abrasive has largely been the practice in the industry. However, material grown by the EFG method requires a considerable amount of lapping to shape the parts flat, and that is largely due to the fact that EFG requires no slicing. The shape of the sheets as taken out of the EFG growth furnace is usually out of orientation and far from flat. The larger the diameter, the more difficult it is to bring the wafers into spec, especially from the flatness point of view.

The industry has suffered a great deal over this process in the past, for one simple reason: the material to be flattened, sapphire, is harder than the lapping equipment. The top and bottom metal plates on the conventional lappers are usually made of cast iron. Therefore, both plates will wear faster than the sapphire. In addition, the iron plates usually change shape during the lapping process to practically copy the shape of the incoming wafers. The plates will go out of shape even more quickly with high-warp, high-bow wafers. Conventional lapping equipment was designed and optimized for the silicon industry. This issue was manageable for sapphire in the past, when 2" wafers were the main product for the LED industry. When the 6" product became the driving force, this issue became quite formidable, especially for the EFG producers.

The EFG suppliers had to fix two problems in lapping. The first is to grind more material to flatten the wafers

efficiently, and the second is to bring the wafers into orientation. Therefore, these producers had to develop a new grinding process to replace lapping. The solution they introduced was a fixed abrasive system, and it provided multiple advantages. The platform is built on having diamond fixed on the grinding plates in the form of either diamond pellets or pads mounted on the top and bottom plates of the conventional lappers. This design provides a high removal rate and prevents the plates from going out of shape as the sapphire is processed.

Finally, polishing large-diameter sapphire wafers brought the chemical mechanical polishing (CMP) process into a new phase. The flatness of the 6" wafers has grown tighter year after year in an exponential fashion. The reduction of the exclusion zone, as required by the LED makers, added another dimension of complexity to the CMP process. The LED makers want to utilize every possible space on the 6" wafers. The longer the polishing cycle, the

faster the wafers go out of flatness, especially at the edges. The highest removal rate on the surface of the 6" wafers through the CMP process is at the perimeter. Deep scratches from previous operations can be a key factor in the cycle time of the CMP and hence compromise the flatness. An effective process between grinding and CMP needed to be introduced to minimize the subsurface damage and prepare the wafers for polishing. Fine diamond grit is used to remedy this issue.

### **Patterning for large-diameter sapphire wafers**

PSS technology was introduced as a solution to the constant need for more optical output. The initial GaN-on-silicon LEDs were introduced as indicator lights due to their low optical power. However, the outstanding electrical and thermal properties of the LED devices compared with all other light sources motivated the designers to aspire to much greater optical output. With sapphire substrates, high-power LED chips became a reality, but the aspiration did not stop at that point. As designers work harder to get more lumens per watt, they found a way to systematically guide the optical wave to where it is needed through the introduction of optical guiding pattern (PSS). Experiments to vary the shape, size, pitch and aspect ratio of etched patterns will continue to drive even more efficient LEDs.

There are two main contributors by which patterning affects the total optical power at the LED output facet. The first one is the geometric shape/design of the pattern. The second is the dimension tolerances of the pattern. The combinations of the shape (such as dome, pyramid or cone), in conjunction with the dimensions' tolerances, can make an astonishing difference in the coupling efficiency of the LED chips. LED

epitaxial growers continue to demand tighter tolerances of pattern dimensions. The consistency of the dimensions and their tolerances across the total area of the 6" wafers requires tight photo and etching processes. This in turn mandates precise stepper capabilities. The industry continues to drive the 6" substrate manufacturers and PSS equipment makers to achieve the best tolerances they can.

### Implications for sapphire market

The sapphire industry, like the LED industry, has been highly competitive and is characterized by under-absorbed capacity at both the crystal growth level and the wafer fabrication level. Current market trends may cause a bifurcation in sapphire supply, between highly capable large-diameter PSS providers and commodity sapphire core producers focused on components for con-

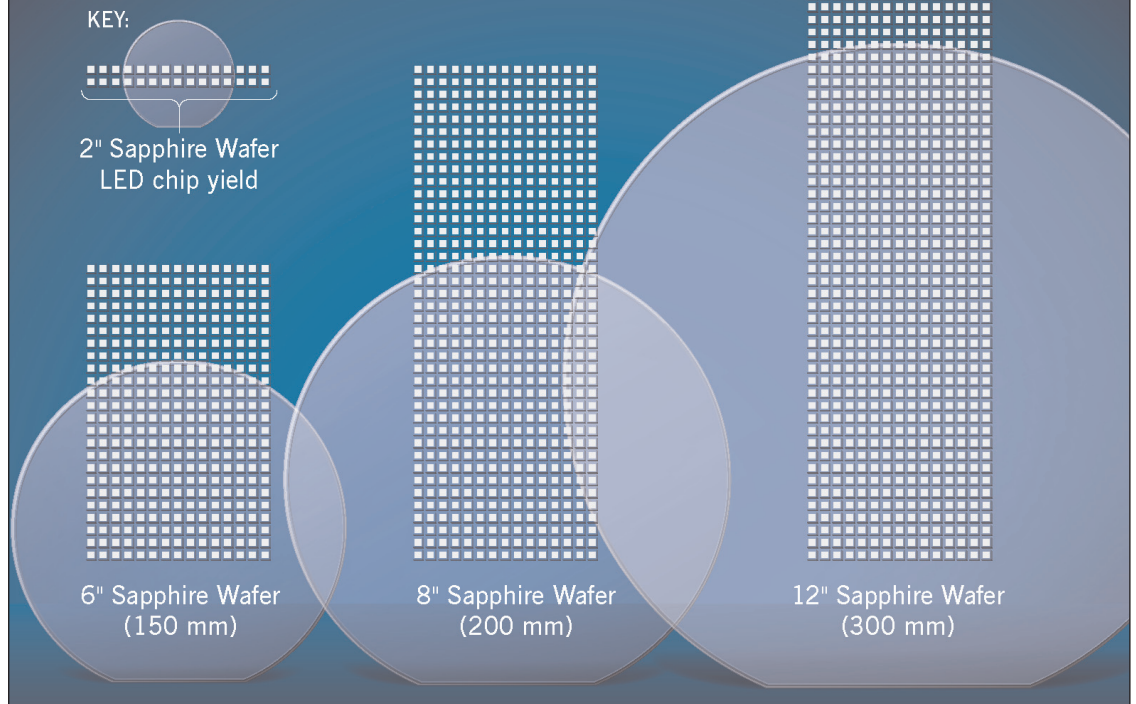
sumer electronics. LED-focused sapphire providers will need not just proficiency but excellence at every stage of crystal growth and wafer production in order to provide the extremely precise orientation and flatness required for 6-inch wafers. We may see some consolidation, as those sapphire producers targeting the LED market seek to internalize the most effective processes and capabilities they need to be successful large-diameter suppliers. For those focused on the consumer electronics market, a low cost structure for sapphire crystal growth and core fabrication is the principal strategic imperative.

### Implications for LED market

The move to larger substrates and PSS means that instead of buying 2" wafers as a commodity product, LED chip makers at the leading edge are now buying a highly engineered custom product from a limited num-

## Larger Wafer, Larger Yield

For years, two-inch and four-inch diameter sapphire wafers have been the standard for LED production. Now, LED manufacturers are migrating to six-inch diameter wafers to increase the number of LED chips made from each wafer processed. A six-inch wafer will produce approximately 10-12 times as many chips as compared to a two-inch wafer. Although the geometrical area increase is 9x, the decreased curvature of the larger sized wafer allows more LED chips to fit along the outer perimeter. This is called the "edge effect"—producing more chips than just the raw calculation of geometrical area.



ber of possible supply-chain partners. Other types of semiconductors grown on silicon wafers use 12- and even 18-inch wafers — an indication that this is the path to efficiency and productivity. Indeed, chip manufacturers are creating value for themselves with the move to larger wafers because they are handling fewer units. Each time the robot arm picks up a 6-inch wafer it moves more chip area by an order of magnitude compared with a 2-inch wafer.

With the increased size of sapphire wafers, LED chip companies need to be aware of the proficiency required in every operation for sapphire suppliers to maintain orientation tolerances and flatness specifications over the increased area of this very hard material. ■

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