EUVL for HVM: Progress and Risks

Mark Phillips

Intel Corporation

International Workshop on EUV and Soft X-Ray Sources, 4 November 2014, Dublin, Ireland

Are we there yet?

Photo by Google Images

Outline

- Review of EUVL outlook at 2013 Source Workshop
- Review of progress in last year
- Status update on EUVL insertion
  - Gaps in tool performance for TD and HVM
  - Challenge to Exposure Source community
  - Gaps in EUVL Infrastructure for TD and HVM
  - Challenge to Metrology Source community

As presented at 2013 Workshop

Problem Statement

- Long delays in the exposure source power roadmap have undercut the credibility of EUVL
- Investments in other EUVL infrastructure have been reduced or delayed due to this uncertainty
- We are now at risk that practical power levels will be available before the complete infrastructure required for use of EUVL in HVM is ready.

As presented at 2013 Workshop

Conclusions

- Realization of 40~80W stable MOPA+PP sources in the field linked to NXE:3300B scanners over next two quarters looks feasible

- This would enable meaningful integrated process development with 0.33 NA EUVL and re-establish confidence in a source power roadmap to HVM levels

- Need to re-invigorate EUVL infrastructure development, especially:
  - Exposure source power scaling beyond 250W with dramatically improved COO
  - Actinic metrology source development to meet performance, productivity, COO and schedule
  - Commercial EUV pellicle infrastructure

Progress in last year: First sources in field at ~40W

July 2014: 44W, 630 wafers in 24hrs at IBM

New Benchmark Established for EUV

21 Replies

I received this news from Dan Corliss of IBM today and it is reproduced below. Dan is the EUV Development Program Manager for IBM. As the previous goal for ASML scanner for 2014 was 500 wafers a day, this is definitely big news. Dan called it a "watershed moment" in his LinkedIn post. Of course, we need to see this type of performance to happen longer term like weekly basis, and it needs to be repeated by several leading edge chip makers but this is a sign of good things to come. Congratulations to Dan and his team, ASML and Cymer for significant achievement. We needed this and it lo
production!

IBM's NXE3300B scanner, at the EUV Center of Excellence
source upgrade. The upgrade resulted in better than projec
measured at intermediate focus and confirmed in resist at th
after the upgrade 637 wafer exposures were completed in

September 2014 confirmed at second customer

Press Releases

Successful EUV-productivity endurance test at second customer

VELDHOVEN, the Netherlands, 2 September 2014 - ASML Holding N.V. (ASML) today announces that a second customer has successfully performed an EUV-endurance test during which wafer processing capability was proven of around 600 wafers within 24 hours, on an NXE:3300B EUV system.

The endurance test was designed to simulate a production run and, similar to an earlier test in July at another customer, exceeded the 500 wafer per day requirement that ASML customers have set for the end of the year. ASML President and Chief Executive Officer Peter Wennink told a webcast investor conference in New York today that ASML is encouraged by the result of this second test. However, EUV-performance needs to be repeated on multiple days and multiple systems which is the goal of the availability improvement programs that will be executed throughout the remainder of the year.

"New Benchmark..." from http://electroiq.com/euvl-focus/2014/07/29/new-benchmark-established-for-euv

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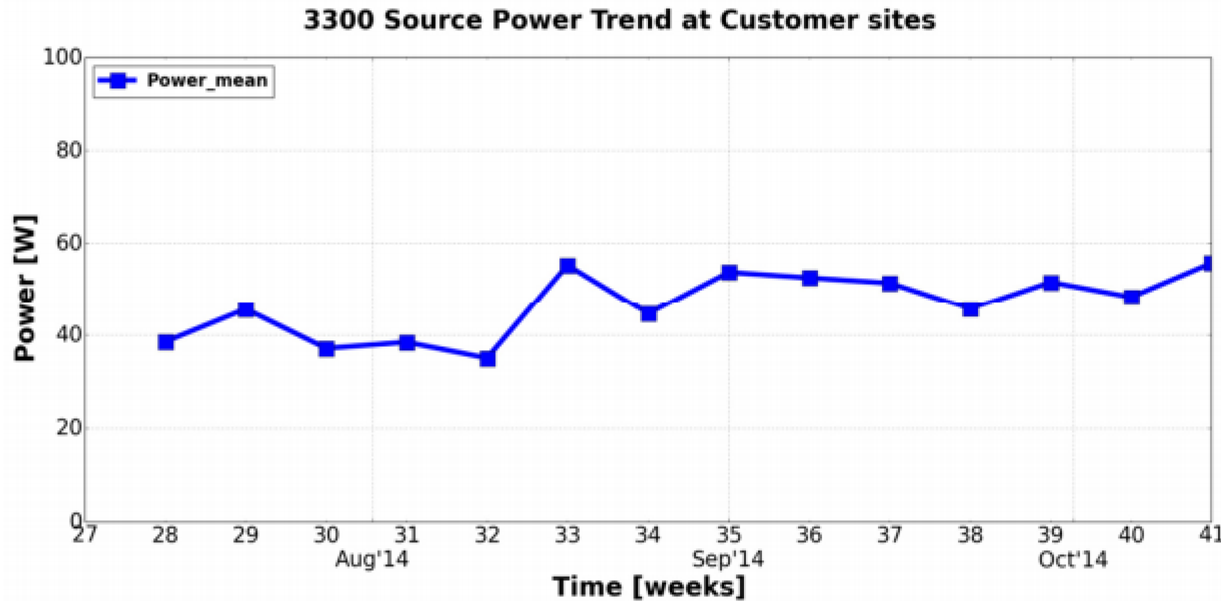
Progress: Sources operating stably in field at >40W (including Intel)



Four Customer Sources

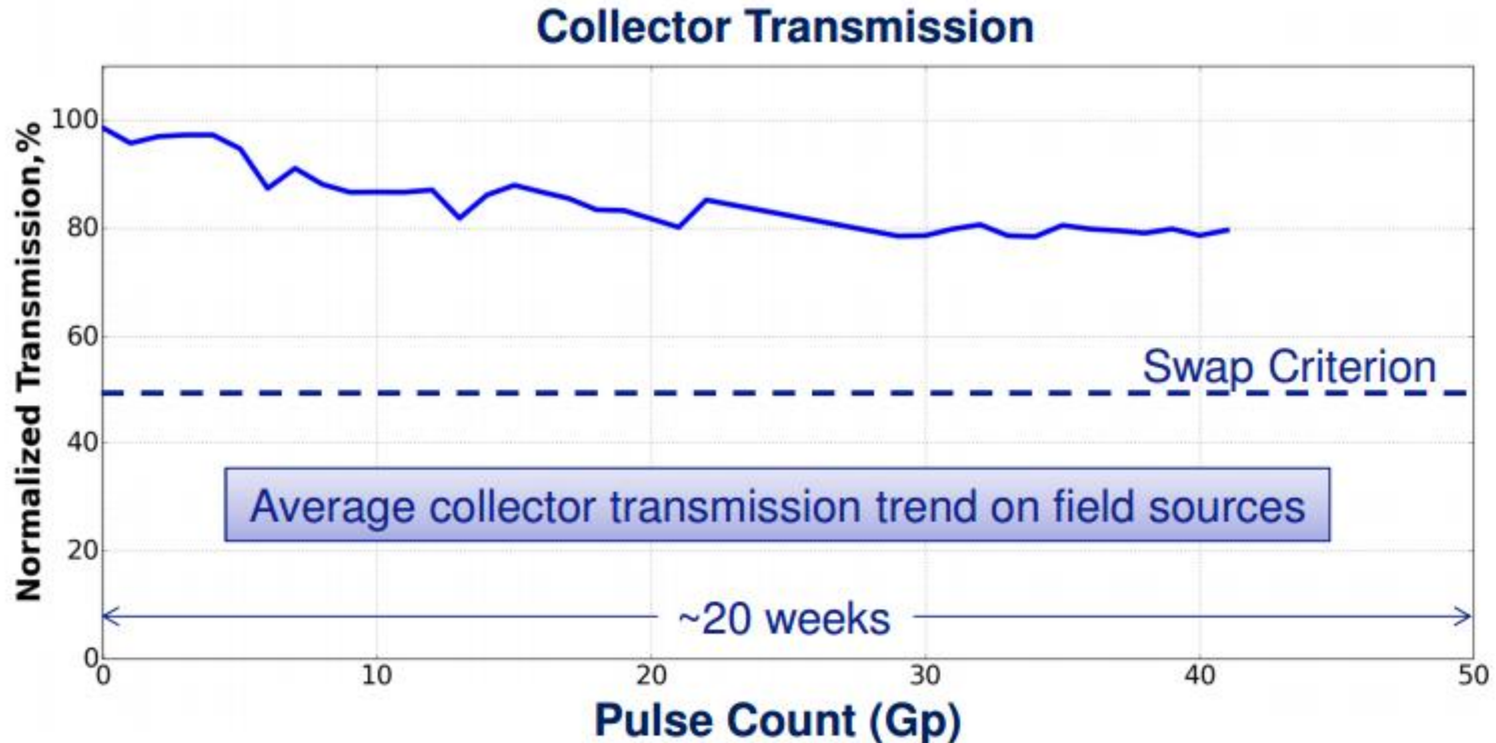
Weekly average power measured in the source

Normalized to clean collector conditions

CYMER An ASML company

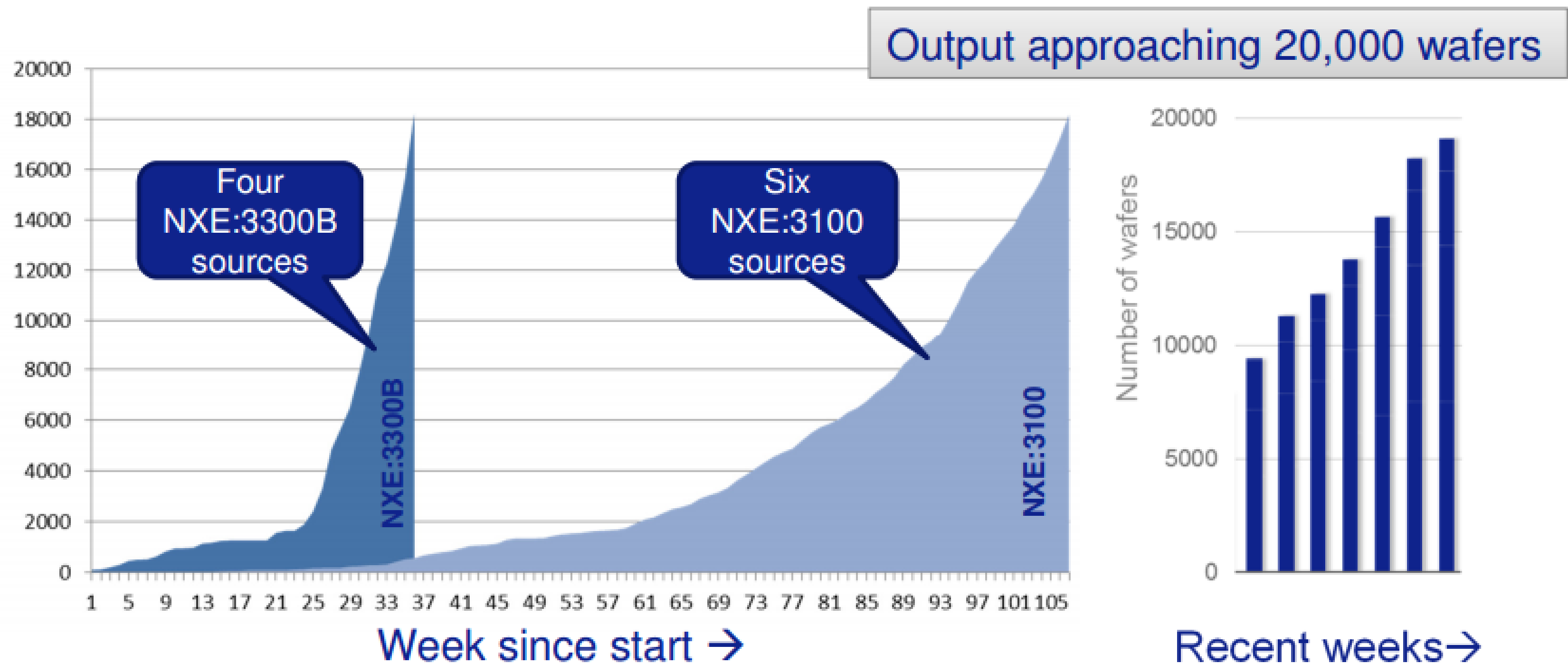
Slide courtesy ASML

Progress: Reasonable initial collector lifetime at >40W



Slide courtesy ASML

Progress: Dramatic improvement in productivity over NXE:3100



Slide courtesy ASML

CYMER An ASML company

Progress in last year: Worldwide summary

- 7 NXE:3300B systems shipped[1]
- 4 NXE:3300B systems in field with sources running >40W[1]
- >500 wafers in 24hrs demonstrated at two customer sites[1]
- One source operating at 80W in field[2] (~55 wph at 20mJ/cm^2 dose)
- Dramatic improvement in wafer processing capacity for process development with EUV

1) Per David Brandt (ASML) at 2014 EUVL Symposium
2) Per Anthony Yen (TSMC) at 2014 EUVL Symposium

Progress in last year: NXE:3300 performance in-house

- System (scanner+source) meets all specs except productivity.
- Productivity is consistent with source power.
- Power is stable and dose control is good.
- Scanner availability is solid.
- Source availability is still poor (average <40%), with Droplet Generator the biggest contributor

Conclusions

As presented at 2013 Workshop

Updated for 2014

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- This would enable meaningful integrated process development with 0.33 NA EUVL and re-establish confidence in a source power roadmap to HVM levels
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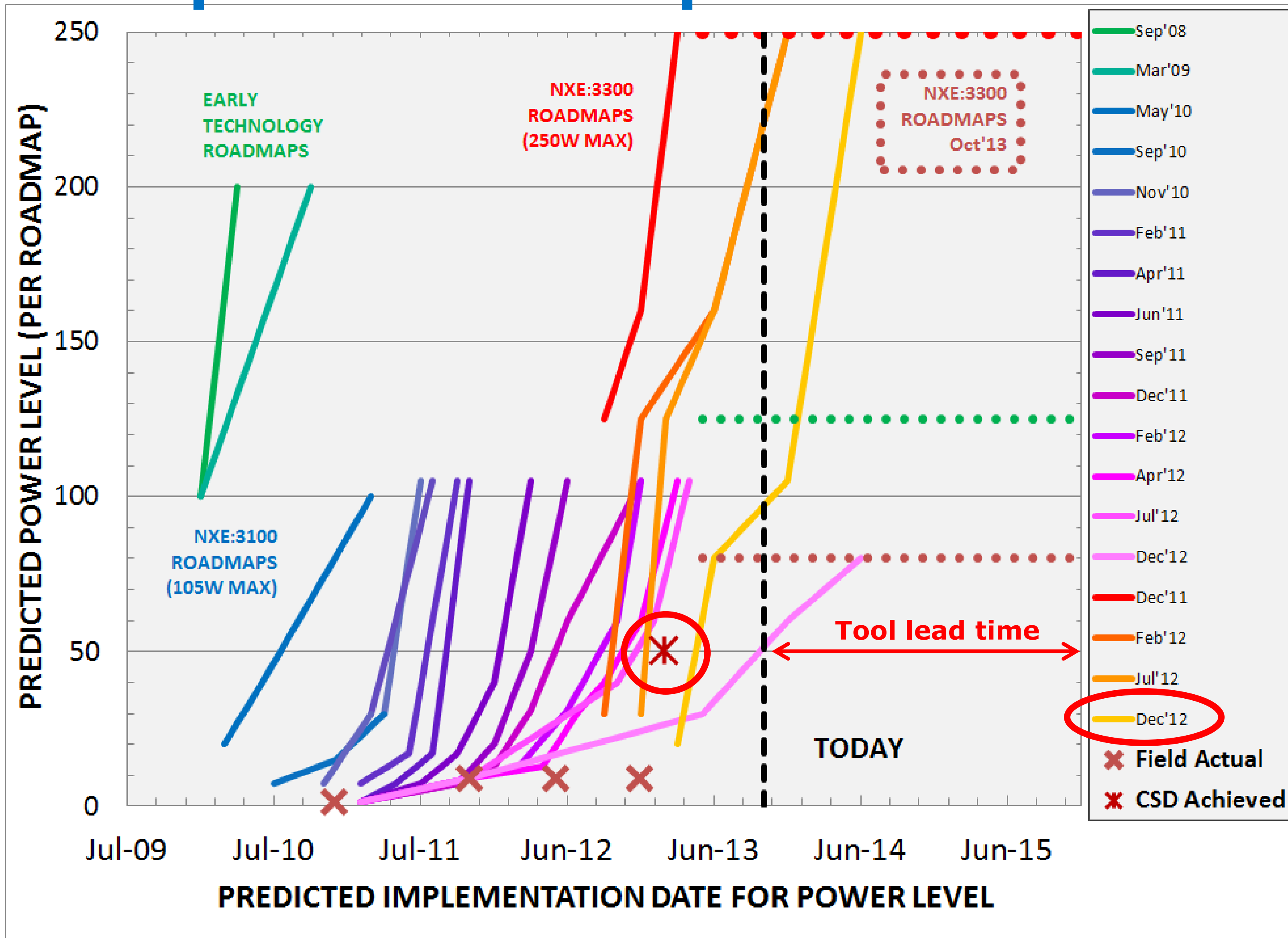
What about exposure tool performance gates committing a process node to EUV?

- Technology Development requires rapid information turns
  - Availability: tool must be up to run TD wafers without delay
- HVM requires reasonable COO and predictability, driven by:
  - Productivity (mostly source power)
  - Availability (mostly source availability)
  - OpEx (mostly source consumables)

As presented at 2013 Workshop

Source power roadmap has lost credibility



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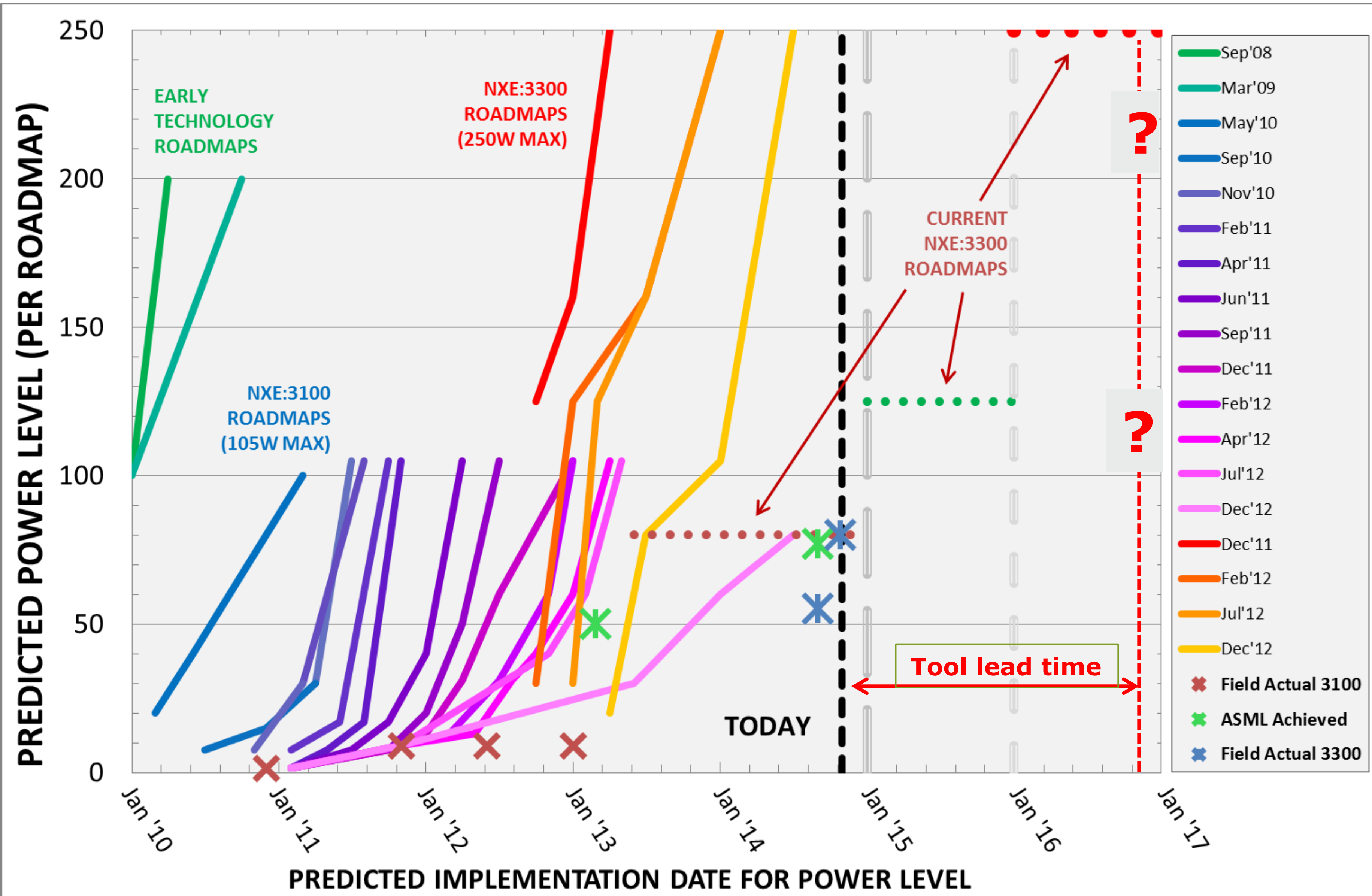
Source power roadmap is regaining credibility

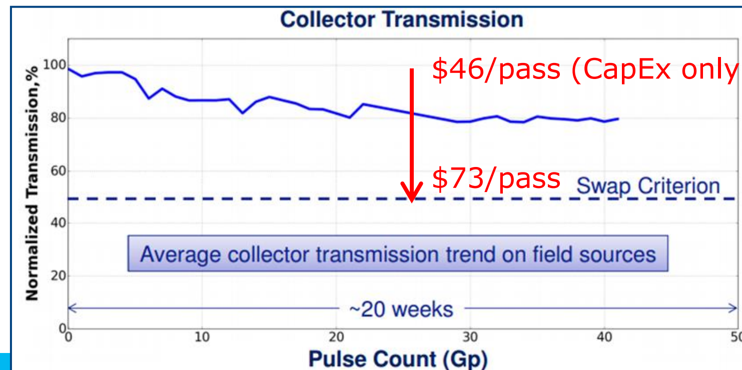


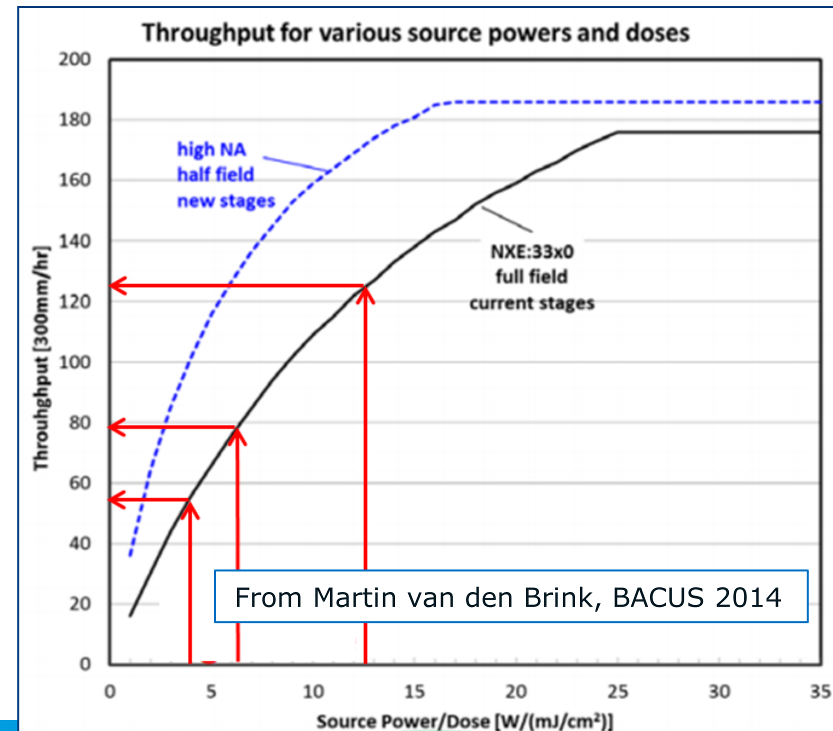
Tool CapEx contribution to wafer cost

tool cost	1.00E+08	$				
4yr depreciation	6.85E+04	$/day				
source power @ IF (W)	dose (mJ/cm^2)	power/dose	raw run rate (wph)	wafers/day @50% efficiency	$/wafer pass	$/wafer (13 layers†)
80	20	4	57	684	$100	$1,302
125	20	6.25	78	936	$73	$951
250	20	12.5	124	1488	$46	$598

† EUV layer estimate for hypothetical 14nm process, Mallik *et al. (IMEC) Proc. Of SPIE Vol. 8679 86782Y-1*

- Finished wafer cost depends strongly on final source power, availability, and OpEx
- All three still far from target
- Peak power drops significantly over life of expensive consumables





Blue = updated for 2014

EUV Source Milestones for HVM insertion and beyond

To keep HVM insertion on track:

- Stable availability >60% (sustained on fleet, not peak) in 1H15
- Proliferation of *in situ* collector cleaning in 1H15, for both COO and stable productivity
- Progress towards 80, 125 & 250W roughly per schedule

For long-term viability:

- Power scaling to ~1kW → ~500W maybe OK given 2X transmission of new optics design
- Dramatic improvements in COO

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No change from 2013

Exposure Source Challenge to Source Community

- HVM insertion of EUV must be with existing LPP & drive laser technology
- In order for EUV to scale for future generations, we need dramatic power and COO improvements
- Are there alternate technologies for drive lasers or the EUV source that are better suited in the long term (say, HVM in ~2019)?

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Updated for 2014

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- This would enable meaningful integrated process development with 0.33 NA EUVL and re-establish confidence in a source power roadmap to HVM levels Update: Good progress. Need to demonstrate better availability.
- Need to re-invigorate EUVL infrastructure development, especially:
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EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs

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E-beam Mask Inspection: HVM capable tool exists

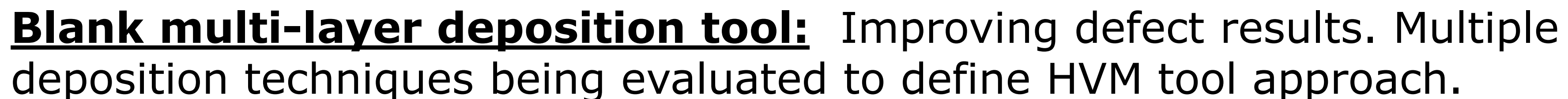
AIMS Mask Inspection: SEMATECH led tool development program

Actinic Blank Inspection (ABI): EIDEC led tool development program

Pellicle: C&F results demonstrated

EUV blank quality: Process and yield improvements ongoing

Actinic Patterned Mask Inspection (APMI): Required for post-pellicle inspection. Industry development framework definition required.


Blank multi-layer deposition tool: Improving defect results. Multiple deposition techniques being evaluated to define HVM tool approach.

EUV resist QC: Rapid turn resist QC infrastructure definition required

Standard mask process flow and tool sets

Blank Supplier

1. Substrate polish/clean/insp
2. Backside film deposition
3. Multilayer dep/insp
4. ML reflectivity monitor
5. Blank clean
6. Absorber deposition/insp
7. Shipping to customer

Patterning process

8. Blank inspect
9. Blank clean
10. Resist coating
11. E-beam patterning
12. Resist bake/develop
13. Pattern etch
14. Resist strip/initial clean

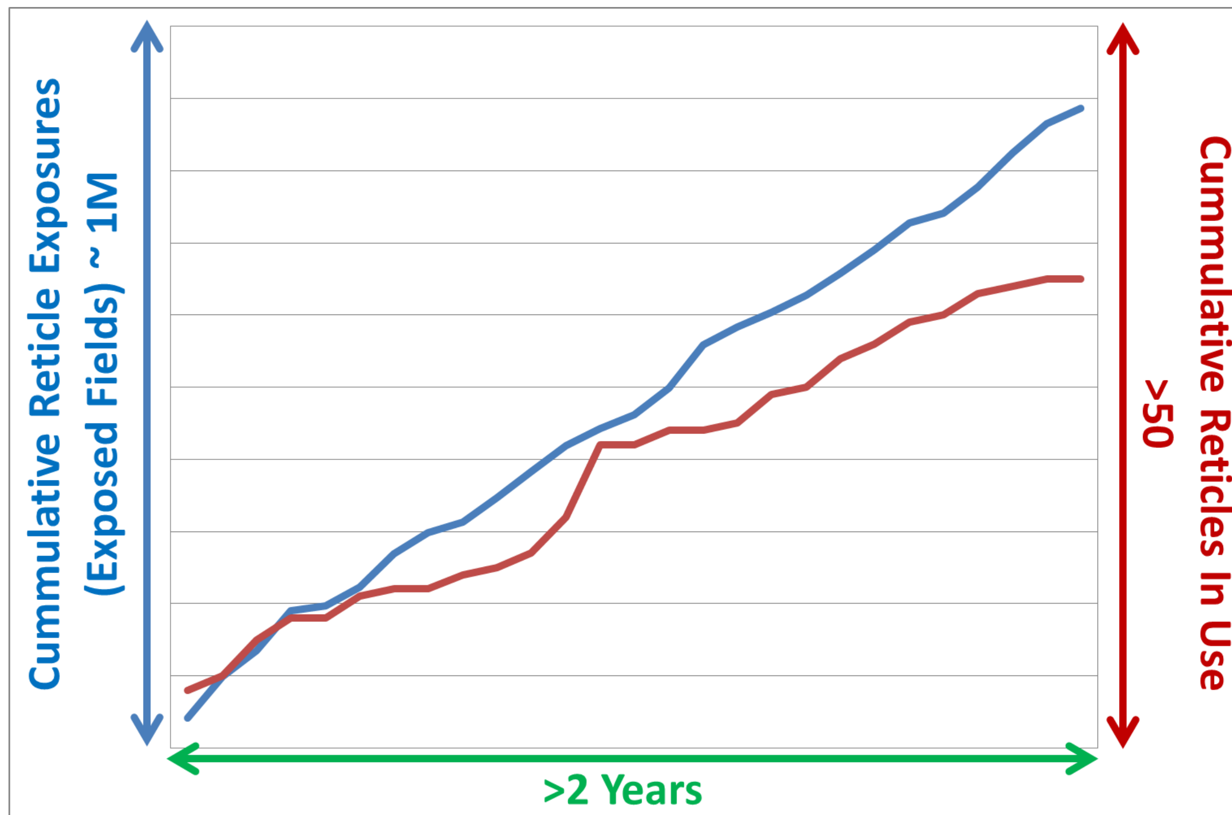
Metro/Charaterizaton

15. Def inspection
16. CDSEM metro
17. Pattern registration
18. Defect verification
19. Defect repair
20. AIMS*
21. Flatness metro
22. EUV reflectivity metro
23. Final clean
24. Inspection
25. Pellicle mount*
26. Actinic inspection (APMI)*
27. Mask transfer to EUV Pod
28. Shipping to Fab

- Blank quality improvement expected
- EUV mask fabrication process shares most optical mask tool sets
- Black-border and blank defect mitigation add additional steps in the process
- AIMS and pellicle are in development
- APMI tool development needs industrial collaboration

Foil from Guojing Zhang (Intel) et al. BACUS 2014, Monterey, California, USA, 9/18/2014

Significant experience with EUV reticles on NXE:3100



- > 300 reticles associated to NXE scanner platform fabricated since 2010
- The NXE reticles are closely monitored in their functionality, reliability and utilization.
- Several plates, each utilized over 2 years, exposed to >10kJ EUV irradiation
- **But** total dose and intensity much lower than required for HVM
- No experience with pellicles in place

EUV actinic metrology for reticles

Three actinic metrology techniques are critical for EUVL in HVM

- A-BI: actinic blank inspection, to check quality of multilayer reflector stack
- APMI: actinic patterned mask inspection, to detect minimum printing pattern defects, contamination or particles, and inspect through pellicle
- EUV AIMS: actinic aerial image metrology, to determine defect printability

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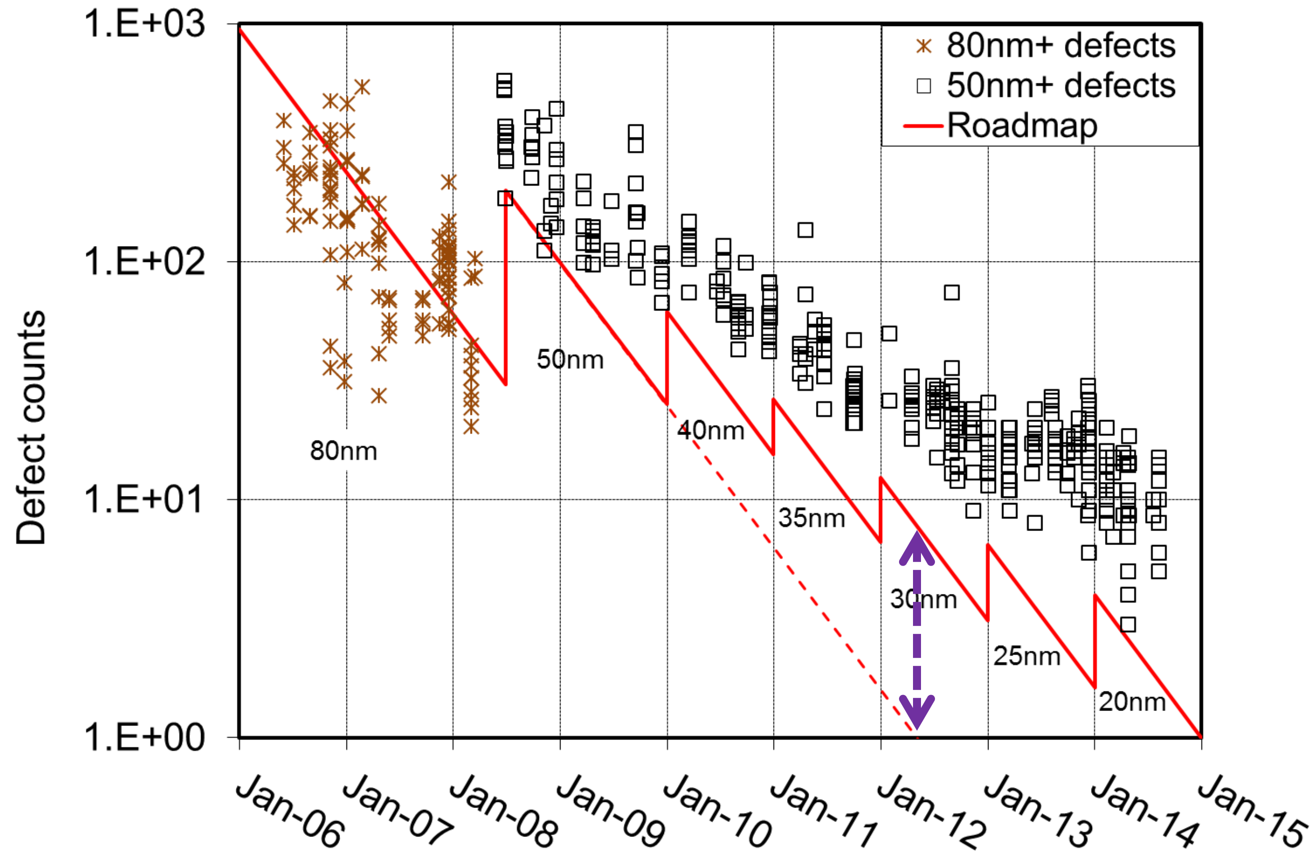
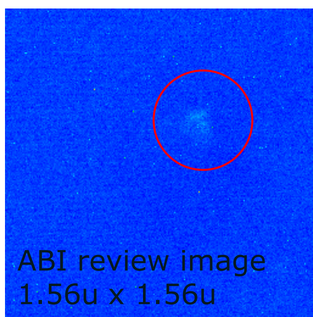
EUV Mask Blank ML Defect Reduction Trend

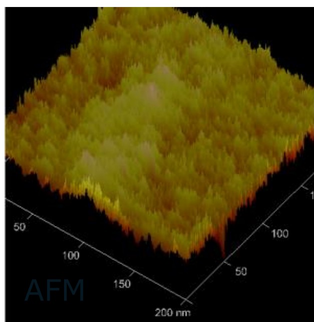


- Steady progress in reducing EUV mask bank defects
- Persistent gap with respect to the roadmap, but mitigation is possible (see later foils) if defects are identified
- Actinic inspection is required to identify all defects for mitigation

ABI new capability enables blank defect reduction and mitigation

Defect 68 – bump

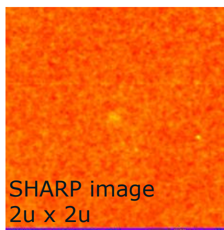


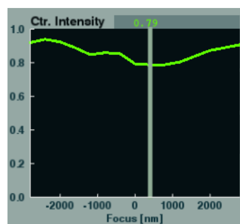


Height: 1.0 nm
FWHM: 36.8 nm

Figure 2: Actinic Blank Inspection Tool at the Lasertec facility in Shin-Yokohama, Japan

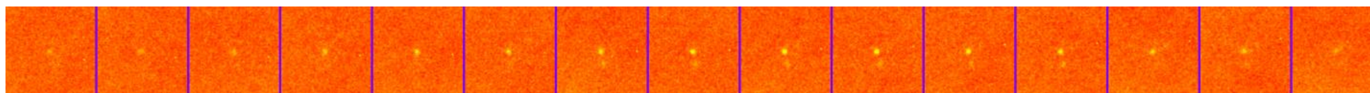
Source: Lasertec paper 2013 SPIE

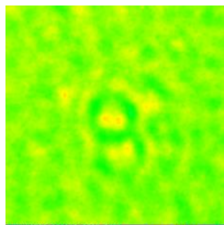


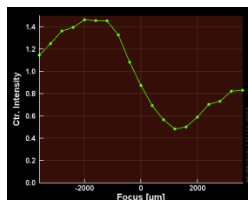


Annular (0.33NA, sigma=0.2-0.9)

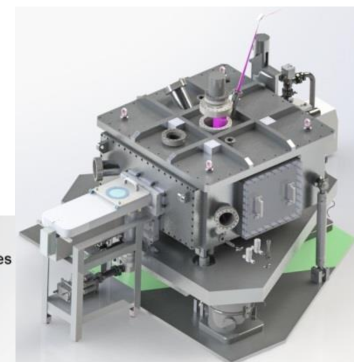
dz=0.4μm, 15 steps





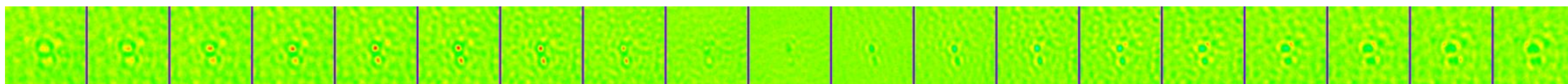


Coherent (sigma=0.1)



SEMATECH/LBNL

dz=0.4μm, 19 steps



Guojing Zhang et al. (Intel) BACUS 2014, Monterey, California, USA, 9/18/2014

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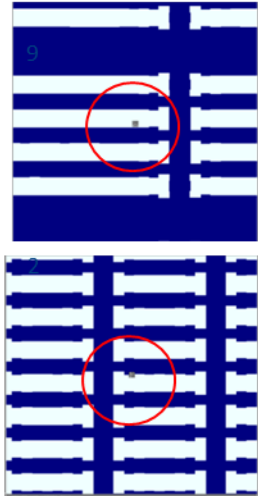
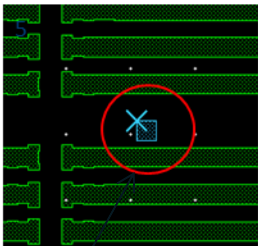
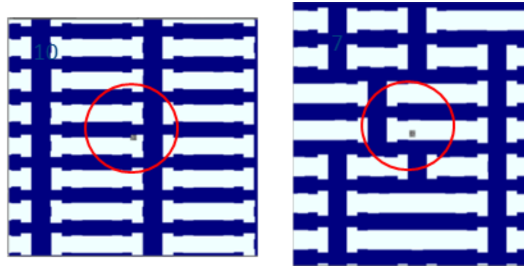
ML blank defect mitigation demonstrated

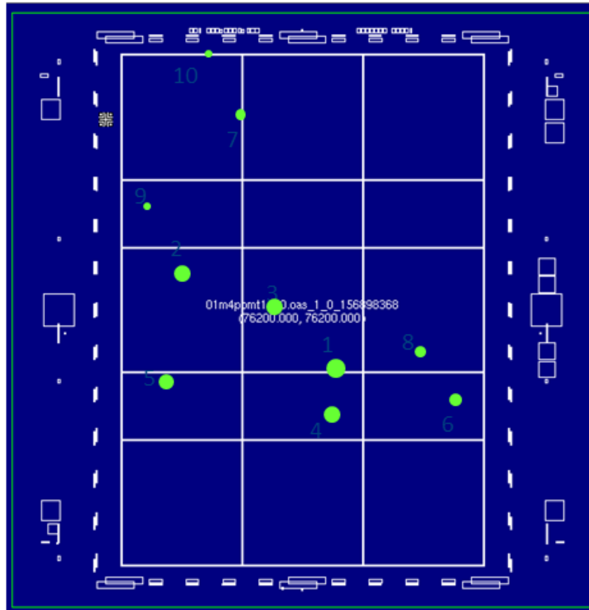
10 selected defects overlapped with the device pattern w/o mitigation

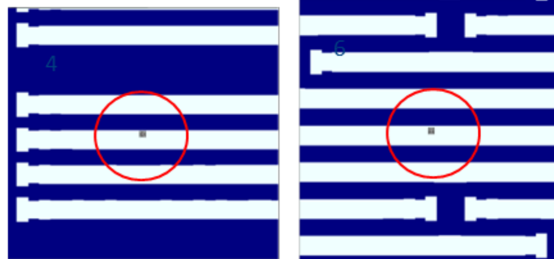




Only 1 defect is naturally covered





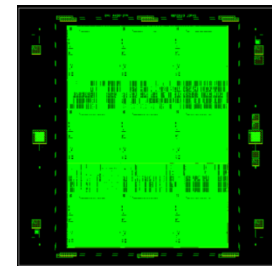


White: ML
Blue: absorber

Defect mitigation requirement

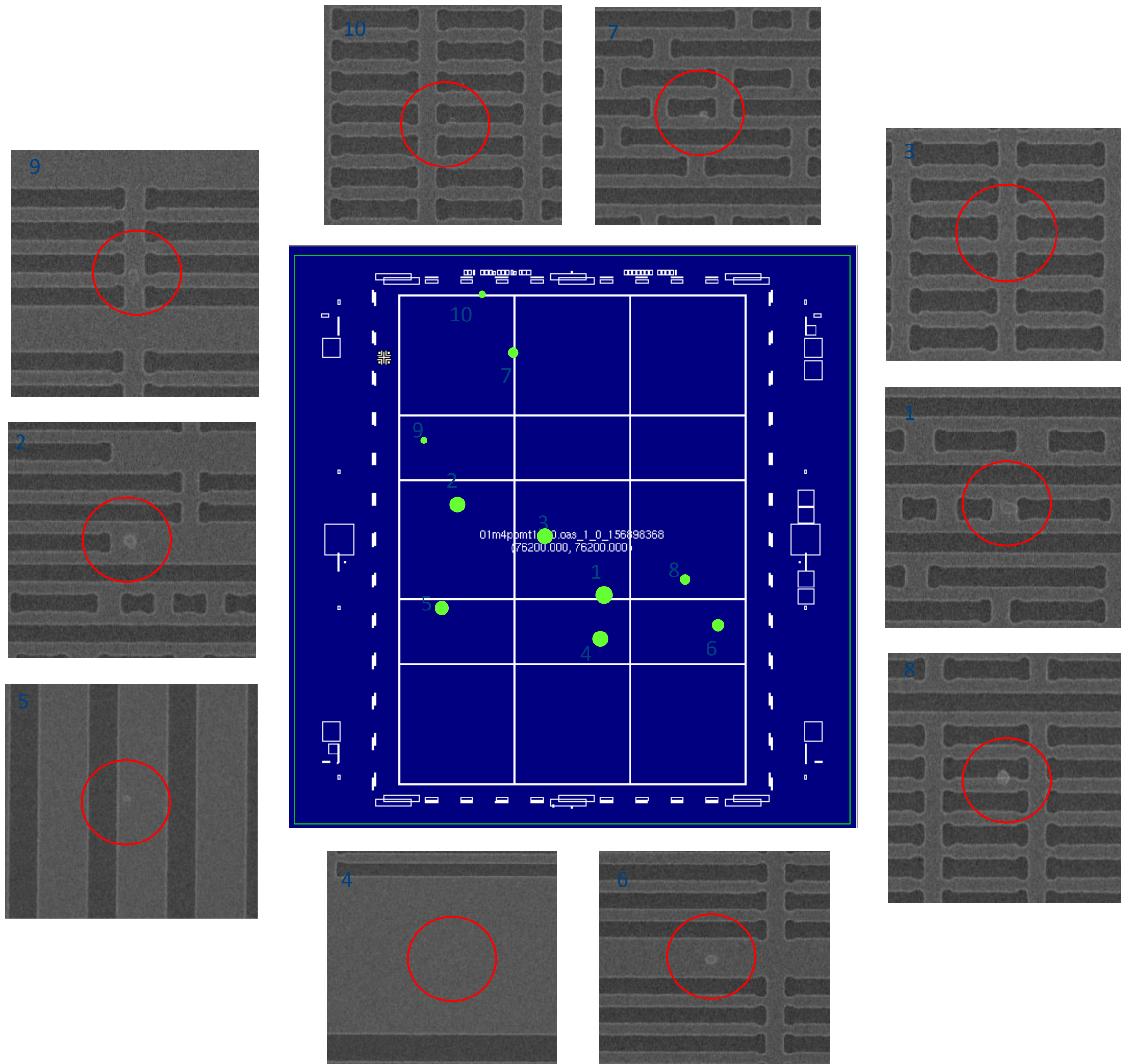
- ML blank defect coordinates from blank suppler
- Verification and correction of defect location (x, y) error
- Selection of # of defects to mitigate
- Simulation with a device for mitigation solutions
- Pattern shifting in e-beam write
- Confirmation of results

14nm device layout#1 at 25% pattern loading



Guojing Zhang et al. (Intel) BACUS 2014, Monterey, California, USA, 9/18/2014

ML blank defect mitigation results



Defect mitigation results

- Top 10 large defects selected for mitigation
- Defect size: ~100nm – 50nm
- Coverage rule: min. 150 nm absorber area
- Blank at normal origination
- 7/10 defects fully hidden
- 3/10 defects partially covered

Mitigation solution

X shift = -48.024um

Y shift = -161.333um

Guojing Zhang et al. (Intel) BACUS 2014, Monterey, California, USA, 9/18/2014

EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs

1 is ready now, 4 are in development, 3 have significant gaps

E-beam Mask Inspection: HVM capable tool exists

AIMS Mask Inspection: SEMATECH led tool development program

Actinic Blank Inspection (ABI): EIDEC led tool development program

Pellicle: C&F results demonstrated

EUV blank quality: Process and yield improvements ongoing

Actinic Patterned Mask Inspection (APMI): Required for post-pellicle inspection. Industry development framework definition required.

Blank multi-layer deposition tool: Improving defect results. Multiple deposition techniques being evaluated to define HVM tool approach.

EUV resist QC: Rapid turn resist QC infrastructure definition required

Pellicle imaging test results

ASML

Public

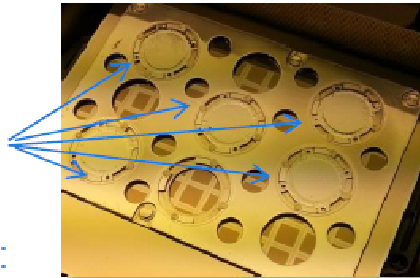
Slide 11

Summary imaging tests results with pellicles

No measurable impact of pellicles in imaging (within measurement noise)

ML Imaging tests

5 pellicle positions
20 mm diameter,
25 nm thickness



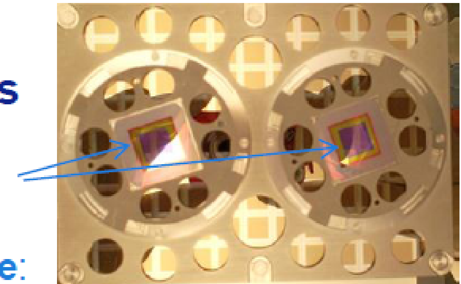
Imaging performance:
- Small decrease in process window, difficult to calculate due to strong process fingerprint
- DOF range without pellicle limited by available focus fields on wafer

Defectivity performance:
- Large printed particles (~ 30um to >100um) due to pellicle manufacturing/handling outside cleanroom

ML pellicle film quality:
- Impact of pellicle/wrinkles not visible

Poly-Si Imaging tests

2 pellicle positions
11mm x 11mm, 75 nm thickness



Imaging performance:
- No measurable difference w/ and w/out pellicle: no variation in exposure latitude and focus window (all within measurement noise, strong process fingerprint)

Defectivity performance:
- No measured printed particles in imaging data

pSi pellicle film quality:
- Variation in EUV transmission observed in CD variation; pellicle manufacturing process improvement required

From Jim Wiley, IEUVI Mask TWG, 6 Oct 2013

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Scalability of free-standing pSi films demonstrated and prototype pSi pellicles successfully tested in EUV tools

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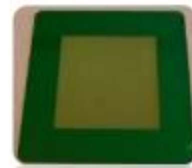
Slide 1
27 Oct 2014

11mm x 11mm (~80% EUV transmission)

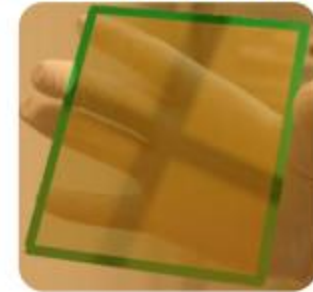


50mm x 50mm (~82% EUV transmission)

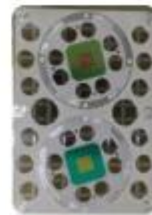
Half size prototype

64mm x 106mm ~(86% EUV transmission)

Full size prototype



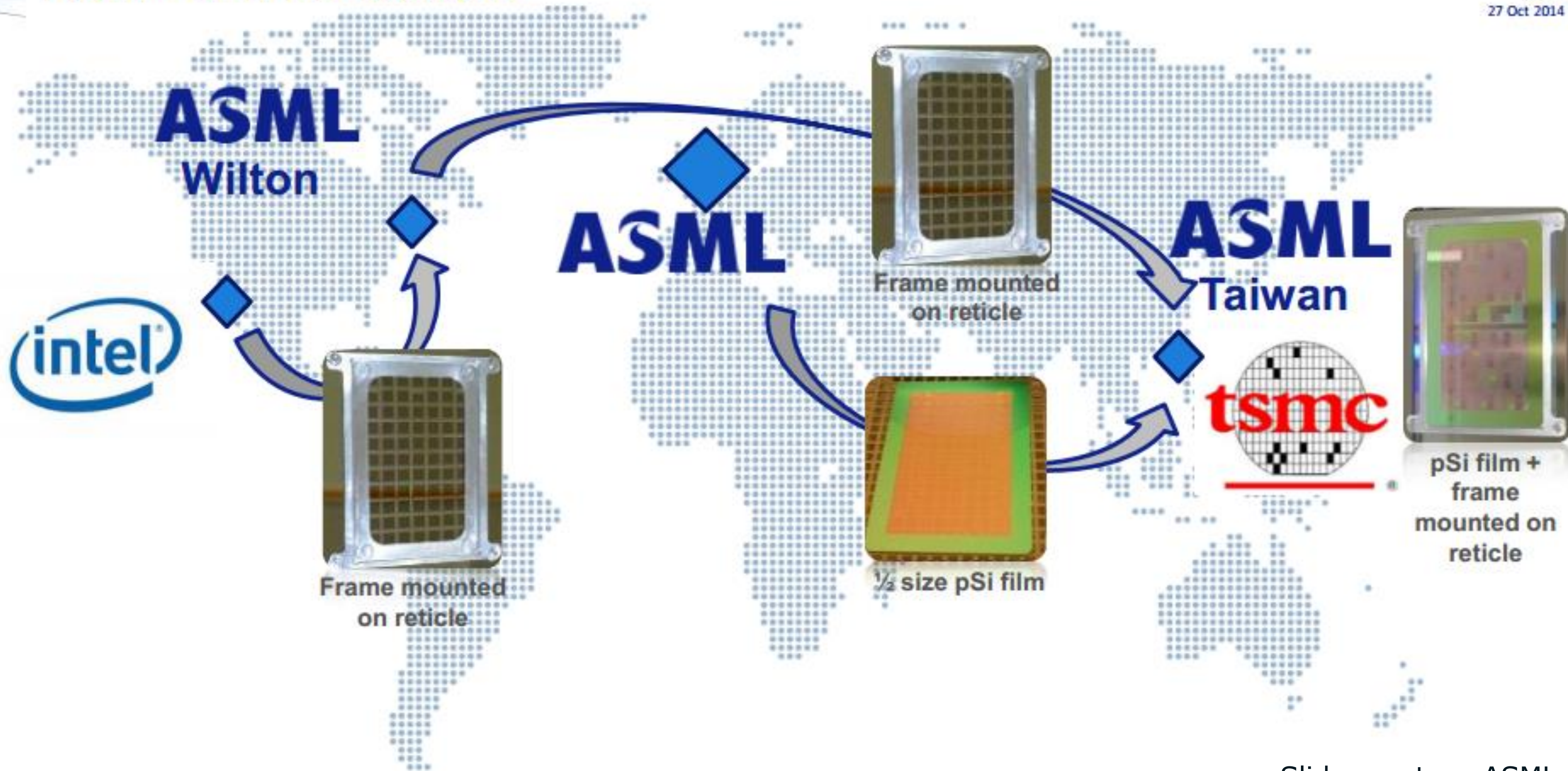
103mm x 122mm (~85% EUV transmission)



Open frames used for testing prototype pSi pellicles in EUV tools

All reticles and frames courtesy of Intel

Slide courtesy ASML



Slide courtesy ASML

~50nm free-standing membranes are now routinely shipped around the world undamaged via ordinary shipping

27 nm L/S features successfully exposed with half-size proto pellicle

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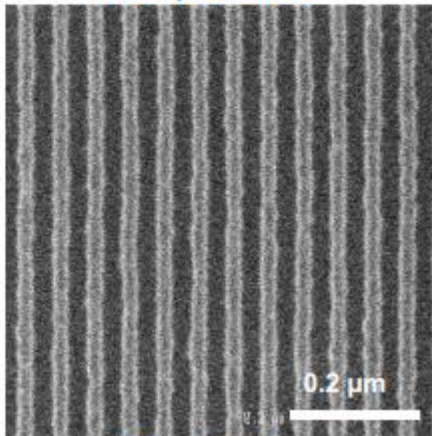
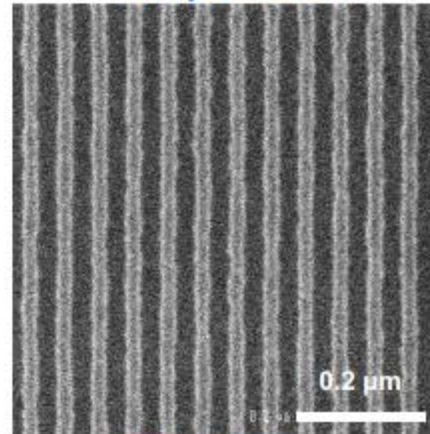
27 Oct 2014

SEM image at BE/BF w/o pellicle



CD = 24.2 nm
LWR = 4.0 nm

SEM image at BE/BF w/ pellicle



CD = 24.0 nm
LWR = 3.7 nm

- NXE:3100, NA=0.25, Conventional Illumination
- CDU difference of 0.18 nm
- Pellicle EUV transmission confirmed in imaging data: 85.5% (single pass)

Joint effort of NXE end users and ASML accomplished imaging results of half size pellicle

Scanner exposures courtesy of tsmc

Reticles and frames courtesy of Intel

Slide courtesy ASML

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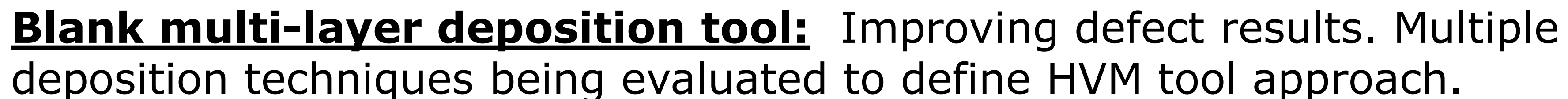

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EUV pellicle changes only timeline of APMI need

- APMI has always been on roadmap
  - Required for adequate sensitivity with reasonable productivity (inspections ~ hours)
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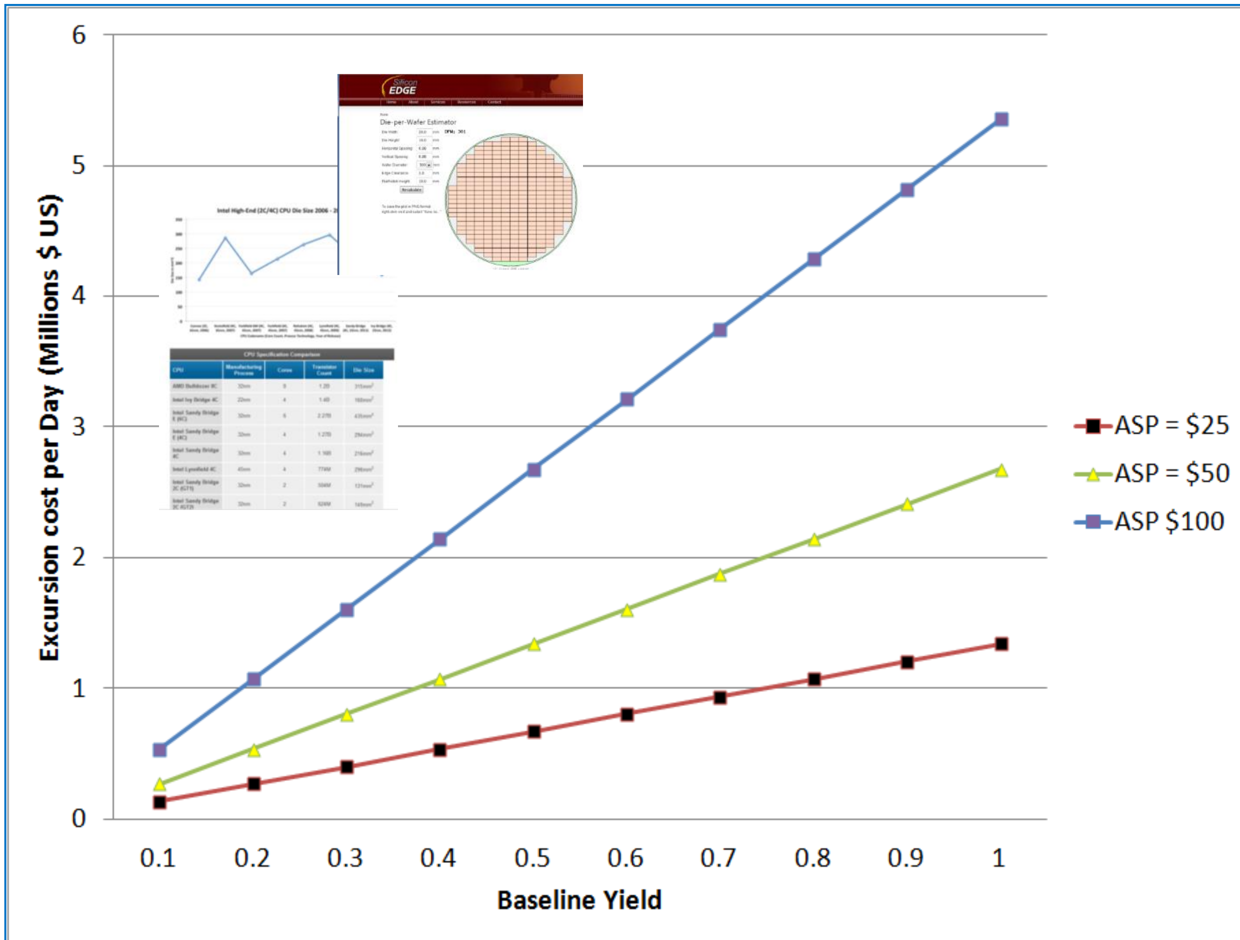
Daily cost of a reticle fall-on particle excursion



Model assumptions:
- Critical area = die area
- 200 mm^2 die
- 300 die per wafer
- Fab capacity = 5000 wafer starts per week.
- Based on representative data from semiconductor industry

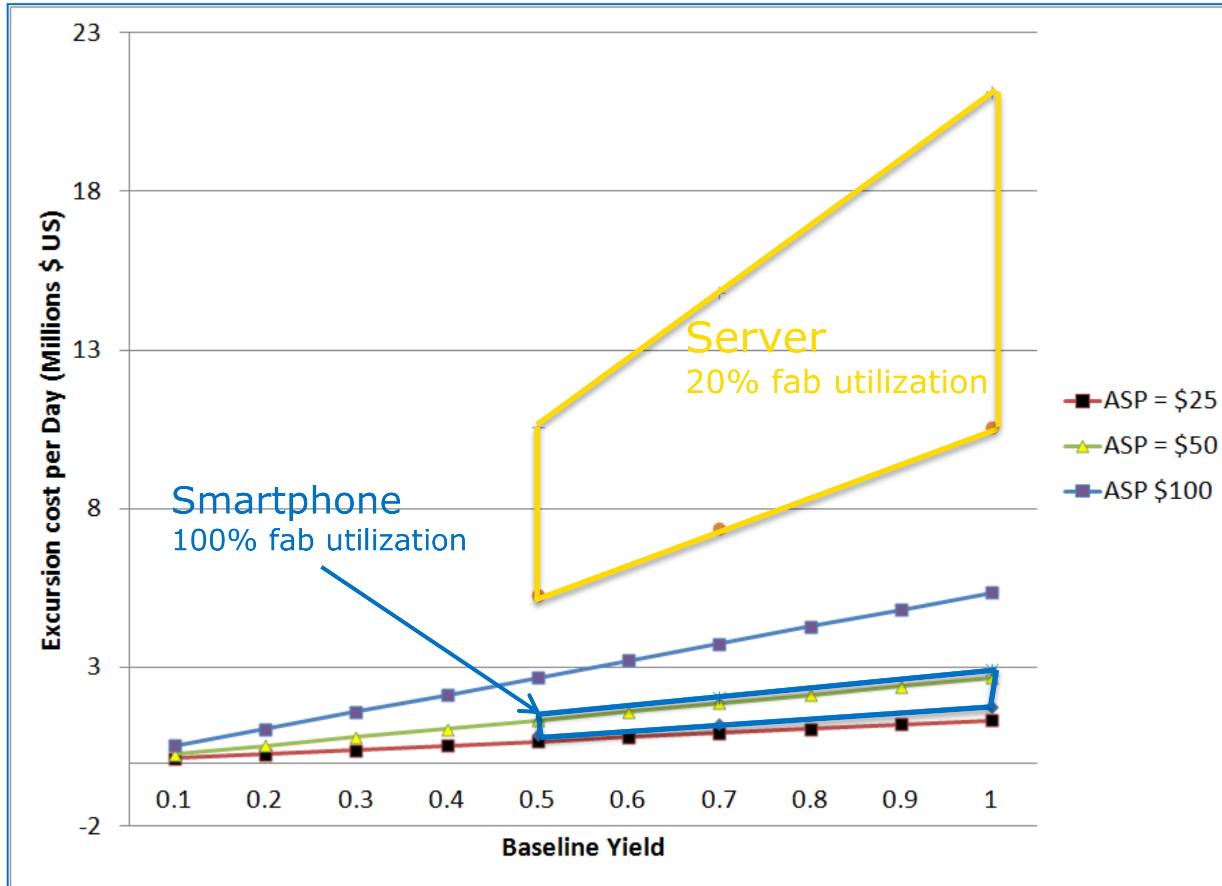
Die sizes from http://www.anandtech.com/show/5771/the-intel-ivy-bridge-core-i7-3770k-review/3

DPW estimate: http://www.silicon-edge.co.uk/j/index.php?option=com_content&view=article&id=68

Reticle defects are tremendously expensive

From: Tim Crimmins (Intel), SEMICON Korea 2013

Daily cost of a reticle fall-on particle excursion



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ASP estimates from:
www.anandtech.com
www.techrepublic.com
www.isuppli.com
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Bottom line: need to drive PRP below 0.0001

From: Tim Crimmins (Intel), SEMICON Korea 2013

EUV pellicle changes only timeline of APMI need

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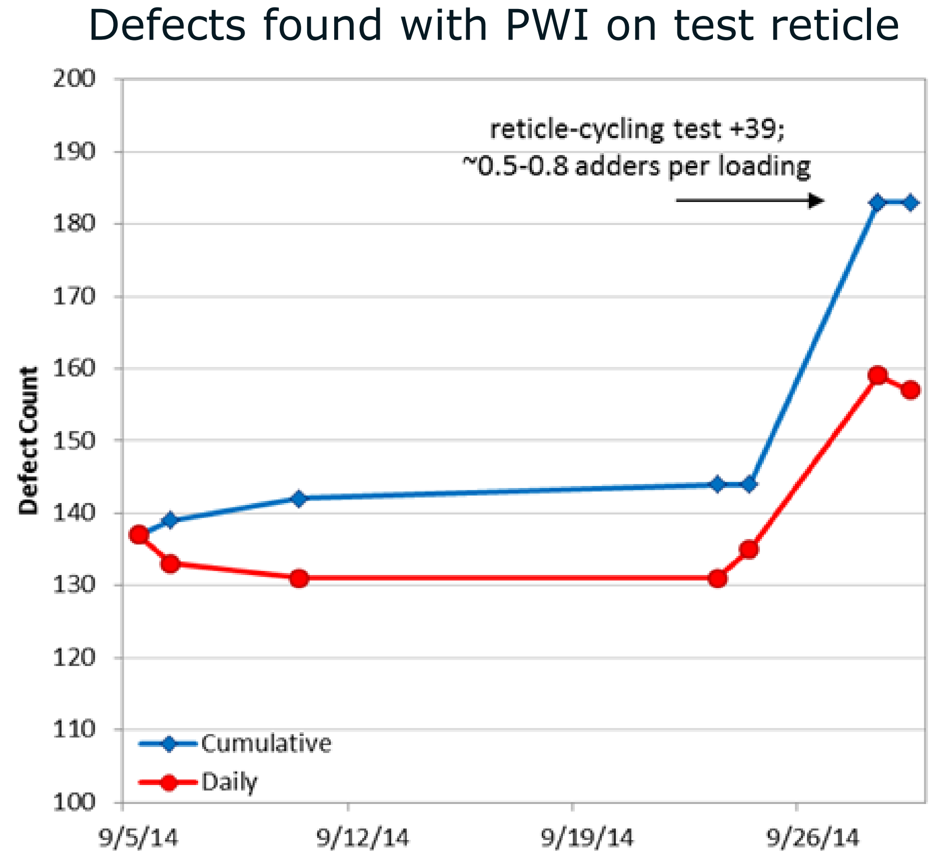
Initial reticle defect trending NXE:3300

- Tool is starting off cleaner than initial data on NXE:3100
- Tool will undoubtedly clean up further over time
- But current performance is >5000X HVM requirement (1 adder in 10^4 reticle loads)
- Testing to HVM requirement would take ~50 days of reticle cycling
- As tool performance exceeds 0.01 PRP, **most tests will show zero adders**



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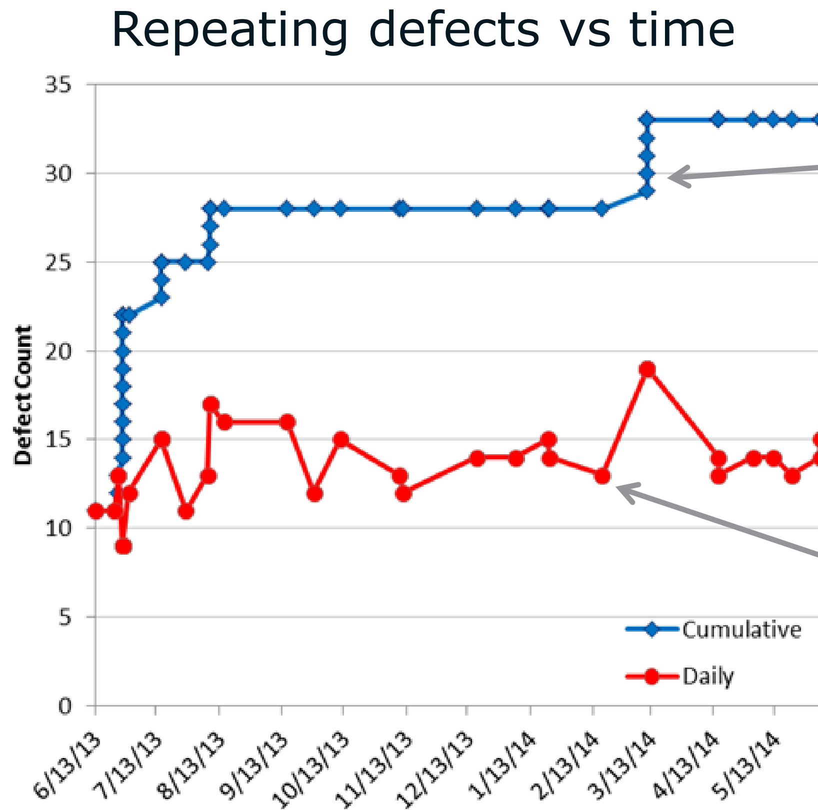
PWI trending – loose geometry



Cumulative, unique defect locations (added particles)

Defects found in individual inspections

- PWI is good at giving a statistically-relevant trend of wafer defects
- Stability of both scanner and inspection tool affect which reticle defects print and are captured in a given run.

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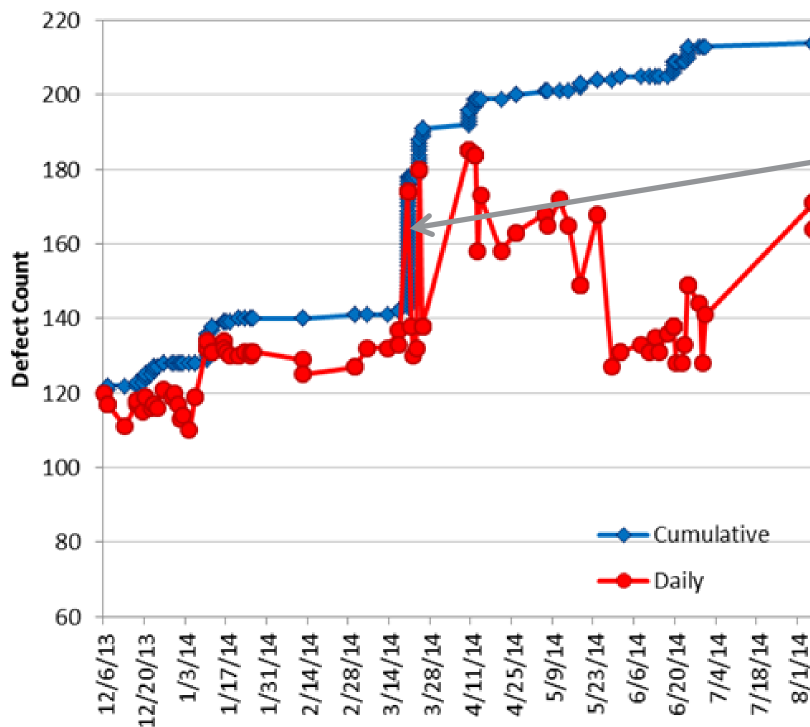
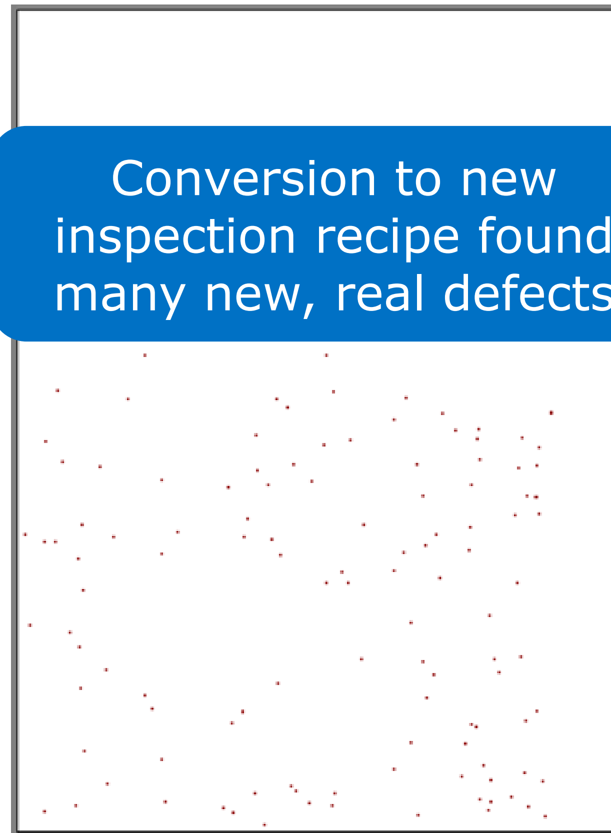
PWI trending – tight L/S defect test reticle





- PWI will only become more difficult as EUV pushes to smaller features
- Even today, PWI is not capable of determining whether a reticle has 0 or >0 printing defects

APMI conclusions

- Through-pellicle actinic mask inspection has been a vital component of quality control in mask shops and wafer fabs for decades

- In addition to particles or damage caused by pellicle mounting, through-pellicle inspection captures and contains ESD damage, chrome migration, and photo-induced defects (PIDs) *none of which were expected.*

- To date, only optical PMI techniques have adequate productivity for mask shops and wafer fabs

- Only EUV APMI can guarantee the overall integrity (ML stack and absorber) of a pelliclized EUV reticle. PID mechanisms for EUV masks are unknown, but only APMI can catch them.

- Other techniques (e.g. e-beam, PWI) are adequate for TD and perhaps initial HVM (depending on the product) but given the long lead time, APMI tool development needs to start now.

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EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs

1 is ready now, 4 are in development, 3 have significant gaps

E-beam Mask Inspection: HVM capable tool exists

AIMS Mask Inspection: SEMATECH led tool development program

Actinic Blank Inspection (ABI): EIDEC led tool development program

Pellicle: C&F results demonstrated

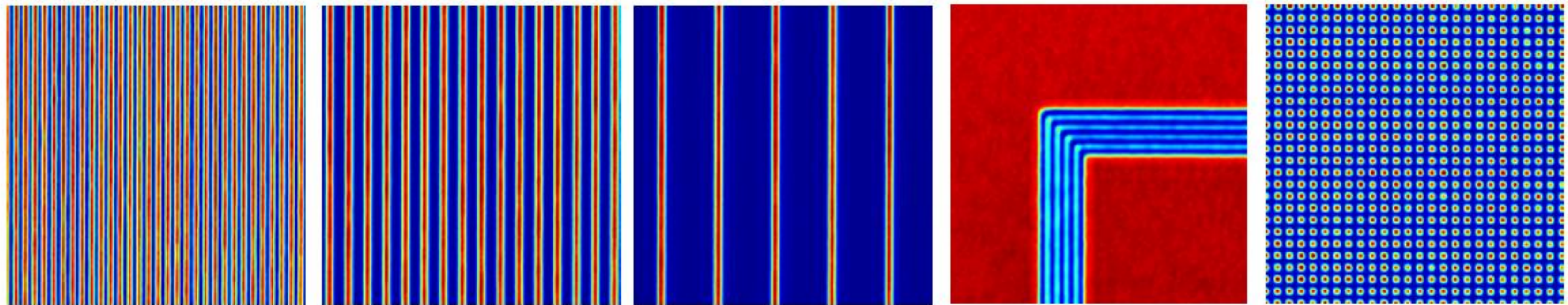
EUV blank quality: Process and yield improvements ongoing

Actinic Patterned Mask Inspection (APMI): Required for post-pellicle inspection. Industry development framework definition required.

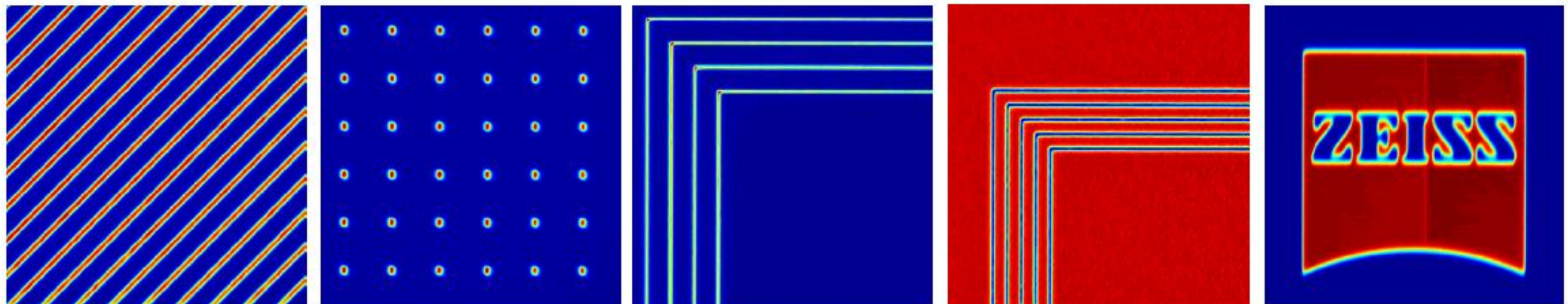
Blank multi-layer deposition tool: Improving defect results. Multiple deposition techniques being evaluated to define HVM tool approach.

EUV resist QC: Rapid turn resist QC infrastructure definition required

AIMS™ EUV images from EMI prototype system



CD/Pitch:	64nm / 128nm	64nm / 256nm	64nm / 768nm	64nm / 128nm	80nm / 160nm



CD/Pitch	64nm / 640nm	128nm / 1280nm	64nm / 640nm	64nm / 384nm	6µm x 6µm

Source: Courtesy of Zeiss

- Adequate imaging performance at the first light demonstrated for target application at 7nm logic node
- System integration and operation reliability will be tested for EUV mask manufacturing

Guojing Zhang et al. (Intel) BACUS 2014, Monterey, California, USA, 9/18/2014

No change from 2013 Workshop

Challenge to actinic metrology source community

Based on input from metrology tool suppliers and Intel metrology experts:

- Existing sources do not meet brightness, homogeneity, stability, and COO requirements
  - Requirements are feasible, but already late to need
  - Requires focused development activity and funding
- Requirements are specific to each tool design, and are proprietary
  - Source is an integrated part of tool design
  - Correct model is funding through metrology tool suppliers

Conclusions

- Solid progress in last year, with realization of 40~80W stable MOPA+PP sources in the field
- Availability is not adequate for process development and needs substantial improvement over next two quarters
- *In situ* collector cleaning looks promising, but needs to be delivered to field to gain confidence in OpEx and stable productivity
- Continued progress on source power per roadmap is required to build confidence in long-term productivity targets and COO
- EUV infrastructure is now lagging scanner and source, and needs increased focus

Acknowledgements

Yan Borodovsky (Intel)
Steve Carson (Intel)
Ted Liang (Intel)
Rajesh Nagpal (Intel)
Sam Sivakumar (Intel)
Guojing Zhang (Intel)
Steve Johnston (Intel)
Brian McCool (Intel)