APPLICATION NOTES

- Clarification of Non-repetitive On-state Surge Current Ratings
- Insight Into Proposed Ratings for Pulse Power Applications
- SPT400 Series 125mm Thyristors

SILICON POWER

I. INTRODUCTION

A. Need for Highest Power Thyristors

There is a growing need in the market for thyristors of the highest voltage design that can endure heavy fault currents as experienced in new electrical power systems or operating in the pulse power mode as for military weapons and other government laser and magnet supplies. An example of a milestone already past is the installation of 100 mm thyristors on the 500 kV AC transmission line of BPA-Slatt substation: thyristor controlled series compensation, {TCSC} [1]. In that application, the most demanding parameter to meet was the high multi-cycle asymmetrical fault current. It was necessary to predict fault withstand capability [2] according to the highest available standard as designated faults were to be expected and not considered as rare occurrence. Pulse power duty, on the other hand, are single shot events with durations usually less than 8.3 ms and peak current much higher than normally encountered.

When circuit designers encounter more of these stringent surge duty applications, they are sure to realize the inadequacy of normally published surge current data. Moreover if they are to make an evaluation and choose from contending devices using non-repetitive surge current, I_{TSM} ratings as an essential criteria, they will be mislead. Consequently one should make specific inquires to thyristor manufacturers so as to develop a mutual understanding of the real surge current requirement. including details about verification testing and life expectancy.

B. Surge Current Standards

Thyristor standards for surge current are not meant to be indicative of the aforementioned applications. Surge on-state current, I_{TSM}, as defined in IEC thyristor standard *[747-6 para. 3.2.17]* is *as being of short duration and specified waveshape whose application causes the maximum rated virtual junction temperature to be exceeded. It is assumed to occur rarely and with a limited number of such occurrences during the service life of the device and to be the consequence of unusual circuit conditions (for example a fault).*The defined event may / may not include a requirement to block reverse voltage.

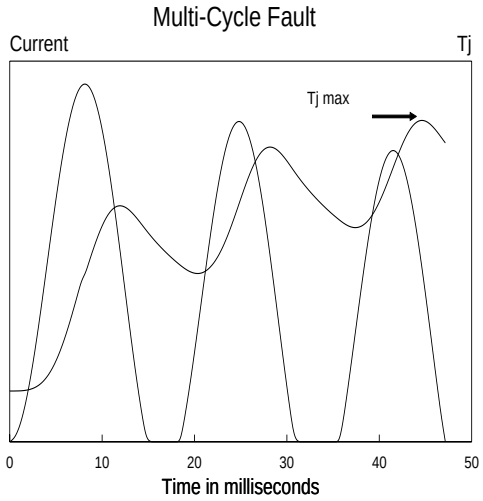

Fig.1 Type of computer representation of a multi-cycle fault showing current waveform and resulting junction temperature excursion.

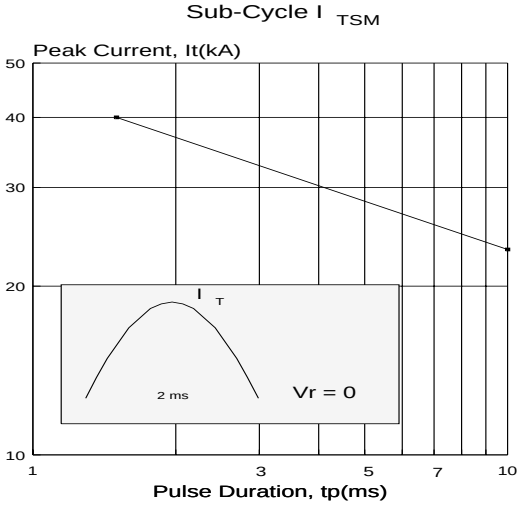

Fig. 2 I_{TSM} as represented through the sub-cycle range. This curve is used to coordinate with fuse let-thru current.

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Although the number of occurrences is not defined by IEC, JEDEC [*EIA RS-397]* states that *the number of surges to be applied shall be 100.* This appears as part of the verification test procedure.

The specific methods proposed by both standards are difficult to use with high power thyristors if pulsating reverse voltage is to be applied. IEC provides the option of not applying voltage for the single cycle rating and both standards specify no reverse voltage for sub-cycle ratings.

C. Ambiguity of Interpretation

Because I_{TSM} is defined as a rare occurrence, standards rightfully do no imply life expectancy [*This is in contrast to the new requirements for pulse power for which the number of "shots" in life enters into the rating. Predictability of life [3] is based on relating junction temperature excursion, ΔT_J, to fatigue failure or fracture within the silicon.*] Since I_{TSM}, is not governed by a strict standard, ratings are subject to wide interpretations among manufacturers, some being conservative and others optimistic while complying with the standards.

I_{TSM} data properly used is in combination with the let-thru currents of fuses for protecting or isolating the power semiconductor devices within unusual service conditions.

E. Verification Test Setup

Given a 5000V/5000A thyristor having a published I_{TSM} of 70,000A, how would a circuit designer compare this surge rating to that of another manufacturer who claims either a higher or lower I_{TSM} for a similar device? What kind of a methods do these manufacturers use to establish such ratings and how would a user verify what is actually needed? Could there be test criteria that contending manufacturers and user-buyers can agree upon on that is devoid of ambiguity?

Testing of this sort requires a laboratory setup under established safety conditions. By its nature, it is a type test usually performed on new product types within one's engineering facility.

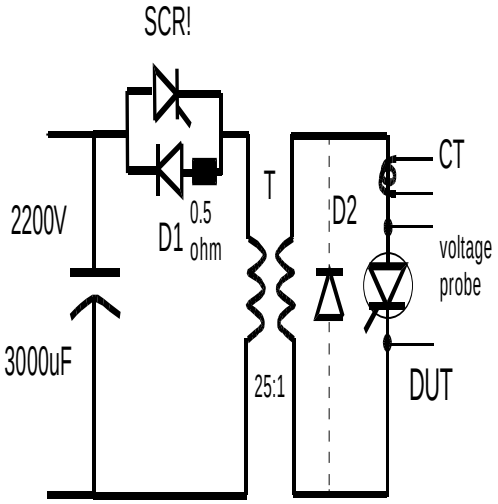


Fig.3 Type of laboratory circuit used to verify or establish ratings for I_{TSM} and pulse power

II. VERIFICATION TESTING

A. Laboratory test setup

A laboratory setup similar to that of Fig.3 is used by the authors to establish or verify single surge cycle ratings or to explore and establish new ratings for pulse power applications up to 200 kA. Recently some thyristors were purchased from local distributors to test for information purposes. It was decided to perform an evaluation of their corresponding 8.3ms I_{TSM}'s.

B. Proposed evaluation criterion and application to thyristors on the market

Specific failures modes in thyristor structures when subjected to short pulses are well documented, such as given in [4]. What is less known, however, is the theory of thermal runaway described by Freydin [5] and followed up by others in [1] and [2].The onset of this phenomenon is readily detected and is described in the section ahead. At this point it suffices to say that *any device exhibiting thermal runaway, when subjected to its rated I_{TSM}, even though not failing in test, is not acceptable*.

The results of testing various devices purchased from the market to their rated I_{TSM} and the evaluation according to the above criterion are tabulated below. Each was classified as **C** conservative, **S** satisfactory or **U** unacceptable. The results were mixed, ranging from conservative to unacceptable.

TABLE I
Evaluation Results for Various Thyristors

Manf. Code	Thyristor Si diameter (mm)	I_{TSM} Rating (kA)	Evaluation Code
A	77	59	**S**
B	77	55	**U**
B	77	45	**S**
B	53	20	**C**
C	53	27	**C**
C	30	10	**U**
D	53	32	**U**
D	40	19	**U**
E	53	23	**C**

Code: **C** conservative rating
S satisfactory rating
U unacceptable, exhibiting thermal runaway

C. Explanation of thermal runaway

Thermal runaway is caused by a rapidly increasing power which exceeds the capability of proper dissipation. This is induced when the change of on-state voltage which is normally positive for surge currents begins to increase drastically. This change, $\Delta V_{T,}$ expressed as *millivolt/^{o}C*, in Fig. 4 increases according to a complex function, dependent on both current level and temperature. As the temperature changes between 200 - 350^{o}C the function becomes sharper in a positive manner and then beyond 400^{o}C it becomes drastically negative.

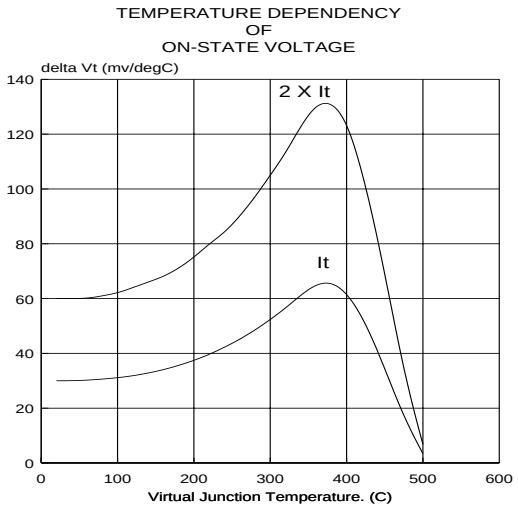


Fig.4 The change in on-state voltage per degree Celsius is shown as a complex function of temperature. Two current levels are plotted.

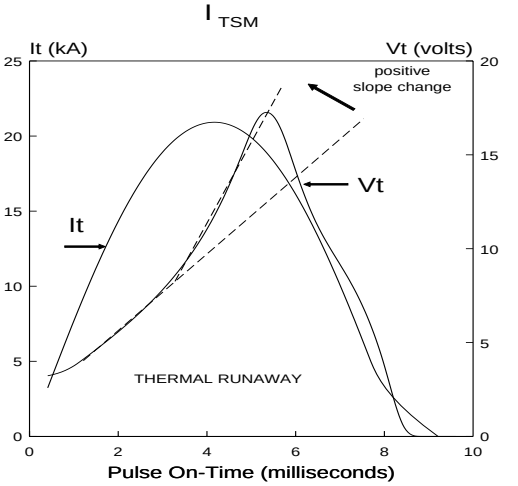
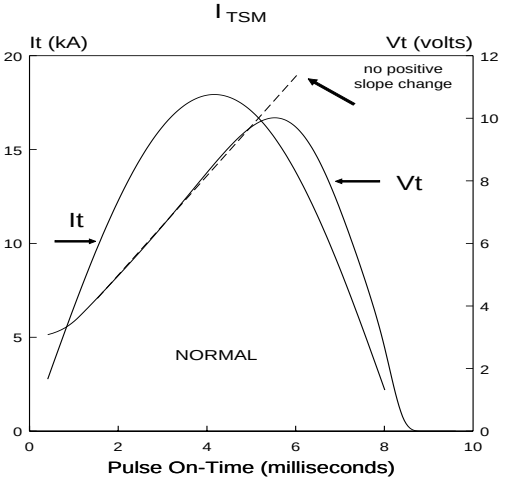


Fig.5 above and Fig. 6 below show I_{TSM} waveforms with and without evidence of thermal runaway.



This behavior is observed readily in test and has been discussed in detail by the authors in [2]. The rapid decrease above 400°C has been discussed briefly in [1] & [5] explaining how it causes "current squeezing" or "funneling" of the surge current and failure of the device. In brief, during a high current surge current, the silicon temperature can soar above 400°C, sufficient for the thermally generated intrinsic carriers to dominate the conduction process. Since the intrinsic carrier concentration is strongly dependent on temperature, any localized area of higher temperature will have higher intrinsic carrier concentration. When this occurs, the current funnels into these areas, further increasing the local temperature, causing thermal runaway and ultimate destruction of the device.

D. Detection of thermal runaway

The onset of thermal runaway can be seen on test voltage waveform if it starts increasing when it should be decreasing. A representation of this sudden increase is depicted in Fig. 5 using an empirically based computer model. The normal case for comparison is shown in Fig. 6. These apply for half sine pulses of 8.3ms duration. Other pulse power waveforms show the same behavior but appear differently in accordance with the duty profile and the thermal time constants as in Fig. 7 & Fig. 8.

III. RATING FOR PULSE POWER

A. General Description

Pulse power involves the storage of energy until it is released at very high power levels. Dethlefsen [6] has bracketed the requirements for suitable solid state power switches as falling within the following envelope:

- blocking voltage, 5 to 60 kV
- peak current, 5 to 200 kA
- pulse widths, 0.1 to 1000 ms

Some of the applications encountered by the authors have di/dt requirement >1000A/ms requiring special considerations on device design and method of gating. Investigations are currently performed in the range of 500 to 1000ms pulse duration and up to 200 kA.

B. General Approach to Pulse Power Ratings

A combination of surge current testing such as according to Fig.1 and an empirically based computer model [2] are used. The exact current profile needed for the application is used in both cases. It is verified based on test that thermal runaway does not occur by observing the V_T vs. time or the I_T vs. V_T loop. An internal examination of the device is made to ensure that the mating surfaces are not arcing or spitting as due to insufficient metallization or flatness.

Next, DT_J for the hottest portion next to the gate boundary is determined by computer model, considering the finite expansion rate of the turned-on region in combination with the gate geometry. Finally life expectancy in terms of the number of shots is determined as in [3], that is:

$$\#\ \text{shots} = (\ 300\ /\ DT)^9$$

using Celsius temperature

An example of a rating for a 12 kV thyristor, switch (using three 125mm SPT402 thyristors in series) is shown as Fig. 9. It is presented for half sine pulses at three levels of life expectancy. The pulse waveform will vary for specific cases, varying from job to job.

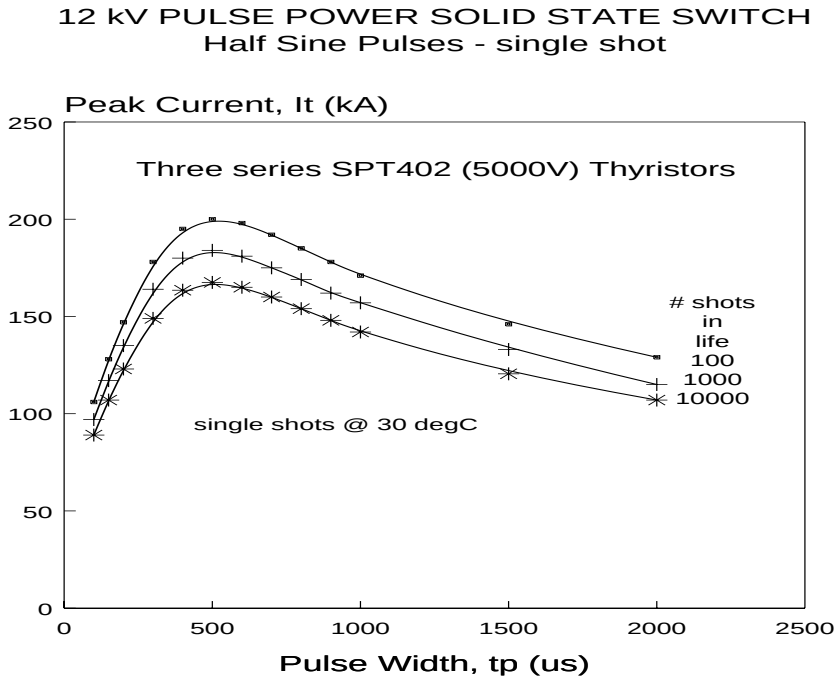


Fig.9 Pulse power rating curves for a 12 kV thyristor switch with alternative life expectancy choices for increased power.

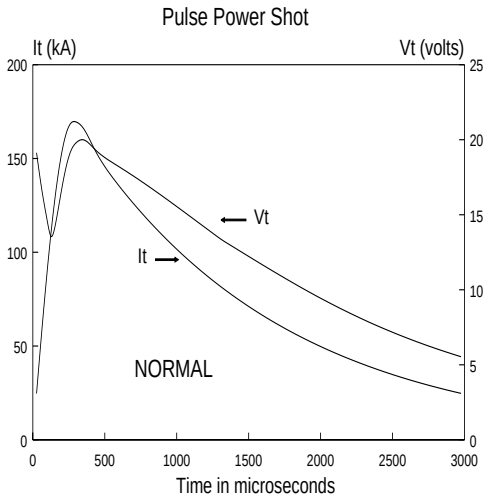
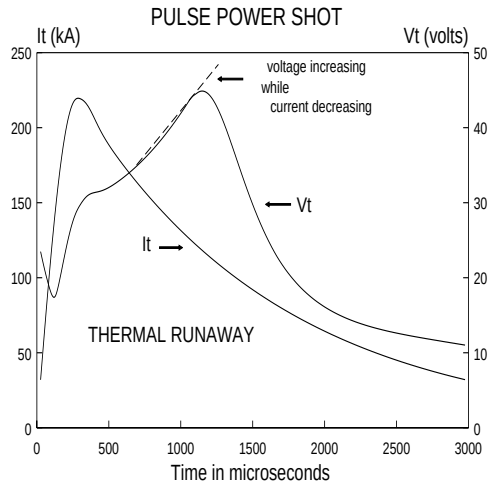


Fig.7 above and Fig. 8 below show waveforms of a particular pulse power shot with and without evidence of thermal runaway.



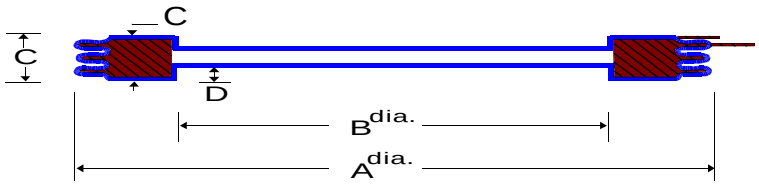
IV. 125mm THYRISTORS

A. Design Concept

The authors belong to an engineering team responsible for design and manufacture of the SPT400 series of 125mm thyristors. These are designed to meet the special requirements of the emerging markets for electrical power FACTS systems, military weapons, ship power propulsion & control and commercial ventures using pulse power switches.

A decision was made after consulting with several customers and the military to house it in a light weight low profile plastic disk package as shown:

Plastic Package



Nominal Dimensions

	inch	mm
A dia.	6 13/32	162.7
B dia.	4 3/16	106.4
C	43/64	17.06
D	0.230	5.84

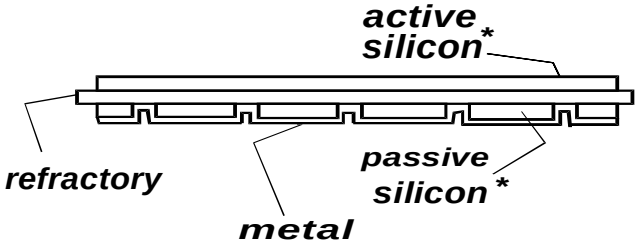
Weight: 18 oz

Internally, a flat junction assembly is accomplished in design by novel means, taking advantage of compensating forces which prevent any tendency for the silicon to bow while cooling down from the process temperature at which it is bonded. The figure below shows the concept of having a layer of inactive silicon of equal thickness to the electrically active silicon, separated by a very thin refractory layer. Bonding the anode to a relatively thick substrate used in conventional designs is not used for this large diameter, but unlike the "free floating" or "alloy free" silicon junctions assemblies offered by off-shore manufactures with "dry" interfaces on both silicon sides, the thermal advantage offered by bonding is achieved.

lightweight alloyed construction

(PATENT APPLIED FOR)

(alloyed interface needed for pulse duty)



*** both silicon thicknesses matched for zero bow***

V. TEST RECORD / SPT407 2500V 125mm THYRISTOR

I_{TSM} for 8.3 msec = 100 kA

T_{case}= 125°C ; V_R=0

Test Recordings @ T_{CASE} = 125°C

V_T versus time trace meets the conditions set forth is Section II and Fig. 6 for an acceptable I_{TSM} rating of 100 kA, that is without evidence of thermal runaway as defined by the authors.

Corresponding I_T vs. V_T loop

VI. Overall Comments

I_{TSM} ratings must be properly understood. These apply for unusual circuit conditions such as surviving when other components fail and for coordinating with fuses.

I_{TSM} ratings should not be used as criteria for comparing contending vendors as the standards provide only conceptual insight into understanding this rating; consequently it is subjected to broad interpretations. Allowing this, a vendor who provides a conservative rating would be evaluated unfavorably compared to one with an optimistic rating.

Predictability of surviving multi-cycle fault currents requires knowledge of the temperature dependency of the on-state voltage beyond 125^{o}C and well beyond the 250^{o}C. A relationship is needed for on-state voltage representing changes over this very wide temperature range and used with proper thermal representation in a computer model.

Pulse power ratings are usually of sub-cycle duration and very high peak currents: these should be backed up with proper test verification and linked to an empirically based computer model so as to determine ΔT_J and resulting life expectancy.

REFERENCES

[1] D.J. McDonald, J. Urbanek, B.J. Damsky, *Modeling and testing of a thyristor for controlled series compensation (TCSC)*, IEEE Power Engineering Society, 1993 Winter Meeting

[2] I.L. Somos, D.E. Piccone, L.J. Willinger & W.H. Tobin, *Power semiconductors - a new method for predicting the on-state characteristic and temperature rise during mult-cycle fault currents*, IEEE Transactions on Industry Applications, Nov.-Dec. 1995

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[4] L.O. Eriksson, D.E. Piccone, L.J. Willinger & W.H. Tobin, *Selecting fuses for power semiconductor devices*, IEEE Industry Applications Magazine, Sept./Oct. 1996

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[6] R. Dethlefsen, *Evolving pulse power industrial market requires better solid state switches*, PCIM Magazine, February, 1996