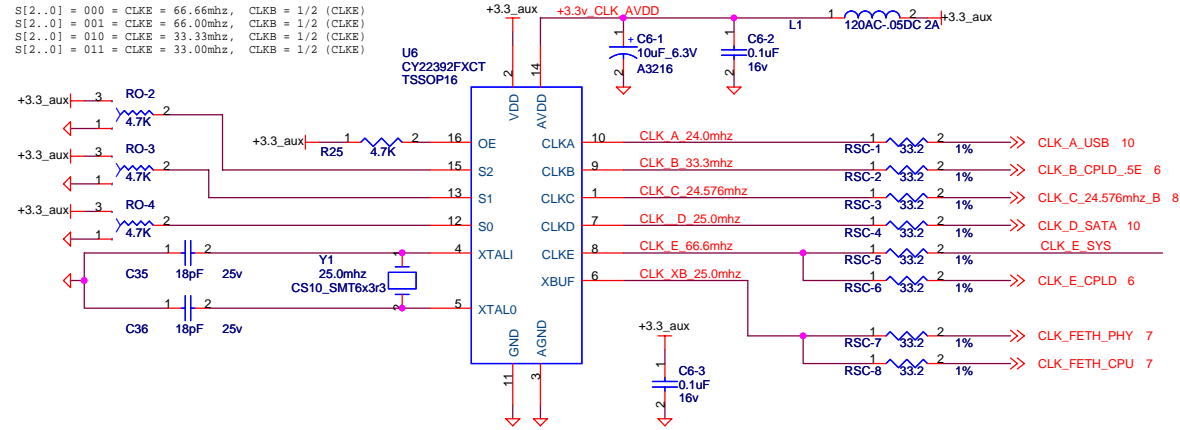
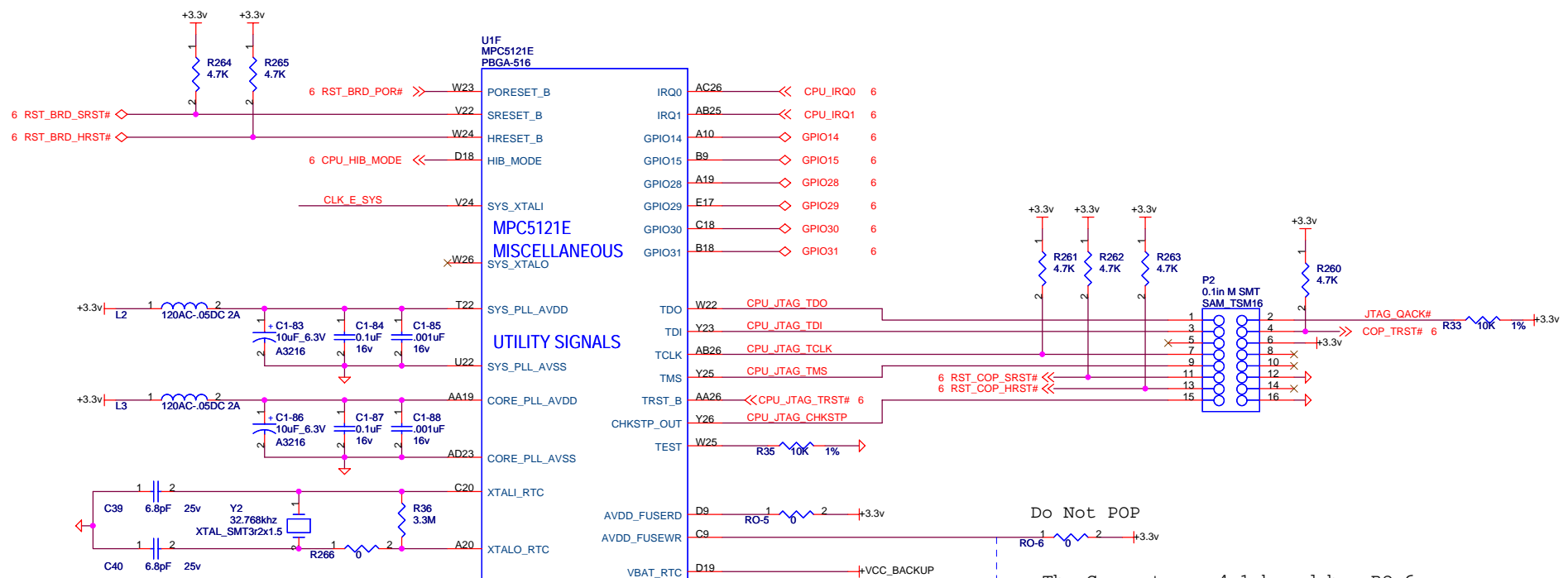
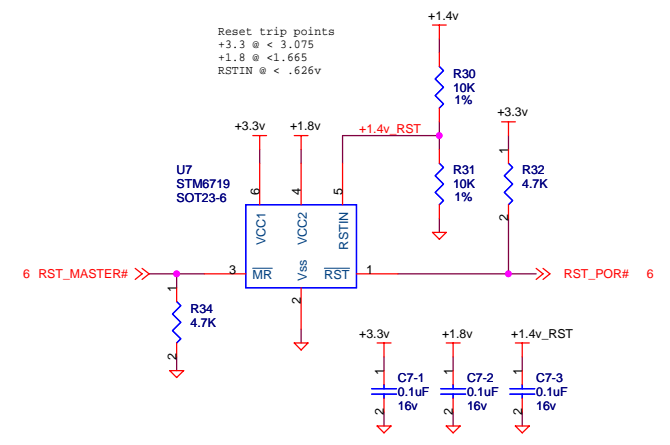
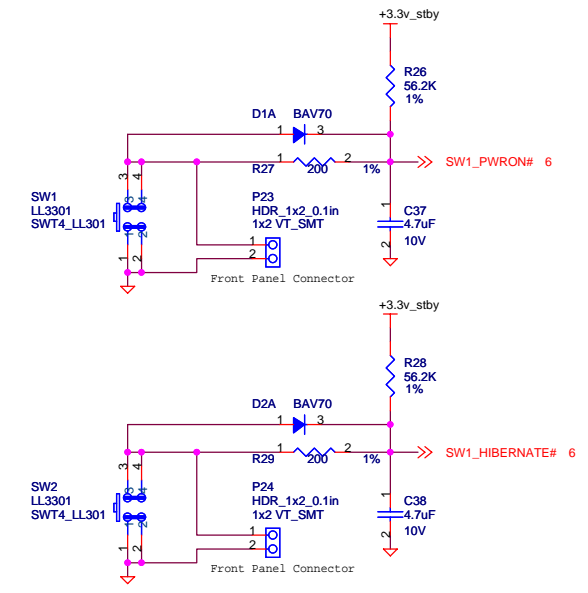


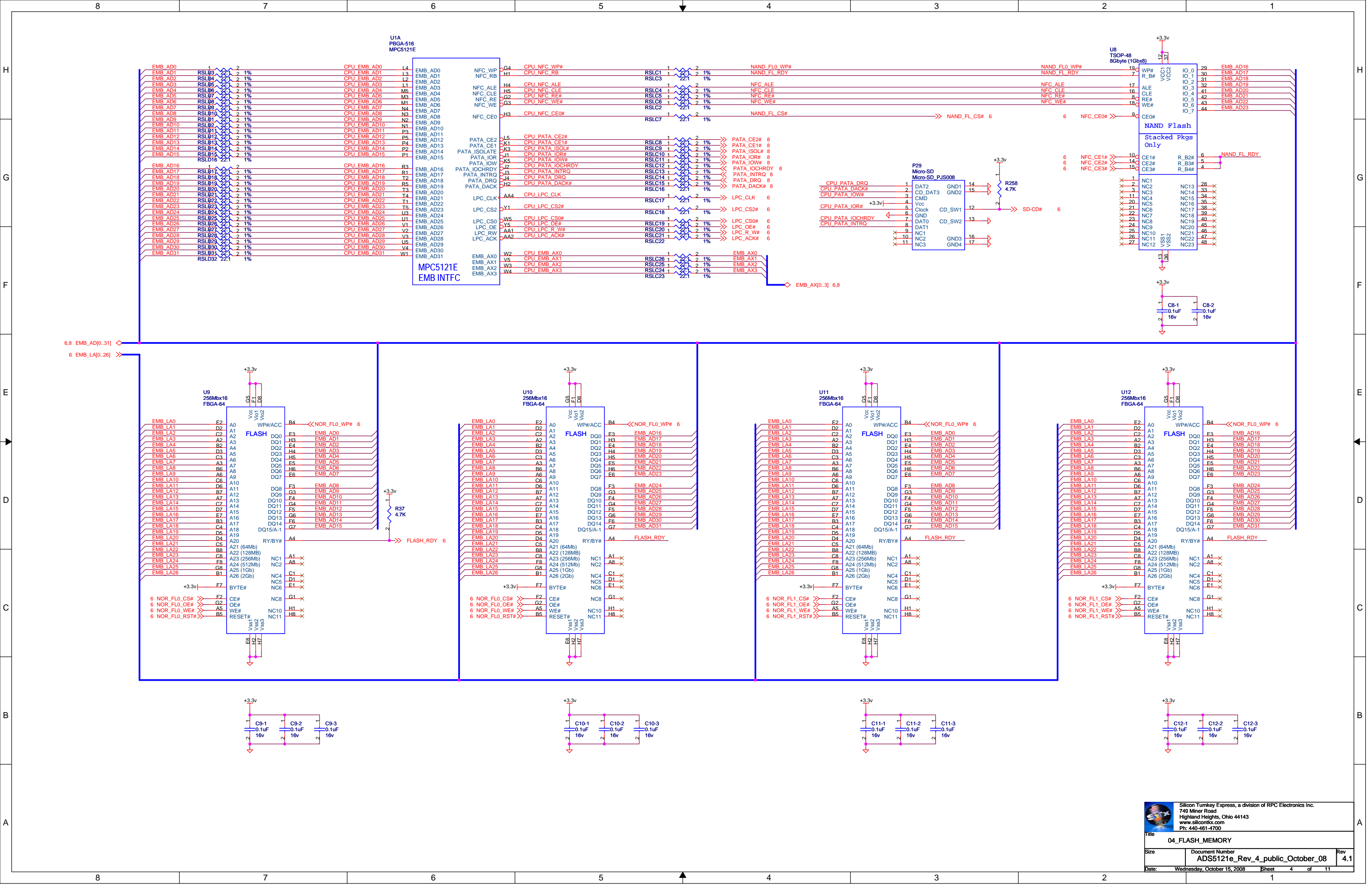
S[2..0] = 000 = CLKE = 66.66mhz, CLKB = 1/2 (CLKE)
 S[2..0] = 001 = CLKE = 66.00mhz, CLKB = 1/2 (CLKE)
 S[2..0] = 010 = CLKE = 33.33mhz, CLKB = 1/2 (CLKE)
 S[2..0] = 011 = CLKE = 33.00mhz, CLKB = 1/2 (CLKE)

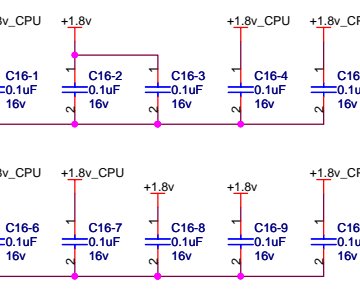
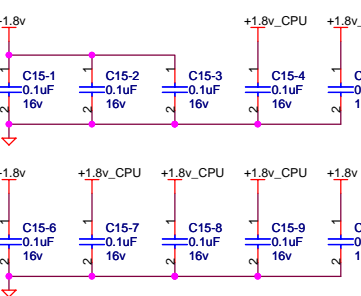
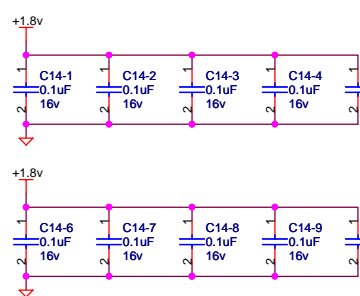
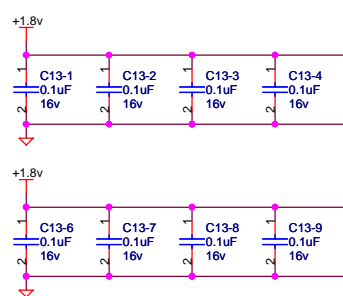
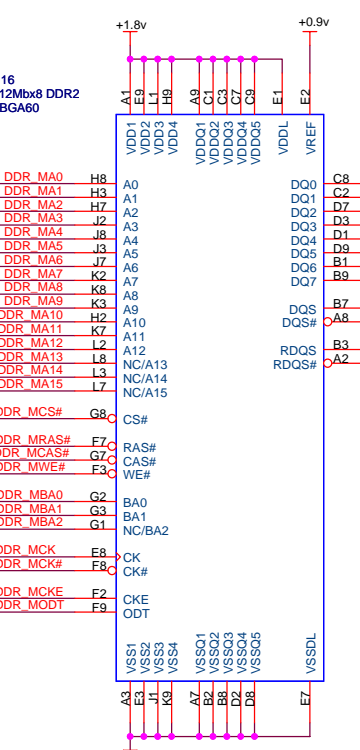
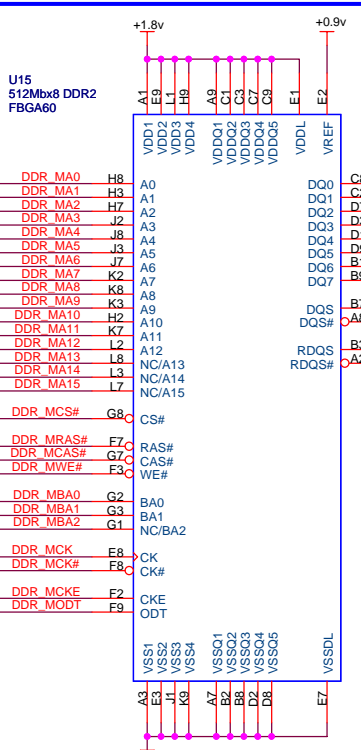
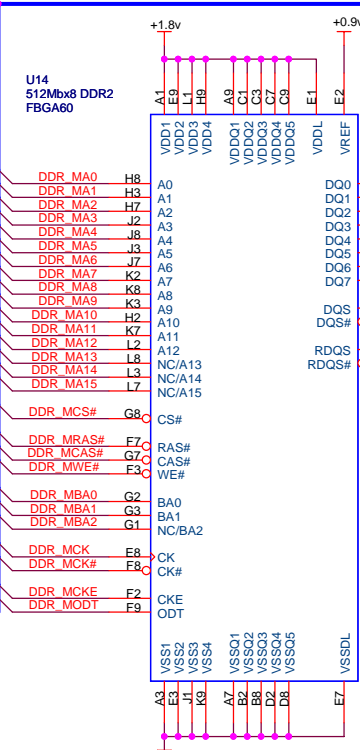
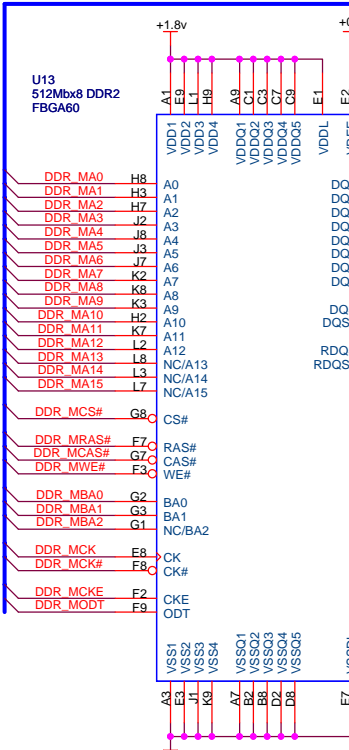
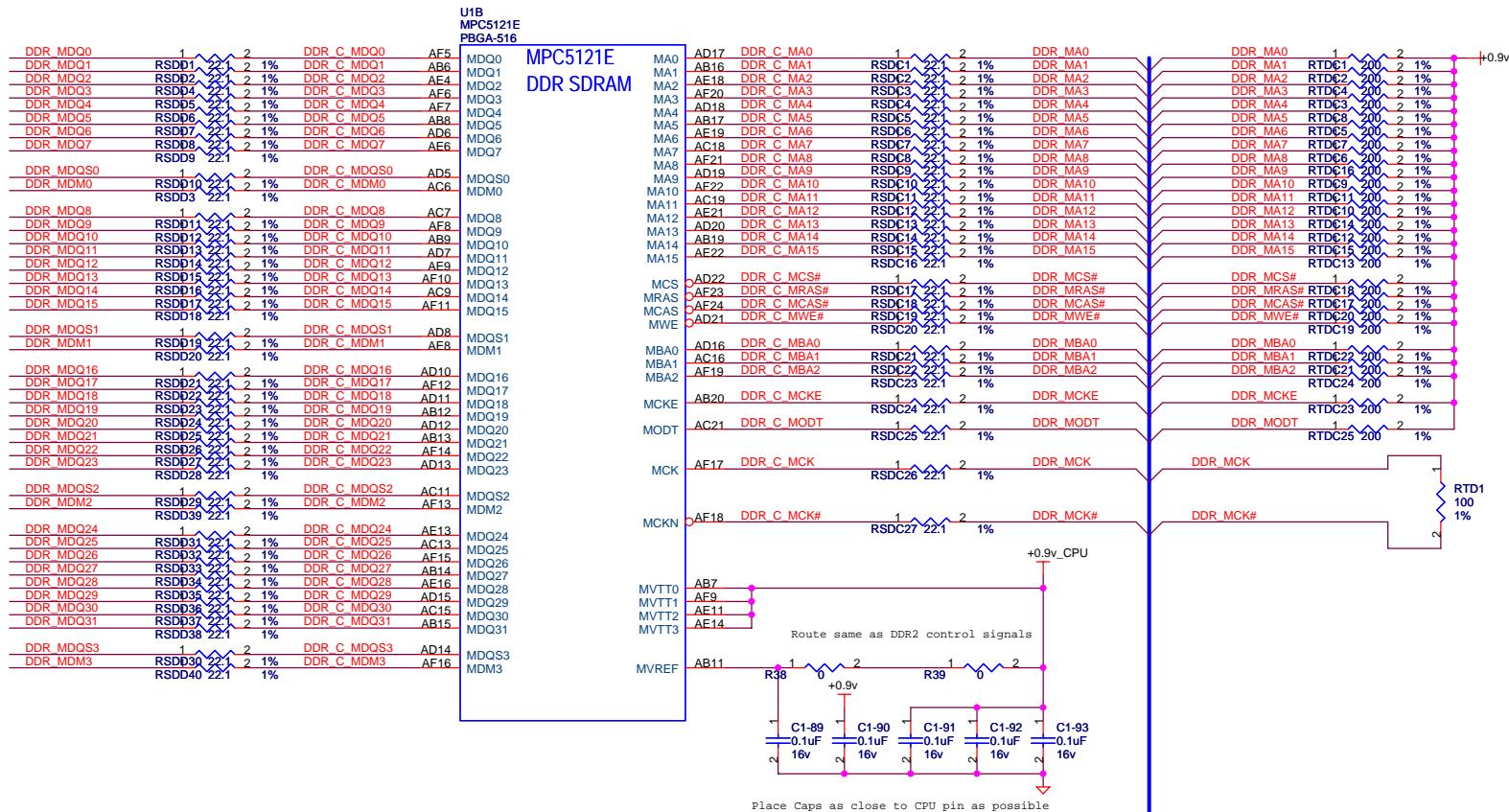


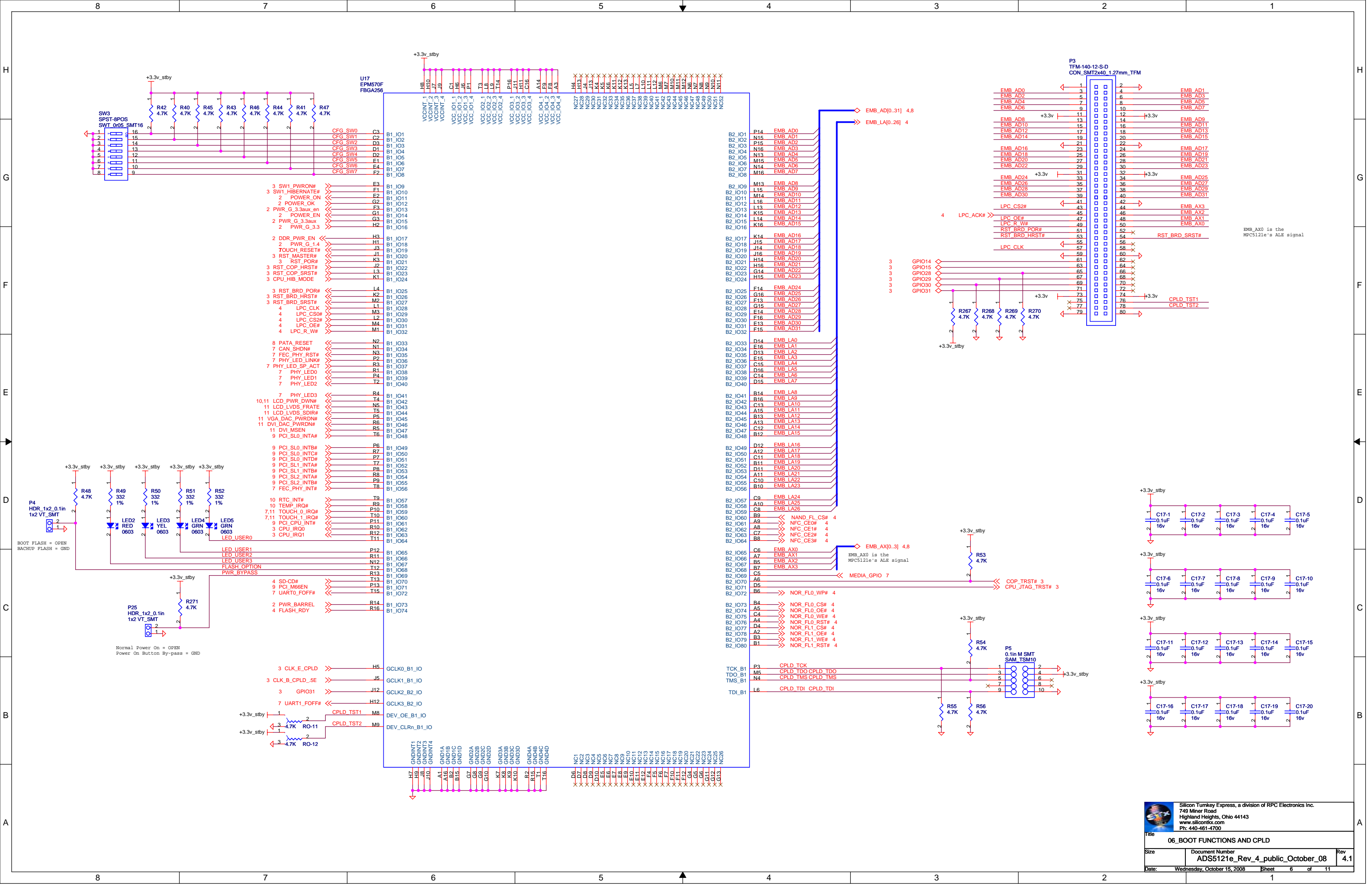
CLOCK RULES:
 All Clock traces are to be as short as possible
 CLK_E_SYS = CLK_E_CPLD
 CLK_FETH_PHY = CLK_FETH_CPU



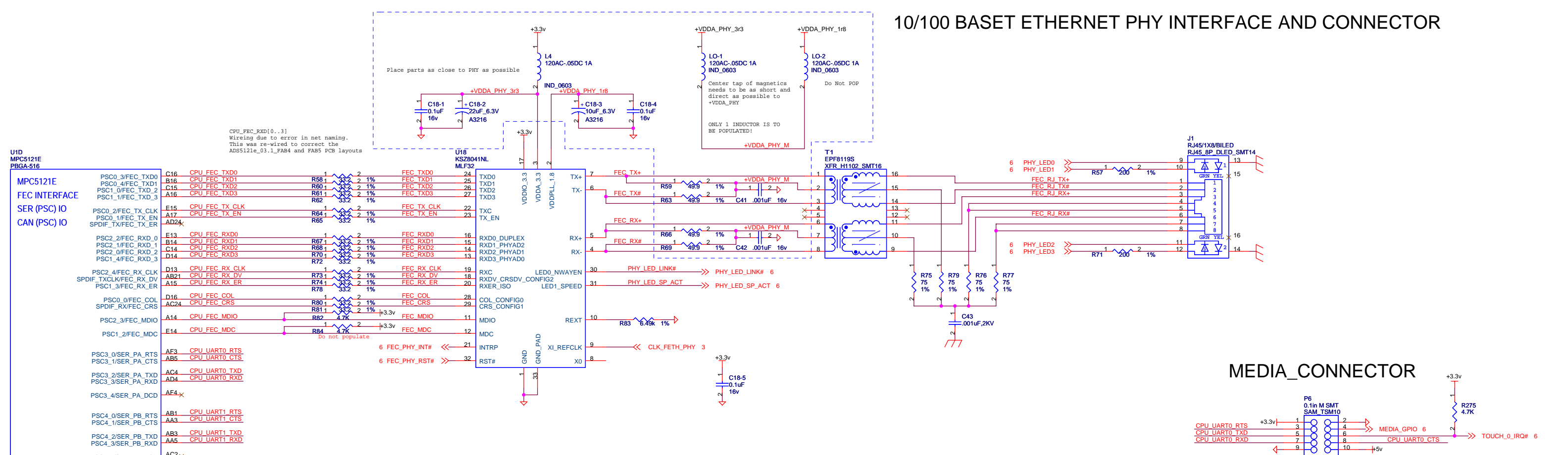
Do Not POP
 The Current rev 4.1 board has RO-6
 Removed
 and Pin C9 (FUSWR) is left floating.
 Future designs should have pin C9
 (FUSWR) connected to GND







10/100 BASET ETHERNET PHY INTERFACE AND CONNECTOR

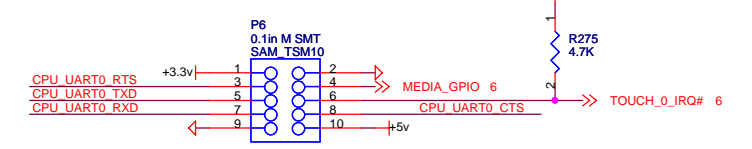


U1D MPC5121E PBGA-516

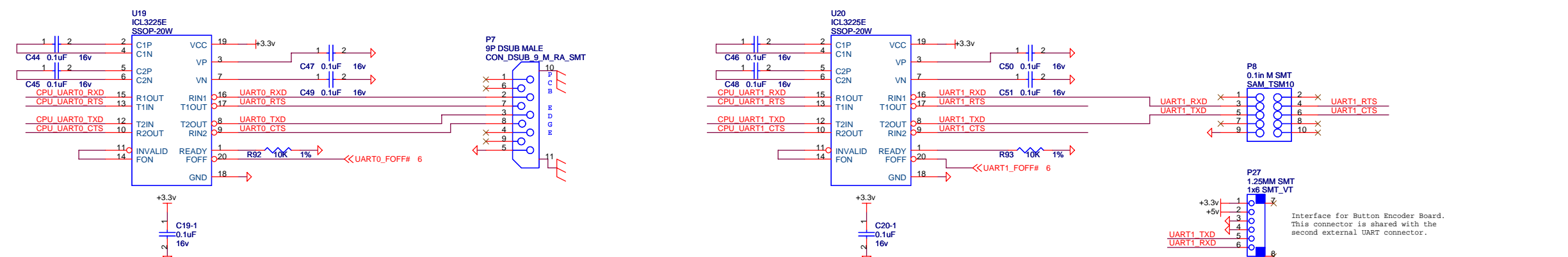
PSC0_3/FEC_TXD0
PSC0_4/FEC_TXD1
PSC1_0/FEC_TXD2
PSC1_1/FEC_TXD3
PSC0_2/FEC_TX_CLK
PSC0_1/FEC_TX_EN
SPDIF_TX/FEC_TX_ER
PSC2_2/FEC_RXD_0
PSC2_1/FEC_RXD_1
PSC2_0/FEC_RXD_2
PSC1_4/FEC_RXD_3
PSC2_4/FEC_RX_CLK
SPDIF_TXCLK/FEC_RX_DV
PSC1_3/FEC_RX_ER
PSC0_0/FEC_COL
SPDIF_RX/FEC_CR_S
PSC2_3/FEC_MDIO
PSC1_2/FEC_MDC
PSC3_0/SER_PA_RTS
PSC3_1/SER_PA_CTS
PSC3_2/SER_PA_TXD
PSC3_3/SER_PA_RXD
PSC3_4/SER_PA_DCD
PSC4_0/SER_PB_RTS
PSC4_1/SER_PB_CTS
PSC4_2/SER_PB_TXD
PSC4_3/SER_PB_RXD
PSC4_4/SER_PB_DCD
PSC5_0/AC97_CLK
PSC5_1/AC97_SYNC
PSC5_2/AC97_TX
PSC5_3/AC97_RX
PSC5_4/AC97_RST#
CAN0_TX
CAN0_RX
CAN1_TX
CAN1_RX
PSC_MCLK_IN

C16 CPU FEC TXD0
B16 CPU FEC TXD1
C15 CPU FEC TXD2
A16 CPU FEC TXD3
E15 CPU FEC TX CLK
A17 CPU FEC TX EN
AD24
E13 CPU FEC RXD0
B14 CPU FEC RXD1
C14 CPU FEC RXD2
D14 CPU FEC RXD3
D13 CPU FEC RX CLK
AB21 CPU FEC RX DV
A15 CPU FEC RX ER
D16 CPU FEC COL
AC24 CPU FEC CRS
A14 CPU FEC MDIO
E14 CPU FEC MDC
AF3 CPU UART0 RTS
AB5 CPU UART0 CTS
AC4 CPU UART1 TXD
AD4 CPU UART1 RXD
AF4
AB1 CPU UART1 RTS
AA3 CPU UART1 CTS
AB3 CPU UART1 TXD
AA5 CPU UART1 RXD
AC2
AC1 AC97_CLK
AC3 AC97_SYNC
AD1 AC97_TX
AD2 AC97_RX
AE3 AC97_RST#
A18 CPU CAN0 TXD
C19 CPU CAN0 RXD
E16 CPU CAN1 TXD
B19 CPU CAN1 RXD
C17 CLK_FETH_CPU_3

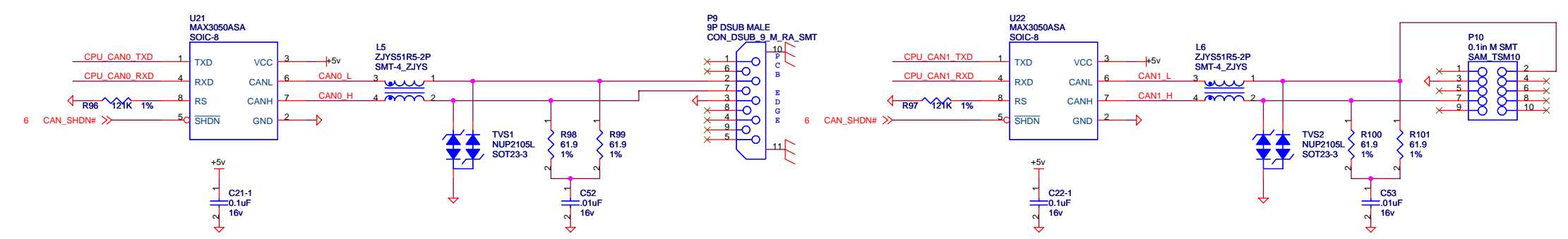
MEDIA_CONNECTOR



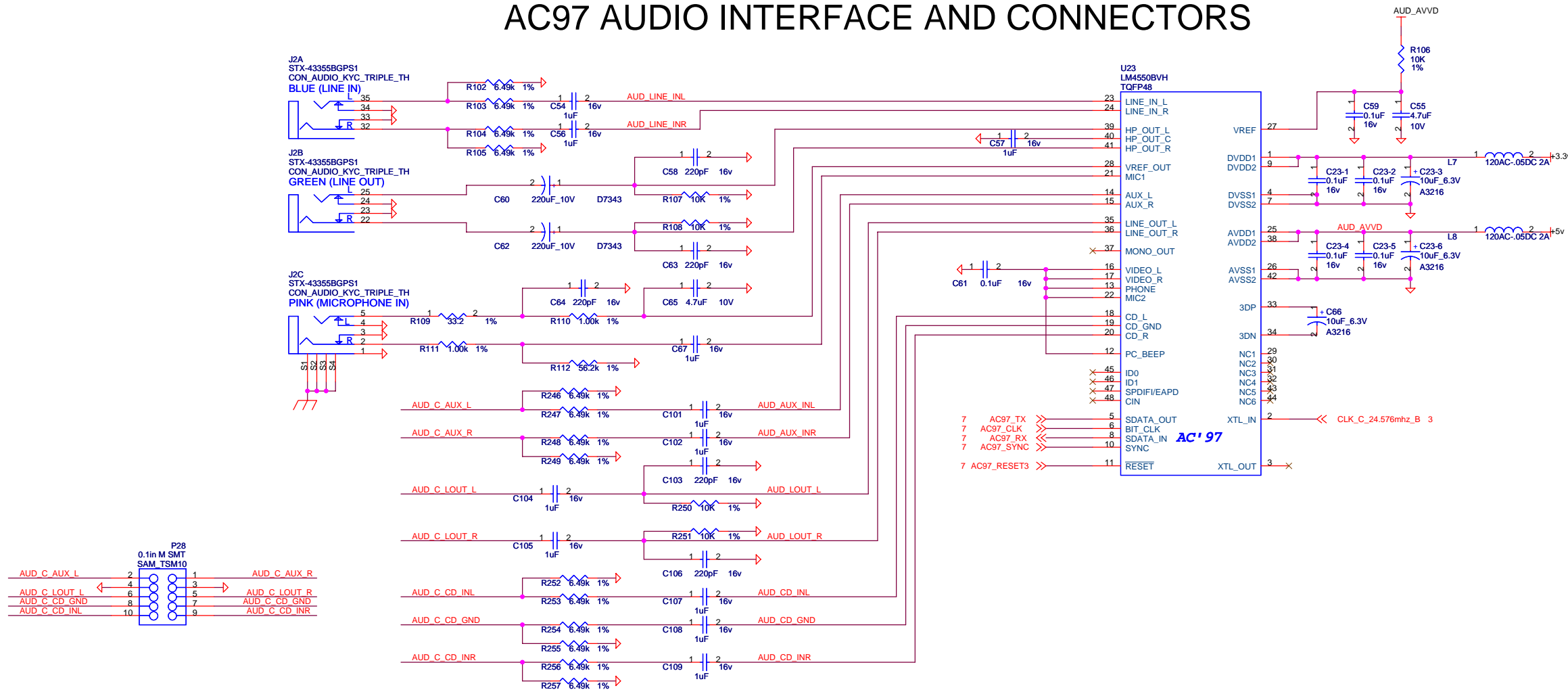
RS232 UARTS



CAN BUS



AC97 AUDIO INTERFACE AND CONNECTORS



PATA INTERFACE AND CONNECTOR

