NOTES:

1. FABRICATE BOARD PER:
   - _____ MIL-P-55110
   - X IPC TYPE 3, CLASS 2.
2. MATERIAL:
   - X LAMINATE AND PREPREG SHALL CONFORM TO IPC-4101/26 OR BETTER, MUST BE "LEAD FREE COMPATIBLE", MEET ROHS DIRECTIVE 2002/95/EC, AND HAVE A FLAMMABILITY RATING OF UL 94V-1 MINIMUM.
   - SEE "DETAIL A" FOR LAYERING STRUCTURE.
3. COPPER THICKNESS:
   - 1 OZ. EXTERNAL 1 OZ. INTERNAL LAYERS
4. FINISH:
   - _____ SMOBC WITH HASL PLATING.
   - _____ TIN/LEAD PLATING:
   - _____ HARD GOLD PLATING (DEPICTED IN AREA SHOWN)
   - X ENIG (Electroless Nickel, immersion Gold) per IPC-4552
5. SOLDER MASK:
   - _____ LPI PER IPC-SM-840 (CURRENT REV) WITH SEMI-GLOSS FINISH MUST BE "LEAD-FREE PROCESS COMPATIBLE"
   - X Encroach the s/mask onto the via pads, leaving a 3-mil clearance per side of the drill to keep the s/mask out of these holes. Then plug/ cap these vias on the top side (where the BGAs are located) per print instruction "after" the application of the Gold immersion. The bottom side will remain encroached.
6. SILKSCREEN:
   - _____ NONE
   - X WHITE (ALL SILKSCREEN TO BE REMOVED FROM ANY EXPOSED PLATED AREAS) MUST BE "LEAD-FREE PROCESS COMPATIBLE"
7. DIMENSIONING AND TOLERANCING PER ANSI-Y-14.5 (1982).
8. ALL UNUSED INTERNAL PADS SHALL BE REMOVED.
9. COPPER ON ANY LAYER CLOSER THAN .015 FROM THE EDGE SHALL BE TRIMMED BACK A/R.
10. COPPER THIEVING MAY BE ADDED TO TOP AND/OR BOTTOM SIDE. THE CLOSEST TO ANY COPPER FEATURE IS .050.
11. MUST ADD BREAK AWAY RAILS AS A MINIMUM, OR PREFERED A PANEL SIZE OF 18x24.
12. PANEL DRAWING MUST BE RETURNED
13. ALL VIAS SHALL BE PLUGGED
14. manufacture with rout tolerance of +/-.005"".
15. The via tolerance (holes .015"" and under) will be +.003"" - finished hole size- the component holes of +/-.003""- and the unplated holes of +/-.002""

LAYERING STRUCTURE DETAIL

NOTE: THIS IS A CONTROLLED IMPEDANCE PRINTED CIRCUIT BOARD.
ASSUMED VALUES AND EXPECTED IMPEDANCE ARE AS FOLLOWS:
* 1.00 OZ COPPER - ALL LAYERS
* 4 MIL TRACES, 50 OHMS +/- 5xxx - ALL SIGNAL LAYERS
* 4 MIL TRACES (DIFF PAIRS), 100 OHMS +/- 5xxx - ALL SIGNAL LAYERS
* TRACE WIDTHS MAY BE MODIFIED IN ORDER TO MEET THE IMPEDANCE REQUIREMENTS (0.00325" MIN FINISHED)

REVISIONS			
Rev	DESCRIPTION	DATE	APPROVED
4.0	ADS5121e	3-11-08	

THIS DRAWING HAS BEEN CREATED USING A COMPUTER GRAPHIC PROCESS TO INSURE THE INTEGRITY OF THE DATA BASE, ALL CHANGES OR REVISIONS MUST BE MADE ON THE PADS POWERPCB SYSTEM.

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Bottom

FILM TOOL REFERENCE CHART	
QTY	DESCRIPTION
1	DRILL DRAWING
8	MASTER LAYER PATTERNS
2	MASTER SOLDER MASK, BOTH SIDES
2	MASTER SILKSCREEN, BOTH SIDES

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS IN INCHES
TOLERANCES
FRACTIONS +/-1/64
ANGLES +/-2 DEC.
DEC XX +/-.02 XXX +/-.005

PROPRIETARY DATA

DRAWN	DATE
CHECKED	
ENGR	
APPROVED	
RLSE DATE	

TITLE: ADS5121e

SIZE	PART NUMBER	REV
D	ADS5121e_3.2_PCB_01	4.0

SCALE 1/1 SHEET 8 OF 1

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